INTELLIGENT 100MHz OSCILLOSCOPE SYSTEM TYPE 5110

Workshop Manual.

GOULD

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Workshop Manual.

GOULD

Hainault Essex England

Telephone 01-500 1000
Telegrams Attenuate Ilford
Telex 263785

ADDENDUM SHEET FOR 5110 MANUAL

'Y' PRE-AMP

Add the following components:-

R45	CF	82	Part No. 28717
R46	CF	82	Part No. 28717
R59	CF	56	Part No. 28715
R60	CF	56	Part No. 28715
R79	CF	82	Part No. 28717
R80	CF	82	Part No. 28717
R81	CF	820	Part No. 44225
R82	CF	820	Part No. 44225
R87	MF	270	Part No. 452442
R88	MF	270	Part No. 452442
R89	MF	270	Part No. 452442
R90	MF	270	Part No. 452442
R93	MF	1M	Part No. 451608
R94	MF	1M	Part No. 451608
C59	CE(3)	12pF	Part No. 42409
C60	CE(3)	12pF	Part No. 42409
C83	CE(2)	1000pF	Part No. 22387
C84	CE(2)	1000pF	Part No. 22387
C89	CE(2)	15pF	Part No. 22366
C90	CE(2)	15pF	Part No. 22366

Amend to read:-

R120 Delete 2% add 0.25%, amend Part No. to read 452441

R121 Delete 2% add 0.25%, amend Part No. to read 452441

R123 Add to read 6R8 MF Part No. 38542

R136 Delete 2% add 0.5%, amend Part No. to read 452443

R137 Delete 2% add 0.5%, amend Part No. to read 452443

R320 Delete 2% add 0.25%, amend Part No. to read 452441

R321 Delete 2% add 0.25%, amend Part No. to read 452441

R323 Add to read 6R8 MF Part No. 38542

R324 Delete 2% add 0.1%, amend Part No. to read 452440

R325 Delete 2% add 0.1%, amend Part No. to read 452440

R336 Delete 2% add 0.5%, amend Part No. to read 452443

R337 Delete 2% add 0.5%, amend Part No. to read 452443

R490 Delete 2k2 add 270, amend Part No. to read 28720

R494 Delete 2k2 add 270, amend Part No. to read 28720

R495 Delete 2k2 add 270, amend Part No. to read 28720

R496 Delete 2k2 add 270, amend Part No. to read 28720

R569 Delete 2k2 add 1k8, amend Part No. to read 44229

R575 Delete 2k2 add 2k7, amend Part No. to read 44232

N83 Add to read 'RESISTOR NETWORK' Part No. 43135

N84 Add to read 'RESISTOR NETWORK' Part No. 43135

N501 Delete 560 x 8 add 270 x 8, amend Part No. to read 450697

C519 Delete intoto add 'NOT FITTED'.

L1, L2, L3, L4, Add under "Miscellaneous" Part No. 26986

TIMEBASE

R1413 Delete 2k2 add 4k7, amend Part No. to read 21805

R1418 Delete 180, add 120, amend Part No. to read 28718

R1501 Add to read 820 CF Part No. 44225

R1537 Delete 180, add 270, amend Part No. to read 43716

R1538 Delete 120, add 180, amend Part No. to read 43715

C1545 Add 150pF CE(3) Part No. 451799

C1653 Delete 1nF, add 100nF, amend Part No. to read 43498

C1656 Delete 1nF, add 100nF, amend Part No. to read 43498

C1663 Delete 1nF, add 100nF, amend Part No. to read 43498

C1666 Delete 1nF, add 100nF, amend Part No. to read 43498

DATA DISPLAY

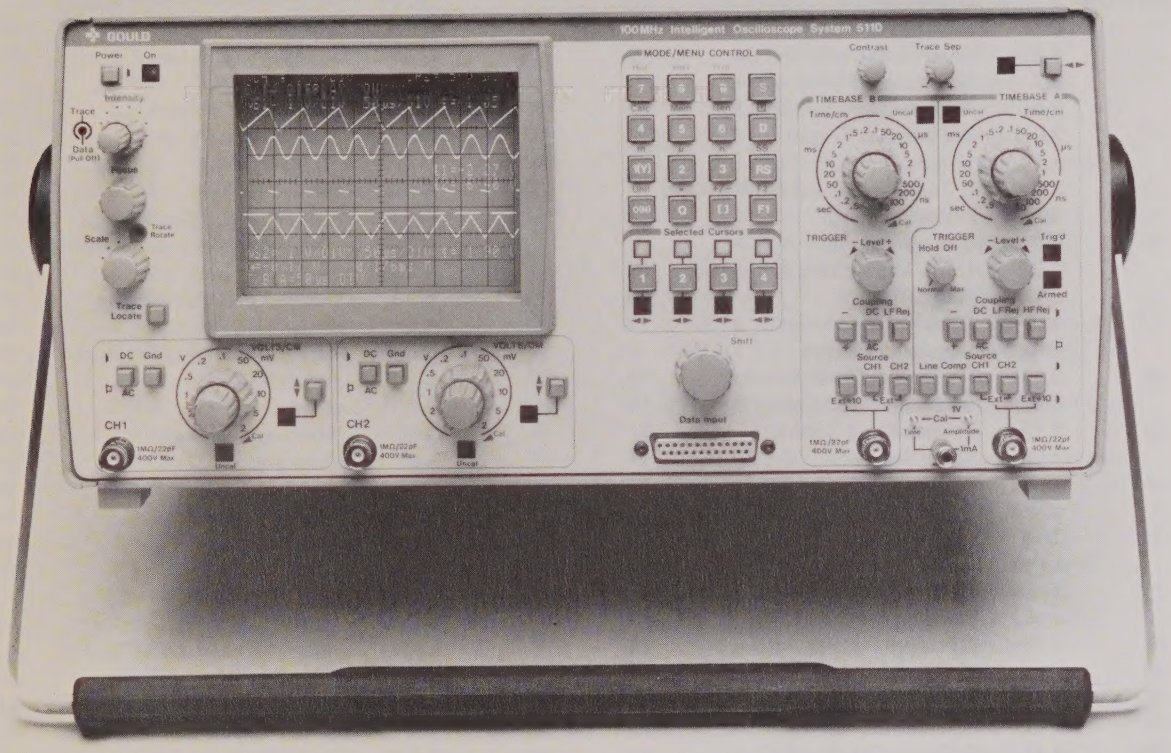
C2716 Delete intoto.

I.E.E.E. OPTION 5104

N2945 Add to read 68 x 4 'RESISTOR NETWORK'
Part No. 452931

N2946 Add to read 68 x 4 'RESISTOR NETWORK'
Part No. 452931

R2902 Add to read 10k CF Part No. 21809


GOULD
100MHz Intelligent Oscilloscope System 5110
Power
On
Intensity
Trace
Data
(Pull Off)
Focus
Scale
Trace Rotate
Trace Locate
MODE/MENU CONTROL
Selected Cursors
Shift
Data Input
Contrast
Trace Sep
TIMEBASE B
TIMEBASE A
Time/cm
Uncal
TRIGGER
Level
Hold Off
Coupling
DC
LFRej
HFRej
AC
Source
CH1
CH2
Line
Comp
Ext
Ext/10
Trig'd
Armed
Cal
Trace
Amplitude
1mA
DC
Gnd
AC
VOLTS/Cal
CH1
CH2
1MΩ/22pF
400V Max
1MΩ/32pF
400V Max

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DISPLAY

CRT 8 x 10cm rectangular.

EHT 16kV.

Graticule Internally, with 8 x 10cm divisions and 2mm sub-divisions. Independent continually variable illumination for Trace and Data.

Phosphor P31 standard.

Trace Locate Compresses trace to within graticule area.

VERTICAL DEFLECTION

Two identical input channels.

Bandwidth DC–100MHz (-3dB) DC coupled.
2Hz–100MHz (–3dB) AC coupled.

Sensitivity 2mV/cm to 5V/cm.
Uncalibrated fine gain control gives continuous adjustment between ranges with 'Uncal' warning light and symbolic indication on screen.

N.B. Bandwidth at 2mV/cm limited to 85MHz.

Accuracy ±3% in calibrated position.

Input Impedance 1M Ω/22pF.

Input Coupling AC–Ground–DC.

Maximum Input Voltage 400V DC or pk AC.

Display Modes Channel 1 only.
Channel 2 only.
Channel 1 and Channel 2 chopped (500kHz approx).
Channel 1 and Channel 2 alternate.
Channel 1 and Channel 2 added.
Trigger View, CH1 and/or CH2 alternate or chopped.
Trigger View, alternate or chopped with CH1 and CH2 added.
Channel 1 and/or Channel 2 can be inverted.
x 10 probe scaling selection for calculation mode.

HORIZONTAL DEFLECTION

Display Modes Main Timebase A.
Main Timebase A intensified by delayed Timebase B.
Delayed Timebase B.
Main Timebase A and delayed Timebase B simultaneously (alternate sweeps).
X-Y with 'A' trigger defining X deflection input source.

TIMEBASE (A)

Sweep Speeds 50ns/cm to 0.5s/cm in 22 steps (1-2-5 sequence).

Fine Sweep Control Uncalibrated. Reduces sweep rate up to 2.5 times
(slowest sweep approx. 1.25s/cm).
Warning light indicates uncalibrated condition and symbolic indication on screen.

Expansion x 10 gives max. sweep rate of 5ns/cm.

Accuracy ±3% (±5% with x 10 expansion).

DELAYED TIMEBASE (B)

Sweep Speeds 50ns/cm in 22 steps (1-2-5 sequence).

Fine Sweep Control Uncalibrated. Reduces sweep rate up to 2.5 times.
(slowest sweep approx. 1.25s/cm)
Warning light indicates uncalibrated condition and symbolic indication on screen.

Expansion x 10 gives max. sweep rate of 5ns/cm.

Accuracy ±3% (±5% with x 10 expansion).

Trace Separation Operates in A+B timebase alternate sweep mode and provides up to ±4.0cm shift on the B sweep.

Common Variable Control (Shift) Y CH1, YCH2, X and the four cursors are positioned by the common control assigned by the dedicated push button. Also control of trigger delay, trigger division ratio and phase steps.

TRIGGER

	Trigger (A)	Trigger (B)
Source	Internal CH1 Internal CH2 Composite (CH2/CH2) External External ÷ 10 Line	Internal CH1 Internal CH2 External External ÷ 10
Slope	Positive/Negative	Positive/Negative
Coupling	DC, AC, AC (If rej. AC (Hf rej.)	DC, AC, AC (If rej.)
Modes	Manual level Auto Bright Line Single shot Arm Single shot Manual Trigger Delay	Manual level Cursor Cursor + Delay Cursor + 'B' Trigger Delay Delay + 'B' Trigger Start at 'A'
Delay	Time, 10ns to 344 seconds 6 digit resolution Accuracy ±0.002% ±1 count Digital, 0–999,999,999 events	
Sensitivity	Internal To 10MHz<2mm (below 50Hz sensitivity decreases when AC coupled) 10MHz to>100MHz <1cm	Internal To 10MHz<2mm (below 50Hz sensitivity decreases when AC coupled) 10MHz to>100MHz <1cm

	External: To 10MHz at 10mV (100mV with ÷ 10 Below 50Hz sensitivity decreases when AC coupled. 10MHz to>100MHz <50mV (<0.5V with ÷ 10) Level range (internal): ±8cm. Level range (external): ±0.5V approx (±5V with ÷ 10)	External: To 10MHz at 10mV (100mV with ÷ 10 Below 50Hz sensitivity decreases when AC coupled. 10MHz to >100MHz <50mV (<0.5V with ÷ 10) Level range (internal): ±8cm Level range (external): ±0.5V approx (±5V with ÷ 10)
External Trigger	Input impedance, 1MΩ/22pF. Max.input volt. 400V (DC plus AC pk)	Input impedance, 1MΩ/22pF. Max.input volt. 400V (DC plus AC pk)

Trigger Hold-off Continuously variable up to approx one sweep length of main timebase, except for three slowest ranges.

Calibrator Voltage: 1V±1%, 1KHz approx.

Current: 1mA between 'CAL' voltage output and OV,1KHz approx.

Time: Front panel output of time is provided from an internal crystal oscillator, for calibration in the X axis, 40ns–344 secs., 6 digit resolution, min. step 20ns. Accuracy; 1 part in 10^5.

SYSTEM MEASUREMENT ACCURACY (15–35°C)

Differential measurement by centre line (single channel):
±(0.5% of reading + (0.4% of V/div. or 1 l.s.d.))

Current cursor voltage and voltage from programmed datum reference:
±(0.5% of ℄ reading + (0.5% of cursor voltage–℄ voltage) +4% of V/div. or 1 l.s.d.) after automatic zero correction

Current cursor time:
Analogue-
±(0.5% of reading + (0.1% of time/div. or 1 l.s.d))
Crystal-
For values >300μs
±(0.01% of reading + 20ns + 1 l.s.d.))

For values from 10μs–300μs
±(0.1% of reading + 1 l.s.d.)

For values <10μs
±(1% of reading + 1 l.s.d.)

Differential voltage or time and automatically calculated results, typically ±2%.
Measurements on stored waveforms, typically ±3%.

REAR PANEL

A Ramp
A timebase ramp output 2 volts peak from 50Ω source impedance

B Gate
High output for the duration of the B timebase.
TTL compatible.

Z Modulation Input
Bandwidth: DC to 10MHz.
Sensitivity: +4V from zero gives complete blanking.
Input Impedance: 2.2kΩ.

DIGITAL FACILITIES

Store size 2048 x 8 bits.

Vertical Resolution 1024 for each channel (approx 100 samples/cm).

Max. Sample Rate 1MHz (1μs/sample) reducing in proportion with timebase range.

Repetitive Sampling 1K samples stored over sequential timebase sweeps.

Real time 1K samples/channel stored in one timebase sweep.

Auxiliary store 8 sets of machine states with associated pair of stores. Scaling parameters stored with each trace. (Non-volatile).

Cursors Four cursors numbered 1–4 individually selected.
Indicated by bright up on trace, nominally 1mm horizontal width on A timebase.

DISPLAY MODES

Single or dual trace display of real time, repetitively sampled or transient storage of waveforms with alpha-numeric indication of:
–scale factors for input sensitivities and timebase
–measurement results.
or Menu selection for vertical, horizontal trigger, calculation, memory and plot mode functions.
Storage of last used settings with battery back-up.

GENERAL

Supplies 100V, 120V, 220V, 240V, 45–65Hz, 225W.

Size 184mm x 440mm x 630mm (7.25in x 17.3in x 24.8in).
176mm x 390mm x 590mm (7in x 15.35in x 23.25in excluding the handle and feet).

Weight 19.5kg (43 lbs)

Temperature Range Operating 0–50°C.
Full spec. 15–35°C.

ANALOGUE OUTPUT (Plot)

Plot Mode Menu selected start.

Y OUTPUT

An output via BNC connector selected from store 1 or store 2.

Amplitude: 100mV per cm of screen height Bipolar output with OV corresponding to the middle of the screen.

Accuracy Output voltage per cm of display ±3%.
Output to input voltage (cal) ±3%.
± fullscale pre-setable for external cal.

Bandwidth DC–16KHz (–3dB)

X OUTPUT

X ramp via BNC connector.

Amplitude 100mV per cm of screen width.
Positive ramp resetting to OV.

Accuracy Output voltage per cm of display ±3%.
Output voltage per unit of time recorded ±3%.
Time output accuracy of Y Channel outputs ±1% (record to replay ratio).

Output impedance Output 1,2, and X ramp 100Ω/0.1μF.
Continuous short circuit protection.

Output Rate Internal clock, 50s/cm–20ms/cm.

Plot marker output TTL compatible.

Pen lift
Contacts isolated. Single contact closes from Start command to the end of read-out cycle.

Rating 50V d.c., 250mA d.c.

Isolation 50V max.

GPIB IEE–488

The optional IEEE interface printed circuit board allows the OS5100 to transmit and receive stored data, control settings and calculation results.

SH1 SOURCE HANDSHAKE – COMPLETE CAPABILITY
AH1 ACCEPTOR HANDSHAKE – COMPLETE CAPABILITY
T5 BASIC TALKER, SERIAL POLL, TALK ONLY UNADDRESS IF MLA.
TE0 EXTENDED TALKER – NO CAPABILITY.
L3 BASIC LISTENER, LISTEN ONLY, UNADDRESS IF MTA.
LE0 EXTENDED LISTENER – NO CAPABILITY.
SR1 SERVICE REQUEST – COMPLETE CAPABILITY.
RL1 REMOTE/LOCAL – COMPLETE CAPABILITY.
PP0 PARALLEL POLL – NO CAPABILITY.
DC1 DEVICE CLEAR – COMPLETE CAPABILITY.
DT1 DEVICE TRIGGER – COMPLETE CAPABILITY.
C0 CONTROLLER – NO CAPABILITY.

GENERAL

ACCESSORIES SUPPLIED

Two Probe Kits PB18
A passive Probe Kit with x 10 attenuation.
Input Impedance is 10MΩ/18pF.

OPTIONAL ACCESSORIES

Viewing Hood PN42224

Trolley TR7 General Purpose Oscilloscope Trolley.

Protective Carrying Case PN452343
A strong carrying case which completely encloses the oscilloscope with three thicknesses of padded material covering the front panel.

Rack Mount Kit PN452344

Front Panel Cover PN452121

PB100 DATA POD (Optional)

INPUTS

Number Eight signals and two qualifiers.

Impedance 50KΩ, 8 pF nominal.

Threshold Fixed TTL (÷1.4V) and ECL (–1.3V), adjustable approximately ±12V nominal. Test point measurement of one tenth actual level.

Minimum Pulsewidth 10nsec at 500 mV threshold overdrive.

Maximum Voltage ±25V continuous.

CLOCK

Input Via Q1 or Q2, same electrical specification as data inputs above. One input may be the clock and the other a qualifier. Logic sense switches provided.

Output Via BNC cable. Bipolar signal: ZERO level–1.7V; ONE level +2V nominal.

TRIGGER

Source Via eight switches: 1,X (Don't care), and 0. For the time period that the input signals satisfy the combination selected, a positive level (+2V) is output.

Qualifiers Q1 and Q2 may be used to qualify the 8 bit parallel word.

Output Via BNC cable, TTL level. LED indicator blinks on for 0.5 sec when trigger occurs.

Response in FAST position, combination must be true for 20nsec minimum. In SLOW position, combination must be true for 180±25nsec.

DATA OUTPUTS

Provision Via cable with D type connector.

Levels ZERO, 0.4V, ONE, 3.4V nominal.
Noninverting with respect to input signals.

MISCELLANEOUS

Temperature Range Operating, 0 to 50°C.

Power ±5V at 360 mA, –5V at 100mA.
(Supplied from the OS5100).

Size 3.6 in. (9.2cm) wide, 6.8 in. (17.3Cm) deep, 1 in. (2.5 cm) thick; 1 lb (0.5 kg) weight.

3.1 INTRODUCTION

The 5110 has all the analogue controls and facilities of a conventional dual trace oscilloscope, but backed up by a sophisticated software system controlled by a front panel keypad (MODE/MENU CONTROL). This software system provides for the display of alphanumeric data (eg timebase and amplifier settings etc) with the traces, and also a large number of menu pages for the selection of various operational modes. Therefore, because of the instrument's versatility and complexity it is assumed that the reader is conversant with the use of modern oscilloscopes, and hence this section is concerned mainly with the use of the keypad and the menus to obtain the operational modes.

An internal nickel-cadmium battery provides a "keep-alive" voltage for the RAM stores so that when the instrument is switched on it will always start up in the operational mode that it was in when switched off. This is known as the "warm start" facility. In the event of the instrument not having been used previously (ie on receipt from the manufacturer) or the nickel-cadmium battery being completely discharged (ie the instrument having been left unused for more than 9 months), the software carries out a "cold start" procedure on switching on. This, however, can be considered as an unusual situation and as such is described elsewhere in this section (section 3.22). In general, therefore, the "warm start" can be assumed to be the normal start up procedure.

The following sections discuss, first, the basic switching on procedure and then the conventional amplifier, timebase and shift controls, the use of the keypad, and finally, the interpretation of the menu pages and the selection of the operational modes.

NOTE: The expression "default" used in this publication and appearing on displays refers to the state of specifiable operating modes. Any mode that has not been specified by the operator is specified instead by the instrument software, this being known as the default setting.

SAFETY

This instruction manual contains information and warnings which must be observed by the user to ensure safe operation and retain the apparatus in a safe condition. The instrument has been designed to operate indoors, within the specified limits of temperature. It should not be switched on if there are obvious signs of mechanical damage and it should not be used under wet conditions.

EARTHING

The instrument must be operated with a protective earth connected via the appropriate (yellow/green) conductor of the supply cable. This is connected to the instrument before the line and neutral supply connections when the supply socket is inserted into the plug on the back of the instrument. If the final connection between the instrument and the supply is made elsewhere, the user must ensure that the earth connection is made before line and neutral.

If any supply cable other than that supplied with the instrument is used, it must carry an adequate protective earth conductor.

WARNING

Any interruption of the protective earth conductor inside or outside the instrument is likely to make the instrument dangerous. Intentional interruption is prohibited.

Signal connections into the instrument should be connected after and disconnected before the protective earth connection is made, i.e. the supply lead must be connected at all times that signal leads are connected.

LIVE PARTS

The instrument is safe to operate with the covers fitted and these must not be removed under normal usage. The covers protect the user from live parts and they should be removed only by suitably qualified personnel for maintenance or repair purposes. (see maintenance section).

3.2 SAFETY AND SWITCHING ON

CAUTION: The 5110 has an integral blower motor to provide forced air cooling and must always be operated in a position such that there is no restriction to the air entering through the louvres around the unit case and exiting at the rear.

1. Set the support/carrying handle to the required operating position. The handle is released by pulling both fixing bushes outward, and can then be turned to lock in any of five positions.
2. Before connecting the 5110 to the mains supply, check that the supply range switches are set to suit that supply voltage to be used and that the correct fuse is fitted. Note that the fuse has to be changed when switching between the 100V and 220V ranges. The switches and fuse holder are mounted on the back panel of the instrument. Do not operate the supply selection switches while the instrument is switched on.
3. Push the POWER button and ensure that the ON lamp lights. An alphanumeric display should be obtained within 15 seconds and full calibrated performance within 20 minutes.
4. If necessary, adjust the FOCUS and DATA (inner) INTENSITY controls to obtain a clear display, and the SCALE control to illuminate the graticule.

3.3 Y CHANNELS OPERATION

A similar set of controls are provided for each of the Y channels, CH1 and CH2.

1. A locking push button is provided for selecting DC/AC input.

(a) For direct coupling of the input signal, select DC (button in).

(b) For coupling via the internal 0.1μF capacitor, select AC (button out).

2. Two controls are provided for deflection sensitivity.

(a) Adjust the VOLTS/CM switch to obtain the required vertical deflection.

(b) The variable VOLTS/CM control fitted concentrically with the switch provides continuous variation of sensitivity between the stepped ranges. When the variable control is turned in an anticlockwise direction from its CAL position, a red warning light (UNCAL) illuminates to show that the deflection sensitivity is no longer calibrated.

3. To locate the ground or zero volts level, operate the GND push button. This open circuits the input signal and connects the amplifier input to ground.

4. Either CH1 or CH2 can be removed from the display by operating the blue (S) push button on the keypad and the ▲▼ shift push button in sequence. The channel is restored to the display simply by pressing the ▲▼ push button a second time.

3.4 A TIMEBASE OPERATION

The speed of the A timebase is determined by the setting of the A TIME/CM switch. A variable TIME/CM control is fitted concentrically with the switch and provides a further 3:1 (approx.) variation. When the variable control is turned in an anticlockwise direction from its switched CAL position, a red warning light (UNCAL) illuminates to show that the A timebase is no longer calibrated.

The timebase setting is indicated at the bottom of the Alpha-Numeric display. When the UNCAL is operated, a > symbol is used and a := is used to indicate that the X10 scaling has modified the value.

NOTE: Any misalignment of the trace with the horizontal lines on the graticule should be corrected by adjusting the TRACE ROTATE preset control.

The CONTRAST control adjusts the contrast between the A timebase and the brightened part of the A timebase (ie that part of the trace selected for display on the B timebase).

3.5 A TIMEBASE TRIGGER

1. The A timebase may be triggered by the following sources as selected by the SOURCE locking push buttons.

(a) CH1 or CH2 selects the output of the appropriate amplifier.

(b) COMP (composite) selects a mixture of CH1 and CH2 signals such that each channel may produce a stable trace.

(c) LINE: the power supply line input frequency derived internally from the supply transformer.

(d) EXT: an external triggering source connected to the associated socket is selected when CH1 and CH2 are selected simultaneously. The sensitivity of this external input can be reduced 10 times by the additional operation of the EXT÷10 push button.

2. The LEVEL control allows the selection of the triggering point on the trigger waveform and hence the determination of the start of the horizontal trace.

3. If required, the COUPLING locking push buttons are used in conjunction with the SOURCE push buttons to connect different networks into the trigger amplifier circuit.

(a) Negative/positive (marked – +) determines whether triggering occurs as the input signal passes the selected trigger level in a negative or positive-going direction. This allows the amplifier to trigger on negative-going leading edges (button in), or on positive-going leading edges (button out).

(b) DC/AC input. AC (button out) coupling is useful for wideband trigger on most signals. The DC position (button in) is also a wideband trigger mode but is most useful at very low frequencies or when the mark-space ratio of a pulse signal is likely to wary. The Y input coupling (section 3.3) must also be set to DC for this mode to be effective on internal trigger.

(c) LF REJ (button in) switches a filter into circuit to reject low frequencies. This allows stable triggering on the high frequency component of complex waveforms by rejecting the lower frequency component(s). Note that this switch automatically reverts the trigger amplifier to an ac coupled mode even if dc trigger has been selected.

(d) HF REJ (button in) switches a dc coupled filter into circuit to reject high frequencies. This allows low frequency triggering to be effected from complex waveforms containing high frequency components. The cross-over frequency of both the hf and the lf filters is approximately 10kHz.

3.5.1 TRIGGER HOLD-OFF

When the HOLD OFF control is in its normal (fully anticlockwise) position, the hold-off circuit provides sufficient delay for the timebase to recover before the start of the next sweep. When used as a variable control its main function is to provide effective triggering on some complex waveforms.

In most positions of the timebase range switch, the

range of hold-off variation is about equivalent to the time taken for the timebase to complete one sweep. In the case where the timebase is required to be triggered on a complex waveform (eg a repetitive logic pulse pattern containing pulses of different widths), the HOLD OFF control may be used to inhibit triggering until the desired period in the waveform is reached.

NOTE: When triggering at high frequency, any slight jitter visible on the trace may be removed by fine adjustment of the HOLD OFF control.

3.6 B TIMEBASE OPERATION AND TRIGGER

The speed of the B timebase is determined by the setting of the B TIME/CM switch which, with its uncalibrated variable control, has the same ranges as the A TIME/CM switch (section 3.4). The TRACE SEP control offsets the B timebase with respect to the A.

The B trigger source selection is similar to that of the A timebase (section 3.5) but does not incorporate COMP or LINE trigger. The trigger coupling facilities are also similar to those of the A timebase but without the HF REJ push button.

There is no hold-off facility for the B timebase trigger.

3.7 SHIFT CONTROL

The single, general purpose, SHIFT control is used for CH1 and CH2 Y shift, X shift and cursor shift. Unless it has previously been allocated by the system software for some other function, the control is selected for a shift function simply by operating the appropriate push button, eg pressing the ◄► push button provides the X shift facility. Similarly, pressing the CH1 or CH2 ▲▼ push button allows it to be used for Y shift on that channel, and the SELECTED CURSORS push buttons allow it to be used for moving a particular cursor along in associated trace.

The allocation of the SHIFT control for a particular purpose is indicated by the illumination of the associated green indicator light. The deselection of the control is achieved either by operating the push button a second time (they are a non-locking press on, press off type), or when it is selected for another purpose.

3.8 CURSORS

Four cursors, C1 to C4, are available on the display for voltage and time measurement purposes and appear as brightened spots, or sections, on the trace. Measurements are made at the leading (ie left hand) edge of a cursor.

Cursors are selected individually by operating the SELECTED CURSORS push buttons, and their presence is indicated by the illumination of the associated indicator light situated above the push button. A cursor may be removed from the display by operating the blue (S) push button on the keypad and its SELECTED CURSORS push button in sequence. It is restored to the display simply by pressing its push button a second time which would also result in it being attached to the SHIFT control (section 3.7).

The current cursor referred to in the alphanumeric data appearing on the display is that cursor attached to the SHIFT control (section 3.7) or the last cursor selected. Unless a calculation is being performed (section 3.15), current cursor time and voltage information is displayed on line 15 of a mixed display. Cursors associated with store traces always flash. Real time trace cursors can also be caused to flash by holding their SELECTED CURSORS push button pressed (this is useful for identifying a particular cursor when there is more than one appearing on the display).

The allocation of cursors to channels (CH1 and CH2), timebases (A and B) and stores (ST1 and ST2) follows a set of rules and priorities.

(a) In general, cursors are allocated to channels in the order C1 and C2 to CH1, and C3 and C4 to CH2.

(b) Similarly, the general rule for the allocation to timebases is that C1 and C3 appear on timebase A, and C2 and C4 on timebase B.

(c) If only one channel is selected, all four cursors are allocated to that channel.

(d) If only timebase A is selected, all four cursors appear on that timebase.

(e) If only timebase B is selected, only C2 and C4 appear on the display. C1 and C3 cannot be made to appear on timebase B.

(f) If the contents of either store (ST1 or ST2) are displayed, then C1 and C3 are allocated to that store and are removed from whatever real time trace they may have been previously allocated to. Cursors C2 and C4 remain allocated to their associated real time traces.

(g) If the contents of both ST1 and ST2 are displayed, then C1 and C2 are allocated to ST1, and C3 and C4 to ST2. No cursors then appear on any real time trace on the display.

3.9 MODE/MENU CONTROL KEYPAD

The fourteen MODE/MENU CONTROL push buttons are allocated as follows:

(a) Ten push buttons, coded 0 to 9, are used for inputting numeric data as instructed by the menu pages. Two of the push buttons (1 and 0) also serve for inputting "yes" (Y) and "no" (N).

(b) The blue S, or second function, push button has no direct effect on its own, but modifies the function of the next push button to be operated. If this is one of the ten numeric push

buttons mentioned above, then it takes on the function referred to in the annotation above it, eg by pressing S7 the HOR (horizontal) menu page is displayed. As discussed previously (sections 3.3 and 3.8) the S push button is also used in conjunction with the appropriate shift push button for deselecting a channel or a cursor.

(c) The Q, or quit, push button provides an abort facility in that it takes the display down one level of information. In this respect, examining a trace is considered as the lowest level. In effect, pressing Q stops the operation in process and restores the display to the previous state.

(d) The [ ] push button can be dedicated to a particular function by a menu and is indicated as such on the display. Otherwise (in the default condition) it may be used for stepping pages within a menu in a continuous manner. All menus consist of at least two pages and always return to page 1 after the final page. This button is also used when viewing a mixed display for reading a menu page (see para. 6 in section 3.10.2).

(e) The D, or dual option, push button allows instant switching between two pre-selected options for a particular mode while setting up another mode (section 3.17).

NOTE: Wherever it appears in this section or on the displayed menu pages, the instruction "key" followed by one or two alphanumerics implies that those keypad push buttons are to be operated sequentially.

NOTE: If at any time an invalid code is keyed in, a statement to that effect, together with an explanation if applicable, appears on the display between two rows of asterisks.

3.10 WARM START

As stated in section 3.1, the 5110 normally starts up in the operational mode that it was in when switched off. Therefore, the alphanumeric display obtained after the initial 15 seconds warm-up period consists of page 1 of Current Control Settings (Fig. 3.3). This, together with the subsequent page 2 (obtained by keying 30 or [ ]), details the software-controlled operational modes. The timebase speed, and the Y amplifier sensitivities are, of course, controlled manually by the rotary switches (sections 3.3 and 3.4).

However, for the purposes of operator instruction we will start by considering the General Mode Index page (fig. 3.2). This is obtained after the appearance of the Current Control Settings page 1 by keying 00, or at any time by keying S6.

3.10.1 GENERAL MODE INDEX

Having obtained the General Mode Index, any of the seven pages listed can be obtained simply by keying the appropriate option number. Alternatively, the [ ] push button may be used for stepping through the pages consecutively.

(a) Key 10 to obtain general operating information and advice.

(b) Key 20 and 30 for Current Control Settings data. In addition to detailing the current settings, these pages also list the key selections for obtaining the Horizontal Mode menu (key S7), the Vertical Mode menu (key S8), the Memory Mode menu (key S5), the Trigger Mode menu (key S9) and the Calculation Mode menu (key S4).

(c) Key 40 for Default Control Setting data. These are the control settings that would exist in the absence of any alternative stored settings. As in the case of Current Control Settings, key selections are listed for obtaining the relevant menus.

(d) Key 50 for the Software Calibration menu.

(e) Key 60 for the Dual Option menu.

(f) Key 70 for the Self Test menu.

(g) Key 80 for the Measurement/Calibration menu.

3.10.2 OBTAINING A TRACE

1. Press the Q push button. The selected trace(s) should appear together with the relevant control setting data (Fig. 3.1). This is referred to as a mixed display.
2. If necessary, operate the TRACE LOCATE push button and adjust the X and Y shift settings (section 3.7) to centralise the horizontal trace (timebase triggered) or spot (timebase not triggered, or X-Y selected for the horizontal mode).

   Active TRACE LOCATE is selected by operating the trace location button at the same time operating the channel ▲▼ button. The cursor on the trace is set to the centre line automatically correcting the values on the screen.
3. Adjust the TRACE (outer) INTENSITY control to obtain a clear display.
4. If both A and B timebases are being displayed, adjust TRACE SEP to separate them.
5. If the A intensified by B or A and B alternate horizontal mode has been selected, adjust CONTRAST to obtain a suitable contrast between the A timebase and the brightened part of that timebase.
6. If required, hold the [ ] push button depressed to read the menu page used immediately prior to pressing Q. Part of the data accompanying the

trace is a line detailing this menu (Fig. 3.1).

7. If required, pull the DATA INTENSITY knob outwards to remove the alphanumeric data from the mixed display.

3.11 HORIZONTAL MODE SETTING

1. Key S7 to obtain the Horizontal Mode menu page 1.
2. The current selection will be shown on the right and there are five possible options.
   (a) A timebase only (key 01).
   (b) A timebase intensified by B (key 02). In this case no B timebase appears, but that part of the A timebase selected for eventual display on the B trace is brightened. Initially, the B TIME/CM switch should be set 2 or 3 ranges faster than the A TIME/CM switch.
   (c) B timebase only (key 03).
   (d) A and B alternate (key 04). This mode provides simultaneous display of the A intensified by B and the B traces by switching the beam between the A and B timebase signals on alternate timebase cycles.
   (e) X-Y mode (key 05). The selection of this mode disables the timebase and the X deflection is derived from the selected A trigger signal. (Refer to section 3.20).
3. Key 06 to switch the B1 facility on or off. With this switched on the start of the B sweep is modified by the setting of the cursor C1.
4. Key 07 to switch the B3 facility on or off. With this switched on the start of the B sweep is modified by the setting of the cursor C3.

NOTE: Options 06 and 07 are available only in certain trigger modes (see section 3.13.2). If the appropriate trigger mode has not been selected then the legend "B SWEEP NOT MODIFIED BY CURSOR" appears on the Horizontal Mode menu page 1 instead of options 06 and 07.

5. Key 10 or [ ] to obtain the next page of the menu.
6. Key 11 to switch the x10 expansion on or off. This option is not operative when the X-Y mode is selected.
7. Key 12 to switch the X tracks cursor facility on or off. This is available only when the x10 expansion is switched on. When shifting a cursor along an expanded trace it causes the trace to move at the same rate and in the opposite direction as the cursor so that the cursor remains in the same position on the display. This overcomes the difficulty normally encountered in positioning a cursor at a particular point on an expanded trace.
8. After pressing the Q push button to obtain the mixed display (section 3.10.2), further amendments can be made to the horizontal mode if required by keying in the options discussed above.

3.12 VERTICAL MODE SETTING

1. Key S8 to obtain the Vertical Mode menu page 1.
2. The current selection will be shown on the right and there are six possible options.
   (a) CH1 only (key 01).
   (b) CH2 only (key 02).
   (c) Dual auto (key 03). This enables CH1 and CH2 signals to be displayed simultaneously, with the instrument software making the selection between the chop or alternate modes of beam switching. In order to force the instrument into either the chop or alternate modes of dual display then either option 04 or 05 should be selected.
   (d) Dual display with the chop mode of beam switching (key 04). This should be selected if the timebase speed is slower than about 1ms/cm.
   (e) Dual Display with the alternate mode of beam switching (key 05). This should be selected if the timebase speed is faster than about 1ms/cm.
   (f) Add CH1 and CH2 (key 06). This enables the CH1 and CH2 signals to be added algebraically onto a single trace. Waveform subtraction can be achieved by means of invert options 07 and 08.
3. Key 07 to switch the invert CH1 facility on or off.
4. Key 08 to switch the invert CH2 facility on or off.
5. Key 09 to switch the trigger view facility on or off. Whatever vertical mode has been selected, switching this on will produce another trace showing the signal in the A trigger amplifier. This facility, however, is automatically disabled if composite trigger (section 3.5) has been selected, and the display of trigger view only (ie no other Y signals displayed) is not possible. The trigger view trace has three main functions.
   (a) It gives a guide to trigger level. When viewing CH1 or CH2, the sensitivity of the trigger view display is approximately that which is selected on the Y channel VOLTS/CM switch.
   (b) It enables the effectiveness of the LF REJ and HF REJ filters to be observed.
   (c) It enables a third Y channel to be available via the EXT A input socket when EXT trigger source is selected. In this case the sensitivity is approximately 50mV/cm (500mV/cm with EXT÷10 selected).
6. Key 10 or [ ] to obtain the next page of the menu.

7. Key 11 to indicate whether or not a x10 probe is being used on the CH1 input. This will cause all measurements to be scaled accordingly.
8. Key 12 to indicate whether or not a x10 probe is being used on the CH2 input. This will cause all measurements to be scaled accordingly.
9. After pressing the Q push button to obtain the mixed display (section 3.10.2), further amendments can be made to the vertical mode if required by keying in the options discussed above.

3.13 TRIGGER MODE SETTING

Trigger selection is a more detailed procedure than horizontal and vertical selection (sections 3.11 and 3.12) in that in addition to the Trigger Mode menu page (key 00), there is a Qualification menu page (key 10), and three Delay System menu pages (key 20, 30, 40).

Two front panel indicator lights are associated with the trigger circuits.

(a) TRIG'D. This lights to indicate that a trigger waveform is present at the A trigger amplifier, and therefore that the timebase is being triggered. This will be found useful when examining complex waveforms in that it will confirm that correct triggering is taking place.

(b) ARMED. This lights in the single shot mode (option 03) to indicate that the timebase is ready to be triggered.

3.13.1 MODE SELECTION

1. Key S9 to obtain the Trigger Mode menu.
2. The current selection will be shown on the right and there are four possible options.

(a) Normal (key 01). In this mode the trace will blank in the absence of a trigger signal.

(b) Auto (key 02). In this mode the timebase will free-run and display a bright line or unsynchronised display in the absence of a correct trigger signal. This helps in finding the trace initially. When the TRIGGER LEVEL control is adjusted and/or the amplitude of the trigger signal is increased to obtain effective triggering, the timebase will revert automatically to normal triggering as in (a) above. The auto mode is useful for wideband signals above 40Hz, but operation below this frequency may cause mis-triggering since the timebase can revert periodically to its free-run state.

(c) Single shot (key 03). In this mode the [ ] push button is dedicated to the timebase arming function, as indicated by the legend [ARM] on the menu page. Once the timebase has been armed by pressing the [ ] push button, indicated by the illumination of the ARMED light, the timebase operates and provides a single sweep only upon receipt of the next trigger signal. To initiate further sweeps it is necessary to re-arm the timebase by pressing the [ ] push button again.

(d) Single shot manual (key 04). In this mode the [ ] push button is dedicated to the timebase triggering function, as indicated by the legend [TRIG] on the menu page. The timebase operates and provides a single sweep every time the [ ] button is pressed.

3.13.2 MODE QUALIFICATION

1. Having made the preliminary mode selection (section 3.13.1), key 10 to obtain the Qualification menu. This provides two options for the start of timebase A (options 11 and 12) and seven options for the start of timebase B (options 13 to 19).
2. Select the start of timebase A:

(a) Key 11 for the sweep to be started by the A trigger source.

(b) Key 12 for the sweep to be started by the delay system. In this case it will be necessary to carry out a selection on the Delay System menu – refer to section 3.13.3.

NOTE: The delay system cannot be used for starting timebase A if it has already been selected for timebase B (options 15, 16, 19), and vice versa.

3. Select the start of timebase B:

(a) Key 13 for the sweep to be started by the appropriate cursor (see section 3.8).

(b) Key 14 for the sweep to be started by the first B trigger signal occuring after the appropriate cursor.

(c) Key 15 for the sweep to be started by the delay system.

(d) Key 16 for the sweep to be started by the first B trigger signal occuring after a delay controlled by the delay system.

(e) Key 17 for the sweep to be started by the B trigger source.

(f) Key 18 for the sweep start to be coincident with the A sweep start.

(g) Key 19 for the sweep to be started by the appropriate cursor after a delay controlled by the delay system.

NOTE: In the case of options 15, 16 and 19 it will be

necessary to carry out a selection on the Delay System menu -- refer to section 3.13.3.

3.13.3 DELAY SYSTEM

1. If the delay system is to be applied to timebase A (ie option 12 selected), key 20 to obtain the first page of the Delay System menu. There are two possible methods for defining the A sweep delay, either "A START DELAYED FROM A TRIGGER" to a particular time or event, or "A STARTS" after a particular number of events or period of time.
   (a) Key 21 for the sweep to start time T after the A trigger.
   (b) Key 22 for the sweep to start on the Nth B trigger after the A trigger.
   (c) Key 23 for the sweep to start on every Nth A trigger (÷N mode).
   (d) Key 24 for the sweep to start every Nx10ns. In this case the sweep is no longer synchronised to the A trigger, but instead is in effect triggered from a free running internal timer/counter.

NOTE: For each of the above options it will be necessary to define a further parameter, either time T or integer N. Refer to para. 5 below.

2. If the delay system is to be applied to timebase B (ie option 15, 16 or 19), key 30 to obtain the second page of the Delay System menu. The delay period is defined by specifying the start, for which there are six options (31 to 36), and the end, for which there are three options (37, 38, 39).
3. Specify the delay period start time:
   (a) Key 31 for the start of the A sweep.
   (b) Key 32 for the B trigger.
   (c) Key 33 for the appropriate cursor.
   (d) Key 34 for the first B trigger signal occuring after the appropriate cursor.
   (e) Key 35 for the A trigger.
   (f) Key 36 for the first A trigger signal occuring after the appropriate cursor.

NOTE: If either option 16 or 19 was selected in section 3.13.2, then options 31 and 33 only are available for specifying the delay period start time.

4. Specify the delay period end time:
   (a) Key 37 for time T.
   (b) Key 38 for the Nth B trigger signal.
   (c) Key 39 for the next event in the Nth B trigger sequence (÷N mode). In this case the start time (options 31 to 36) is irrelevant, the B sweep starts on or after every Nth B trigger.

NOTE: As in the case of the A timebase, for each of the above three options it will be necessary to define a further parameter, either time T or integer N. Refer to para. 5 below.

5. Key 40 to obtain the final page of the Delay System menu. This shows the current selection of T (time), N (events) and S (increment/decrement steps). It will be seen from this page that further options (44 to 47) are available for modifying T or N while observing the trace.

NOTE: When specifying T, N and S in options 41, 42 and 43, the [ ] push button has a "cancel last entry" function. With each of these options, having specified the value and units, the question "IS THIS TRUE VALUE Y/N?" appears at the foot of the menu page. This must be answered by keying (Y), in which case the specified value appears as the current selection, or (N), in which case the value keyed in is deleted and a new value can be specified.

6. To specify a time value for T, key 41. Use the numeric push buttons to specify the quantity, keying SQ for decimal point if required, followed by the units: S0 for seconds, S1 for milliseconds, S2 for microseconds or S3 for nanoseconds.
7. To specify an event number for N, key 42. Use the numeric push buttons to specify a whole number quantity followed by S0 for units.
8. Option 44 allows incremental (keying 1) or decremental (keying 0) stepping of T, or N, while observing the trace(s). The size of the steps is determined by the step value S. To specify S, key 43. If the current selection is "TIME", then S is specified as a time as in the case of T, but if the current selection is "EVENTS", then S is specified as a whole number as in the case of N.
9. Option 46 allows T, or N, to be incremented or decremented by means of the SHIFT control while observing the trace(s), the rate being dependent on the value of S, ie a high value produces a coarse control and a low value a fine control.
10. Options 45 and 47 can be used only with options 23, 24 and 39 (ie where the end of the delay is dependent on N), and provide a means of moving to a point of interest on a waveform by incrementing or decrementing the value of N for one sweep. If N is a low value, Key 45 and use the 1 and 0 push buttons (as in the case of option 44), but if N is large, key 47 and use the SHIFT control.
11. Holding the 1 or 0 key for a time brings the auto keyboard repeat function into operation which after adding continuously increments or decrements, the daley value by the preset steps. The operation stops immediately the appropriate key is released.

3.14 MEMORY MODE SETTING

1. Key S5 to obtain the Memory Mode menu.
2. Key 01 to switch on or off the display of ST1 contents.
3. Key 02 to switch on or off the display of ST2 contents.
4. Press the Q push button to display the trace(s). Alphanumeric data relevant to the stored waveforms at the time of their capture will appear on the display.

3.14.1 CAPTURE SELECTION

There are two methods of capturing and storing a waveform – realtime and repetitive.

In the case of real time capture, as the incoming waveform arrives at the instrument, voltage samples are taken at regular intervals and placed in store. Thus it is possible to capture a transient waveform or a one-shot event. The pre-trigger option (see para. 6 below) makes it possible to also capture events prior to the waveform trigger.

At high sweep rates, however, it is not possible to capture a waveform in this manner. Instead, one voltage sample only is taken on each sweep with the sample point moving with respect to the trigger point between sweeps. This is known as repetitive capture and extends the capture range to 100MHz, but it is not possible to capture transient events.

1. Key 10 to obtain the first page of Capture menu. This and the subsequent page (key 20) detail the options for selecting the waveform to be captured, where it is to be stored, and how it is to be captured.
2. Select the source.
   (a) CH1 (key 11).
   (b) CH2 (key 12).
   (c) Dual (key 13).
3. Select the sweep to be captured.
   (a) A sweep (key 14).
   (b) B/B1 sweep (key 15). As B and B1 are mutually exclusive there can be no confusion.
   (c) B3 sweep (key 16).

NOTE: In the event of an invalid selection being made (eg attempting to select CH2 for capture when CH1 has been selected for the vertical mode setting), an asterisk will appear alongside the current selection.

4. Select the destination store.
   (a) ST1 (key 17).
   (b) ST2 (key 18).
5. Key 20 to obtain the second page of the Capture menu. If the timebase range of the waveform to be captured is within the limits 50μs/cm, it is possible to select either repetitive capture (key 21), or real-time capture (key 22) with reduced resolution. No operator choice is available outside this timebase range, the internal software makes the appropriate choice.
6. If real-time capture has been selected (either by the operator or by the software) it is possible for either 0% (key 23) or 50% (key 24) of the captured waveform to be pre-trigger. However, this facility is available on the A sweep only.
7. The input signal can be averaged to reduce noise. In realtime capture, the number of sweeps can be defined with the resultant average displayed. In 'repetitive' capture, each point can be progressively captured over a preset number of sweeps, displaying the resultant average. To set the number of captures to be averaged (key 25). The displayed number of averages will flash to indicate it is ready to be changed. The number of averages is incremented in powers of 2 by keying 1 and decremented by keying 0, e.g. 0, 2, 4, 8 . . . . 256. The maximum number is 256. Press Q to return to the menu.
8. Key 19 to return to a mixed display and then press the [ ] push button to start the capture.

3.14.2 PLOTTER SELECTION

Key 30 and 40 to obtain pages 1 and 2 respectively of the Plotter menu.

The purpose of the plotter output facility is to provide a hardcopy printout on X-Y or T-Y type plotters of the contents of ST1 and ST2. The single output can be assigned to either Store 1 or Store 2 by keying 81 or 32. The output rate can be set in the range 50sec/div to 10ms/div. by keying 37 and inputting the desired rate via the key pad. Keying 38 starts the output, the X ramp being synchronised to the selected plot rate. The plot can be aborted at any time by keying 39.

To assist in setting the correct operating range for the recorder, the full scale outputs for X (1.024V), +Y (+400mV) and –Y (–400mV) can be set. Note the display centre line corresponds to 0V output. The warning bell to indicate the finish of a plot cycle is available by keying 45.

3.14.3 MACHINE STATE STORAGE

GENERAL

The machine state is comprised of three sections:–

1. The selections made from all menus.
2. The settings of the manual controls.

   CH1, 2 Volts/cm + UNCAL
   TBA, B Time/cm, + UNCAL
   CH1, 2 AC/DC/GND

3. The contents of store 1 & store 2.

At the simplest level, section 1 is preserved during switch off.

OPERATION OF SS (SAVE SWITCH)

Operating SS (second function RS) instructs the instrument to save the current machine state in one of the eight machine state storage areas. These areas are non-volatile and are referred to by their index number 1 through 8.

The operator will be asked to specify the index number and also whether manual controls are to be included. (see RS paragraph for more details about manual controls Section 1 & 3 will be stored automatically.

Note that only alternate locations of each store are saved enabling a pair of stores to be contained in a 1K byte segment. This is referred to as a machine state store (MSS).

OPERATION OF RS (RECALL STATE)

Operating RS instructs the instrument to change the state of the instrument to match that of the stored one.

Again the operator must supply the index number.

Section 1 & 3 are recalled without the intervention of the operator. When section 2 is recalled, the operator will be prompted to adjust the manual controls as appropriate. As this procedure can be lengthy, the operator is given the choice of saving the machine state without section 2. The operator can press Q (Quit) to avoid having to change the manual control.

NOTES:

a) The calibration of the instrument is NOT affected by machine state save/recall.

b) One fixed machine state is included, index number 0, which will 'normalise' the instrument to the settings shown on General Mode option 40 and has the same effect as operating General Mode option 41 with less key presses. Note that machine state zero (MS0) contains only section 1.

3.15 CALCULATION MODE SETTING

To carry out time and voltage measurements, key S4 to obtain the Calculation Mode index page. This mode provides a selection of options to enable a variety of accurate time and voltage measurements and event counts to be made in conjunction with the cursors (section 3.8). The result of any measurements appears on line 15 of a mixed display (Fig. 3.1).

All measurements are made at the leading (ie left hand) edge of a cursor and are taken with respect to ground (0V) and the start of the A or B timebase as appropriate. The displayed values only may be modified as described in the following paragraphs. Current cursor calculations take place when no other specific calculations are requested (section 3.15.3).

3.15.1 X PARAMETER MEASUREMENT

The measurement taken at a cursor has two parameters: voltage and time (or events). The latter is referred to as the X parameter, being measurement along the X-axis of the display.

1. Key 10 for the first page of the menu. Either time or the number of B trigger events can be measured up to a particular cursor.
   (a) Auto-time (key 11). This uses either the sweep ramp waveform to make an analogue measurement which is converted to a 3-digit time readout, or alternatively uses the internal timer/counter if it has not been allocated for any other purpose. If the timer is being used for the measurement, then the legend X appears on line 15 of the mixed display.
   (b) Xtal-time (key 12). This uses the internal timer/counter to give a digit time readout accompanied by the legend X on line 15.
   (c) B trigger events (key 13). This also uses the internal timer/counter to give an events count readout of up to 9 digits accompanied by the legend E on line 15.

NOTE: Options 12 and 13 are not available if the internal timer/counter has already been allocated for any other purpose.

2. The X parameter measurement is assumed to start from the start of timebase A. However, if the cursor in question is on a B sweep, the horizontal datum can be specified if required. Key 30 for the third page of the menu:
   (a) Datum = A start (key 34).
   (b) Datum = B start (key 35).
   (c) Datum = auto (key 36). In this case the datum is the start of timebase A if it is viewed, otherwise it is the start of timebase B.

NOTE: The legend A or B appears on line 15 to indicate the horizontal datum (Fig. 3.1).

3.15.2 USER DATUM SELECTION

The instrument internal datum for any measurement is zero (volts, time or events). If required the operator may set in his own datum in which case the legend U appears on line 15 of the mixed display.

1. Key 20 to obtain the second page of the menu. This shows the current user datum selections for the four cursors.
2. Key 21 to switch the user datums on or off. When switched on, the legend "(TIME)" or "(EVENTS)" appears on this line of the menu to indicate which was selected for the X parameter measurement (section 3.15.1).

NOTE: When specifying voltage, time and events in options 22, 23 and 24, the [ ] push button has a "cancel last entry" function. With each of these options, having specified the value and units, the question "IS THIS TRUE VALUE Y/N?" appears at the foot of the menu page. This must be answered by keying (Y),

in which case the specified value appears as the current selection, or (N), in which case the value keyed in is deleted and a new value can be specified.

3. To specify a user datum for voltage, key 22. The legend "CURSOR 1, 2, 3, 4" must be answered by keying in one cursor number. Use the numeric push buttons to specify the voltage, keying SQ for decimal point if required, followed by S0 for volts or S1 for millivolts.

4. To specify a user datum for time, key 23. The legend 'CURSOR 1, 2, 3, 4" must be answered by keying in one cursor number. Use the numeric push buttons to specify the time, keying SQ for decimal point if required, followed by the units: S0 for seconds, S1 for milliseconds, S2 for microseconds or S3 for nanoseconds.

5. To specify a user datum for events, key 24. The legend "CURSOR 1, 2, 3, 4" must be answered by keying in one cursor number. Use the numeric push buttons to specify a whole number quantity followed by S0 for units.

An alternative method of specifying user datums is by transferring from the current cursor's true value (ie not the displayed value if user datums are in effect).

1. Key 30 to obtain the third page of the menu.
2. (a) Key 31 if it is required to set a user datum for voltage only.
   (b) Key 32 if it is required to set a user datum for time or events, depending on which was selected for the X parameter measurement (section 3.15.1).
   (c) Key 33 if it is required to set a user datum for voltage and time or events.
3. Keying 31, 32 or 33 produces a mixed display and gives the [ ] push button an "execute" function. Set the current cursor to the required position on the waveform and press the [ ] push button. The current cursor setting will now appear on the second page of the menu (key 20) as the current user datum selection (voltage and/or time or events). However, the current cursor setting(s) appearing on line 15 of the mixed display will be zero only if user datums have been switched on (key 21).

3.15.3 CALCULATIONS

1. Key 40 to obtain page 1 of the Calculation menu. Seven calculation options are available, 41 to 47, which enable the cursors to be used for carrying out time or event and voltage calculations.
2. Keying any of the seven options will produce a mixed display with the instruction "specify cursors" (except for option 44 when all four cursors are used). Specify the cursor(s) by means of the numeric push buttons on the keypad. The calculation will then proceed, with the result displayed on line 15.
   (a) Voltage and time between cursors is automatically calculated by (Key 41) and specifying the appropriate cursor. Measurements can be made in Voltage from trace to trace but it is limited to one sweep in time.
   (b) Rise or fall time and overshoot (key 42). With this option, one cursor defines the 0% level and the other cursor the 100% level of a step waveform. Rise or fall time is measured between the 10% and 90% levels, and the maximum overshoot (positive or negative) is measured as a % swing.
   (c) Voltage and time at 50% point (key 43). As with option 42, the specified cursors define the 0% and 100% levels of a step waveform, and the voltage and time at the 50% level is measured.
   (d) Period between two at the 50% points (key 44). With this option the duration of a pulse waveform at its 50% amplitude points is measured e.g. C1 defines the initial 0% level, the 100% level is found automatically (allowing for droop on the top of the pulse, if necessary) and C3 the final 0% level.
   (e) Maximum positive-going voltage swing between two specified cursors (key 45).
   (f) Maximum negative-going voltage swing between two specified cursors (key 46).
   (g) Peak-to-peak voltage between the maximum positive-going and negative-going voltage swings between two specified cursors (key 47).
3. Selecting the SHIFT control for any purpose (section 3.7) while in the Calculation Mode will suspend the calculation in progress. The current calculation result will appear on line 2 of the mixed display and current cursor details on line 15. The calculation will resume immediately the SHIFT control is deselected.
4. Press the Q push button in order to exit from the current calculation routine.
5. Calculations are suspended while repositioning cursors.

3.16 SOFTWARE CALIBRATION

The basic analogue accuracy of the 5110 is ±3%. For cursor-based measurement purposes this accuracy can be improved by calibrating the instrument against known standards. This is known as software calibration and the options available are listed in the Software Calibration menu (key S6, 50). The known standard for time is the instrument's own internal crystal-controlled timer/counter. Vertical calibration, however, requires the use of an external power supply and an accurate digital voltmeter, or an oscilloscope calibrator.

3.16.1 HORIZONTAL CALIBRATION

Options 51 and 52 enable the calibration of the A and B timebases respectively. The procedure in each case is identical.

1. Key 51, or 52, and follow the instruction "SELECT 0.1ms/DIV" by setting the appropriate TIME/CM switch to 0.1ms/cm.
2. The legend "SELECT NEXT RANGE" indicates that software calibration on that particular range has been completed satisfactorily. Set the switch to its next position (either up or down).
3. Repeat this procedure for all of the required (or all 22) positions of the TIME/CM switch. In the event of the legend "OUTSIDE S/W CALIBRATION RANGE RETRY YES/NO?" appearing instead of "SELECT NEXT RANGE", keying (Y) will cause the software to attempt to recalibrate, while keying (N) will cause it to abort the attempt.
4. Press the Q push button in order to exit from the current calibration routine.

3.16.2 VERTICAL CALIBRATION

Options 53 to 56 enable the calibration of the CH1 and CH2 amplifiers with and without a x10 probe. These procedures are more complicated than the horizontal calibration (section 3.16.1) in that they required the use of an external floating power supply and a digital voltmeter (Fig. 3.5) or an oscilloscope calibrator (eg Bradley Type 192).

NOTE: When using an external power supply and DVM, it must be possible to change over the polarity of the input without affecting the DVM reading.

1. (a) Key 53 to calibrate CH1 from a x10 probe.
   (b) Key 54 to calibrate CH2 from a x10 probe.
   (c) Key 55 to calibrate CH1 from its BNC input.
   (d) Key 56 to calibrate CH2 from its BNC input.

NOTE: Only three ranges are checked with options 53 and 54, but all ranges are checked with options 55 and 56.

2. The appearance of the legend "NOT YET WARM CONTINUE YES/NO?" indicates that the instrument has not been switched on for its full 20-minute warm up period. In this event, keying (Y) will cause the software to proceed with the vertical calibration, while keying (N) will cause it to abort.
3. Follow the instructions as they appear on the mixed display. These will give details of the range to be selected.
4. The procedure for using an external power supply and DVM is as follows.
   (a) Supply the input voltage requested to within 10%.
   (b) Answer question "IS THIS TRUE VALUE YES/NO?" by keying (Y) if the DVM indicates that the input voltage is absolutely correct, or (N) if it is not. In the latter case use the numeric push buttons to specify the voltage read on the DVM, keying SQ for decimal point if required followed by the units: S0 for volts or S1 for millivolts.
   (c) Answer question "IS THIS TRUE VALUE YES/NO?" by keying (Y).
   (d) Operate the changeover switch (Fig. 3.5) when instructed to "REVERSE POLARITY OF INPUT".
   (e) Press the [ ] push button to continue with the next value of input voltage. Instructions will be given when to change range.
5. When using an oscilloscope calibrator, the exact input voltages requested can obviously be used and the question "IS THIS TRUE VALUE YES/NO?" always answered by keying (Y). The vertical calibration program has been arranged with the Bradley Type 192 in mind in order to minimise the number of operator steps. This is illustrated by the following example detailing the procedure when calibrating the 2mV/DIV and 5mV/DIV ranges.
   (a) The first input voltage requested for the 2mV/CM range is +6mV. This is obtained by setting the calibrator controls to 2mV/DIV and 3 divisions (2 x 3 = 6mV).
   (b) Answer "IS THIS TRUE VALUE YES/NO?" by keying (Y).
   (c) Reverse the polarity to - on the calibrator when instructed to "REVERSE POLARITY OF INPUT".
   (d) Press the [ ] push button to continue.
   (e) The next input voltage requested is -15mV. This is obtained simply by setting the calibrator to the next range (5mV/DIV) and leaving the divisions control on 3 (5 x 3 = 15mV).
   (f) Answer "IS THIS TRUE VALUE YES/NO?" by keying (Y).
   (g) Reverse the polarity to + on the calibrator when instructed to "REVERSE POLARITY OF INPUT"
   (h) Press the [ ] push button to continue.
   (i) When instructed to do so, switch the 5110 to the 5mV/CM range. Since the first input voltage requested for this range will be +15mV, it will be seen that the entry conditions are exactly as required for that range.
6. Press the Q push button in order to exit from the current calibration routine.

3.17 DUAL OPTION SELECTION

It is often desirable while selecting a particular mode option (say, in the Trigger Mode) to be able to switch quickly between two alternative options of one of the other modes (say, of the Horizontal Mode). This facility is provided by the D push button which may be used for switching between the selections 1 and 2 appearing on the Dual Option menu. This menu may be viewed by selecting 60 from the General Mode Index (key S6). Alternatively it may be viewed at any time by keying SD, and the display then returned to the current display by keying Q with no changes made.

When making selections on the dual option menu the question "PRESERVES CURRENT DISPLAY Y/N?" must be answered "yes" (Y) or "no" (N) before being able to proceed.

(a) If the question is answered "no". Whenever the D push button is pressed in order to switch between the dual selections, the display will always switch to the page associated with that selection.

(b) If the question is answered "yes". It is possible to use the D push button while viewing another menu and have that menu remain on display while the dual mode selection is switched from one to the other.

1. Select the first of the required alternative options (eg for horizontal mode A timebase only, key S7, 01).
2. Key SD to obtain the Dual Option menu.
3. Answer the question "UPDATE SELECTION 1, 2 or both?" by keying 1.
4. Answer the question "PRESERVES CURRENT DISPLAY Y/N?" by keying (Y) or (N) as required (see above).
5. After a brief pause the display will revert to the menu from which the alternative selections are being made (in this example the Horizontal Mode menu). (Press Q to terminate the pause).
6. Select the second of the required alternative options (eg for horizontal mode A alternate B timebase, key 04).
7. Key SD to obtain the Dual Option menu again.
8. Answer the question "UPDATE SELECTION 1, 2 or both?" by keying 2.
9. Answer the question "PRESERVES CURRENT DISPLAY Y/N?" by keying (Y) or (N) as required (see above).
10. Once again, after a brief pause the display will revert to the menu from which the alternative selections are being made.
11. Either, or both, of the alternative options can be amended at any time by following a similar procedure.

In the above example, it is now possible while making a selection in another mode, to switch the horizontal mode from option 01 to 04 and back to 01 simply by the sequential operation of the D push button.

If both are set to 19 in memory mode for example, each time the D push-button is selected, the 5110 will arm ready for capture.

3.18 SELF TEST

Key S6, 70 to obtain the Self Test menu.

No information on this menu is available at present.

3.19 MAINTENANCE/CALIBRATION

Key S6, 80 to obtain the Maintenance /Calibration menu.

No information on this menu is available at present, but it is intended that it will provide information for the maintenance technician on the repair and calibration of the instrument. The calibration procedures will be additional to the software calibration discussed in section 3.16.

3.20 X-Y MODES

The selection of the X-Y mode (option 05 of the Horizontal Mode - section 3.11) disables the timebase and the X deflection is derived from the selected A trigger signal. The x10 expansion on/off facility (option 11 of the Horizontal Mode - section 3.11) is inoperative in this mode.

3.20.1 EXTERNAL X FUNCTION

External X operation is achieved by the selection of EXT trigger (section 3.5) while applying the signal to the EXT A input socket. The deflection sensitivity will be approximately 50mV/cm (500mV/cm with EXT 10 selected. The COUPLING locking push buttons (section 3.5) can be used as required.

This external X deflection can be displayed as a single trace display against the CH1 or CH2 input, or thier sum or difference (options 01, 02, 06 respectively of the Vertical Mode - section 3.12). Alternatively, a dual trace display of both the CH1 and CH2 inputs against the X signal is obtained by selecting the chop mode dual display (option 05) is not available in X-Y display.

3.20.2 X-Y FUNCTION

The full flexibility of the two Y input channels can be utilised for a single trace X-Y display by the selection of CH2 as the A TRIGGER SOURCE and CH1 as the vertical mode (option 01). It is recommended that DC trigger coupling is selected without the use of the LF REJ or HF REJ filters. AC coupling of the trigger signal is best achieved by the relevant Y channel (CH2)

input coupling switch (section 3.3). In this mode X shift is achieved by selecting horizontal (◄►) shift, and the relevant (CH2) vertical shift (▲ ▼) facility is inoperative.

3.20.3 Y LINE FUNCTION

By using the instrument in the X-Y mode and selecting LINE trigger source, a display of Y versus mains frequency may be obtained.

3.21 ADDITIONAL FACILITIES

3.21.1 USE OF PASSIVE PROBE

A x10 passive probe may be used to extend the voltage range and increase the input impedance of the Y amplifiers. The input impedance of the instrument is 1MΩ shunted by 22pF. The effective capacitance of the input lead must be added to this and the resultant impedance will sometimes load the signal source. The probe will reduce this to approximately 10pF and increase the resistive element of the impendance to 10MΩ. To obtain a flat frequency response it is necessary to adjust the probe capacitance to match the capacitance of the instrument. The PB18 is designed specifically to work with the 5110.

1. Set the associated VOLTS/CM switch to 20mV/cm and the A TIME/CM switch to 0.2ms/cm.
2. Connect the probe to the 1V CAL pin.
3. Use a small screwdriver to adjust the capacitor to the probe tip or termination for a square response with no overshoot or undershoot.

3.21.2 CAL OUTPUT

The 1V CAL pin provides a positive-going square waveform of 1V±1% peak-to-peak at approximately 1kHz. Shorting this pin to ground will give a square current waveform of 1mA in the shorting link for current probe calibration.

The TIME CAL pin provides a pulse train output derived from an internal crystal source.

The output is turned on and off by keying 88 on the General Mode Menu 56. The output rate is set by keying 89 and setting the value in the range 40ns to 344 secs. The timecal output is automatically switched off when the internal clock is required for other functions in the capture and delay modes.

3.21.3 DATA INPUT

External data may be connected to the 5110 via the 25-way D-type front panel connect DATA INPUT. This provides for up to 8-bit parallel data. Also available on the connector are +5V, −5V and 0V power supply lines for driving the PB100. The data word is displayed in Binary or Hex and relates to the information present at the time of the current cursor. The PB100 has the facility to identify separately a trigger word for use in conjunction with the external trigger inputs A or B. Switches are located on the PB100 to identify the trigger word required and have positions logic 0.X (don't care) or logic 1. The threshold can be rtl, ecl or variable. There are also two qualifiers which can be used to expand the trigger word to 10 bits wide. When the current cursor data display coincides with the trigger, the word flashes.

3.21.4 Z MODULATION

A rear panel socket allows dc coupled blanking to be applied to the crt. The trace is blanked by a positive input, negative inputs have no effect. The input impedance is approximately 2kΩ, and the required amplitudes are:

(a) +1V for visible modulation.

(b) +4V for blanking at normal intensity.

3.21.5 REAR PANEL OUTPUTS

In addition to a standard IEEE interface connector, there are five BNC and two 2mm sockets on the rear of the instrument providing the following outputs.

1. A ramp, a 2V positive-going sawtooth waveform from a 50Ω source impedance.
2. B gate, a dc level of approximately +3V going to ground for the duration of the B sweep.
3. Plotter outputs (section 3.14.2) at a nominal 50Ω output impedance:
   (a) For use by a recording oscilloscope on three BNC sockets (X and Y deflection and Z modulation).
   (b) For use by a pen recorder on two BNC sockets (X and Y deflection) with "pen lift" (analagous to Z modulation) on the pair of 2mm sockets.

3.22 COLD START

So far in this section we have assumed a warm start for the 5110. However, in the event of a cold start, which by definition means that no operational modes have been specified, the instrument software will select the default settings for all modes. Therefore, the alphanumeric display obtained shortly after switching on will be the Power Up Report (Fig 3.4).

Pressing the Q push button will then cause the Current Control Settings page 1 to be displayed. The procedures then for selecting the required operational modes are as described previously.

After the initial 20-minute warm-up period the legend

"COMPLETE CALIBRATION REQUIRED
SELF ADJUST DAC Y/N?"

appears on whatever display is being viewed. If it is

answered by keying (Y), then adjustment of the digital-to-analogue converter is carried out automatically and the display is retained. However, if it is answered by keying (N) it will continue to reappear at approximately 5-minute intervals until it is answered "yes".

It must be noted, however, that certain fault conditions affecting the RAM and ROM stores also constitute a cold start. In general terms these can be considered as two types, referred to as fatal errors and non-fatal errors.

3.22.1 FATAL ERRORS

A failure of the software programming memory is indicated by the legend "ROM FAILURE-FATAL ERROR" or "FATAL ERROR - NON VOLATILE RAM FAILS R/W" appearing on the display.

In the event of a fatal error, none of the software-controlled mode options will be available, but the manual Y amplifier, timebase and trigger controls will still function normally thereby allowing the instrument to be used as a simple oscilloscope locked in the dual trace, auto trigger condition. There will be no shift control, no cursors and no text display.

3.22.2 NON-FATAL START-UP ERRORS

There are six possible non-fatal error conditions and if any one or more of these occur they will be listed on the display. None of them, in any combination, are capable of completely disabling the instrument, they simply mean that certain facilities may or may not be available.

(a) Memory store 1 failed read/write test. ST1 cannot be used (section 3.14).

(b) Memory store 2 failed read/write test. ST2 cannot be used (section 3.14).

(c) Cursor store failed read/write test. No cursors are available on the stored displays.

(d) Text store failed read/write test. Some text items may not appear or may be incorrect. Beware of proceeding if this error is known to be present.

(e) Memory corrupted and all defaults used. The warm start stored data has been lost and the software has carried out a conventional cold start. Check the condition of the internal nickel-cadmium back-up battery.

(f) Reselection of stored settings has failed and default settings have been used. One or more of the operational modes cannot be set up as per the warm start stored data and the software has selected defaults instead. This is usually the result of switching the instrument off while it is actioning a menu selection.

Pressing the Q push button will then cause the Current Control Settings page 1 to be displayed.

3.23 IEEE INTERFACE

OVERVIEW

The interface will allow a bus controller to read and/or change the state of the functions operated via menu control (although not necessarily in an identical manner). Additionally access is given to all shifts, attenuator controls, timebase controls, channel source coupling, trace stores and machine states.

Calculations may be initiated on a single shot basis with the 5110 producing a service request when the calculation result is available.

Service Request is used to indicate errors, interaction between controller and a particular function and interaction between controller and operator (see detailed information and possible extensions).

When operating without a bus controller, the instrument is capable of sending and receiving store data and machine state (s) in a way which enables two 5110's to communicate

3.23.1 IEEE MODES

Before operating the 5110 through the IEEE bus, the following selections must be satisfied on the General Menu (56) Page 90:-

(a) When communicating with other equipments on the bus, the primary address must be set by keying 91 (Address available 0–31).

(b) For use with a controller where the communication is both to and from the instrument, the 5110 must be in the addressable mode (key 92).

(c) The 5110 can be operated in the talk only mode or listen only mode set by keying 93 or 94. This will enable data to be transferred between instruments or stored information to be printed. The data to be transmitted is specified and started by keying 95 or Store 1, 96 for Store 2 and 97 for the machine states. The data can be separated by carriage return, line feeds known as blocks. Zero length will give continuous data output.

3.23.2 DEFINITIONS (In accordance with recommendation of BS6146/IEC 625–2)

A STRING

Is the smallest complete message unit e.g: VS1=3.12.Comma may be used within a string as a separator, semi-colon is used to separate strings from each other.

A BLOCK

Is a collection of strings. It is merely used in the 5110 to break up bulk transmissions. Blocks are separated by CR LF (Carriage return, line feed).

A RECORD

A record contains a number of strings or blocks and is terminated by CRLF. The instrument will accept one record into its input buffer before actioning it (excepting mass data,.)

When the instrument transmits, it will issue one record for each interrogative command in the record in the input buffer.

Note that when the 5110 is receiving a record, the correct method of termination is CRLF with EOI asserted with LF. However, the CR is completely optional and is ignored; if necessary the LF can be left out as well, so long as EOI is asserted with the last character of the record; and finally, if LF is used to terminate the record, then EOI does not need to be asserted. So valid record terminators are:

record	CR LF	(with EOI)
record	CR LF	
record	LF	(with EOI)
record	LF	
record		(with EOI)

EOI signifies to the 5110 that the talker has nothing more to say, so, in the case of multi-record commands (e.g: "ST1"), EOI should be sent only at the end of the last record, otherwise it will signify the end of the command, and no more strings or records will be excepted.

3.23.3 OPERATION

The 5110 processes commands sent as ASC11 (ISO–7) Blocks Records. The instrument will perform no operations or checking until a LF is received. At any point until the LF has been received CTL – X may be used to expunge the current block from the 5110's input buffer and DEL may be used to remove the last sent character spaces and other characters of hex value less than 30 (with exceptions as specified) will be ignored to ease syntax requirements. Text within brackets ( ) will be ignored to allow comments in self – documenting command sequences. (Note that a right bracket will be assumed upon receipt of LF).

Most commands have an assertive and an interrogative form PARAMETER – CODE = Setting will perform the change indicated while PARAMETER – CODE is a request for the current setting to be transmitted.

e.g:	VP1	(CONTROLLER)
	VP1 = 3.1 E+00	(5110 Vertical position CH1 = 3.1cm)
	VP1 = 6.2	(Controller changing shift value)
	VP1	(Controller)
	VP1 = 6.2 E+00	(5110)

Assertive commands can only be sent when remote or listen only. If an assertive command is sent when local, it is ignored.

When local there is a general 30 second time out on the bus transactions to prevent the instrument being locked up permanently. Thus, if the controller send an interrogative command, but does not listen for the reply, the 5110 will keep trying to send its response for 30 seconds and will then time out.

Special ASCII Characters

"	start or terminate a taxt string
'	(Single quotes)
(	start of comment
)	end of comment
#	string header (as part of numeric base identifier)
*	family descriptor
+	] numeric sign
-	]

DEL (S7F)	delete last character
CTL –X (S18)	delete contents of input buffer

many commands can be used with a family descriptor (*) for example:-

VP* (Controller)	
VP1 = 3.1E+00]	[5110 vertical position CH1 =3.1cm)
VP2 = 2.4E+00]	[5110 vertical position CH2 =7.4cm)
VP* = 6.2	[controller changing both shift values]

In general, several commands can be combined into a record (each command being separated by ";"). The commands will then be actioned in sequence.

e.g: "VP1 = 0 ; CM =RT;ARM"
(Controller sets CH1 shift = 0
capture mode to Real-time and
then arms for acquisition)

Commands which require numeric parameters (eg: cursor position, CP1 Delay Time, DT) have parameters that follow the recommendation of BSI6146 part 2: 1981 (NR1 & NR3). That is, numbers in scientific notation with exponent in multiples of 3 will normally be transmitted for real numbers.

e.g: DT = + 20.01E – 06
e.g: VP1 = 412.0 E+03

and numbers with no decimal point or exponent. Will be transmitted as for integers e.g: DN = 137, e.g: BL = 80 when receiving numeric parameters from the bus the requirements are, in general, more relaxed:

1) The number must contain less than 14 characters.
2) The number can contain but need not contain a decimal point.
3) The number can contain but need not contain a sign ("+" or "–").
4) The number can contain but need not contain an exponent.
5) The exponent is pre-fixed by "E".

6) The exponent can contain but need not contain a sign.

7) The exponent must not contain a decimal point.

8) If no sign is included, "+" is assumed.

Note that bulk data transfer commands (e.g: ST1) have stricter syntax requirements see page Appendix A.

3.23.4 VERTICAL MODE

COMMAND			OPTION
VM	(VERTICAL MODE)	= CH1	01
		CH2	02
		DUAL	03
		CHOP	04
		ALT	05
		ADD	06
TV	(TRIGGER VIEW)	= 1 ON	)09
		0 OFF	)09
P	[1] (PROBE)	= X1	)
	[2]	X10	)11 & 12
	[*]		
VP	[1] (VERTICAL POSITION)	= SIGN NUMBERS	
	[2] (Y SHIFT)	(DIVS)	
	[*]		
VS	[1] (VERTICAL SCALING)	= for UNCAL SIGN	
	[2]	NUMBERS	
	[*]	(V/DIV)	
		└── 07,08	
VC	[1] (VERTICAL COUPLING)	= AC	
	[2]	DC	
	[*]	GND	

Note that assertive commands VS*, VC*, and HS* can be used to change the main control settings.

e.g if "VS1 = 56–3" is sent, a message will appear on the screen, requesting the appropriate manual control change, until the control is in the correct position.

3.23.5 HORIZONTAL MODE

COMMAND			OPTION
HM	(HORIZONTAL MODE)	= A	01
		INTEN	02
		B	03
		DUAL	04
		XY	05
B	[1] (ENABLE B1(3))	= 1 (on)	06,07
		0 (off)	
HE	(HORIZONTAL EXPANSION	= 1	11
	(X10 EXPANSION)	0	
XC	(X TRACKS CURSOR)	= 1	12
		0	
HS	[A] (HORIZONTAL SCALING)		
	[B]	= for UNCAL NUMBER	
	[*]	(TIME/DIV)	
HP	(HORIZONTAL POSITION)	= SIGN NUMBER	
	(X SHIFT)	(DIVS)	

3.23.6 TRIGGER MODE

COMMAND			OPTION
SM	(SWEEP MODE)	= NORMAL	01
		AUTO	02
AS	(A SWEEP START)	= TRIGGER	11
		DELAY	12
AD	(A SWEEP DELAY	T	21
	CONFIGURATION)	N	22
		A/N	23
		CLK	24
BS	(B SWEEP START)	= C	13
		C + TR	14
		D	15
		D + TR	16
		BTR	17
		AS	18
		C + D	19
		TCAL	88
		General Mode	
BD	(B SWEEP DELAY	= AS	31
	CONFIGURATION)	BTR	32
		C	33
		C + BTR	34
		ATR	35
		C + ATR	36
		T	37
		N	38
BD		OR	
		TR/N	39
DT	(DELAY TIME)	= NUMBER	41
		(SEC)	
DN	(DELAY NUMBER)	= NUMBER	42
		(UNITS)	
DST	(DELAY STEP TIME)	= NUMBER	43
		SEC	
DSN	(DELAY STEP NUMBER)	= NUMBER	43
		UNITS	
PH +	/* (PHASE ADVANCE BY		45
	ONE STEP)		
PH –	/* (PHASE RETARD BY		
	ONE STEP)		

/* NO INTERROGATIVE FORM

3.23.7 MEMORY MODE

COMMAND			OPTION
DS	[1] (DISPLAY OF STORE)	= 1 (ON)	01,02
	[2]	0 (OFF)	
	[*]		

CS	(CAPTURE SOURCE)	=	CH1	11
			CH2	12
			DUAL	13
			A	14
			B/B1	15
			B3	16
CD	(CAPTURE DESTINATION)	=	S1	17
			S2	18
			DUAL	13
ARM	/* (START CAPTURE)			19
GET	/* (ARM FOR CAPTURE, TRIGGER ON "GET")			-
CM	(CAPTURE MODE)	=	RT	21
			REP	22
PT	(PRE-TRIGGER)	=	0	23
			50	24
AV	(NO: OF AVERAGES)	=	NUMBERS	25
PS	(PLOT SOURCE)	=	S1	31
			S2	32
PR	(PLOT RATE)	=	NUMBERS	37
PLOT	(START OR	=	ON	38
	STOP PLOT)	=	OFF	39
/* NO INTERROGATIVE FORM.				
PLX	(SET PLOT X OUTPUT TO MAX)			42
PLY+	(SET PLOT Y OUTPUT TO +MAX)			42
PLY–	(SET PLOT Y OUTPUT TO –MAX)			43

3.23.8 CALCULATION MODE

COMMAND				OPTION
XP	(X PARAMETER OF CURRENT CURSOR	=	AUTO	11
			XTAL	12
			EVNT	13
DD	(DATA WORD DISPLAY)	=	1 (ON)	14
			0 (OFF)	
DC	(DATA WORD CODING)	=	1 (HEX)	15
			0 (BINARY)	
HD	(MACHINE HORIZONTAL TIME DATUM)	=	A	34
			B	35
			AUTO	36
UD	(USER DATUM)	=	0 (ON)	21
			1 (OFF)	
UV/*	(C.C. VOLTAGE – USER DATUM)			31
UT/*	(C.C. TIME – USER DATUM)			32
UB/*	(C.C. VOLTAGE – & TIME – USER DATUM) (BOTH)			33

U12 (C1 & C2 User Datum)
value = NUMBER, NUMBER, NUMBER

U34 (C3 & C4 User Datum)

value	22	23	24
	volts	time	events

If a NUMBER is missed out when sending the string then that value will not be changed.

e.g "V12 = „ 12" will change C1 & C2 user datum events to 12, while not changing their time and voltage user datums.

A calculation is initiated by the "CA" command.
A service request will be issued when the result is ready; the latter is read via the "RS" command.

		OPTION
CA =	CP1	
	CP2	
	CP3	
Current cursor type reading:	CP4	
	CS1	
	CS2	
	CS3	
	CS4	

Voltage Between	DIFF		41
Rise Time + Oshoot	TR		42
V & T @ 50%	VT50		43
Period	PER	At between	44
V + MAX	MAX	specified Cursors	45
V – MIN	MIN		46
Peak to Peak	P–P		47

The format is e.g: "CA = CP1"
or: "CA = DIFF,C1,C3"
or: "CA = MIN,C2,C3"
or: "CA = PER,C3,C4"

RS = CRLF

Or string of the form
e.g: "RS = CP1,–4.21E+00,21E–03"
or: "RS - DIFF,C1,C3,2.13E+00,6.53E–06"
or: "RS = MIN,C2,C3,2.70E+00,1E–20"
or: "CA = PER,C3,C4,27E–6"

Note: Quotes shown for clarity only.

Calculations are of two general types; current cursor reading and calculations between cursors.

Current Cursor Calculations

These measure the voltage and time at a particular cursor for example:- "CA = CP3" requests the reading on the realtime trace at cursor 3 position, and "CA = CS2" requests the reading on a stored trace at cursor 2 position. If both stores are turned on, CS1 and CS2 will be on store 1, CS3 & CS4 on store 2. If both real-time channels are turned on C1 and C2 will be on CH1,C3 and C4 on CH2.

The result of the calculation is requested by the command "RS". The response to this is of the form:

+"RS CP3, –3.232E+00, 82.00E–06"

Where the first numeric parameter is the voltage and the second is the time in seconds. Note that if the X-parameter

of current cursor is set to B trigger even to (i.e: XP = EVNT) then the second numeric parameter will be the integer number of B trigger events to the cursor (and not time to the cursor).

Calculations Between Cursors

The calculations correspond to Calculation Mode options 41 to 47. They require two cursors to be specified as parameters.

The format is:

CA = calculation , cursor , cursor

The result is requested by command "RS". The response depends on the calculation last performed as follows:

RS = DIFF , cursor , cursor , volts , time .
RS = TR , cursor , cursor , volts , overshoot
RS = VT50 , cursor , cursor , volts , time ,
RS = PER , cursor , cursor , time ,
RS = MAX , cursor , cursor , volts , time
RS = MIN , cursor , cursor , volts , time
RS = P–P , cursor , cursor , volts ,

If a part of either type of calculation is unsuccessful, for any reason (eg: Uncalibrated Y-Amplifier, or ADC overrange) the value for the unobtained parameter is given as " 1E – 20 " for ease of detection.

3.23.9 GENERAL MODE

COMMAND			OPTION
RESET /* SELECT DEFAULT SETTINGS			41
|*			
UNC (RESET SOFTWARE CALIBRATION FACTORS)	=	H	82
		V	83
		P	84
TC (TIME-CAL)	=	1 (ON)	88
		0 (OFF)	
TP (TIME-CAL PERIOD)	=	NUMBER	89
CAL = [A /*			51
B			52
CH1 (SOFTWARE			55
CH2 CALIBRATION)			56
P1			53
P2]			54

Software calibration when remote users exactly the same sequence as when local, except that response is expected from the GPIB, not the keypad.

Whenever a reply is required from the controller, the serial poll value changes from 16 (busy) to 0 (not busy), and a response must be sent over the bus. A series of responses may be sent, separated by commas or semi-colons and terminated by CRLF. If at any time the calibration for B, the sequence is terminated and a "selection failure" SRQ is sent. On successful completion of the calibration, a "completed" SRQ will be sent.

A typical sequence sent by the controller might be:-
CAL = CH1, Y,N, 6.03E – 3,Y CRLF

Thus requests s/v cal of CH1, this range only 6mV is not time value, 6.03E–3V is time value.

Then wait for serial poll is not busy and reverse polarity of input and send:
" [" CRLF ie continue.
then wait for serial poll not busy and input –15mV and send "Y" CRLF i.e.15mV in time value.
Then wait for serial poll not busy and reverse polarity of input and send " [" CRLF i.e continue.
Then wait for serial poll "completed".

/* NO INTERROGATIVE FORM.

3.23.10 MISCELLANEOUS COMMANDS

CP [1 2 3 4 *] = NUMBER
Cursor Position In Divs:

CS [1 2 3 4 *] = NUMBER
Store Cursor Position In Divs:

BL = NUMBER Specifies maximum Block Length

NB (Numeric Base) = OCT (ASC11) | CHOICE APPLIES
BIN | TO BULK TRANSFER
HEX (ASC11) | ONLY ie: ST1, ST2
DEC (ASC11) | AND MS* AND MSS*

ALL (Interrogative Only) will output the entire state of the instrument as if all interrogatives had been sent.

CA [1 2 3 4 5] = 1 (ON) Turn On Or Off cursor.
0 (OFF) (Cursor Activation)

(Service Request)

In addition to indication of error and previously mentioned messages to the bus controller, 9 service request status values are allocated to the keys 1 through to 9 in REMOTE Mode. This, together with the text (TXT) option allows user defined interraction between bus controller and operator.

SRQ = 1 (On) enable/disable SRQ's
0 (Off)

If required, all SRQ's can be disabled, using "SRQ = 0" to find out if a command was successful "SRQV" can be used.

SRQV /* responds with the value of the last SRQ to be sent (or that would have been sent if not disabled).

ERRV /* responds with an error number indicating a reason for a selection failure.

/* NO INTERROGATIVE FORM.

TXT = " ASCII STRING " Send of receive screen text. .

The command TXT responds by transmitting the contents of

the displayed screen as a string of 512 bytes preceded and terminated by quotation marks. The bytes correspond in general to the ASCII standard, except for special characters which are given values between 0 and 20.

The command can be used to send characters to the screen, when remote, in which case the header is sent followed by the request string in single or double quotations marks (" or '). The ASCII character for line feed (Value 10 or hex value OA) moves the following characters to the start of the next line. Note that input buffer is only 256 characters and this limits the number characters that can be sent to the instrument at any one time.

(e.g: TXT = ' LF LF LF Hello,hello,hello')

CLS /* CLEAR SCREEN.

If the 5110 is in LOCAL mode, it will not respond to programming commands (this is a requirement of the IEEE specification) nor will it store them for use when it enters REMOTE mode.

RS [1 2 3 . . . . 8 *] /*

recall machine state as RS key.

SS [1 2 3 . . . . . *] ,Y /* ,N

Save machine state as SS key but:
,Y causes manual controls to be included
,N does not
,N is assumed if nothing sent

RESET /*

recall machine state 0 (ie. the default settings)

/* NO INTERROGATIVE FORM.

3.23.11 MASS DATA COMMANDS

MS [1 2 3 . . . . 8 9 *]

Will cause the contents of the specified machine state to be input or output as appropriate details as defined in Appendix A. The machine state is in a compressed form not readily readable by the user.

Note: the special case of MS9 which will output the current machine state or input and use a machine state.

ST [1 2 *]

Will cause the contents of the specified store to be input or output as appropriate, as mass data as defined in Appendix A; this is followed by information about the store capture source.

e.g: ST1 = 1,2. . . CRLF [VERTICAL], [HORIZONTAL], [CENTRELINE], [BLANKA], [BLANK B], [MISC] CRLF

Where

[VERTICAL] is an exponent type number (NR3) respeseniting the vertical scaling in volts/Div.

[HORIZONTAL] is an exponent type number (NR3) representing the Horizontal scaling in seconds/Div.

[CENTRELINE] is an exponent type number (NR3) representing the centre line value in volts.

[BLANKA] is an integer (NR1) in the range 0–99 pointing to the first brighted-up store location.

[BLANK B] is an integer (NR1) in the range 0–99 representing the offset from one brighted-up location to the next, decremented by one.

[MISC] is an integer in the range 0–9215 (NR1) representing a 16 bit, bit organised number, defined as follows:-

BIT NUMBER	BINARY WEIGHTING	DEFINITION
15		ALWAYS ZERO
14		ALWAYS ZERO
13	8192	1 = TIMEBASE B, 0 = TIMEBASE A
12,11,10		ALWAYS ZERO
9	512	1 = REAL TIME 0 = REPETITIVE
8	256	1 = HORIZONTAL UNCAL
7,6		ALWAYS ZERO
5	32	1 = CH2,0=CH1
4	16	1 = INVERTED
3	8	1 = X10, 0 =X1
2	4	1 =AC, 0=DC
1	2	1 = SIGNAL 0 = GROUNDED
0	1	1=VERTICAL UNCAL

NOTES:

1. The absolute voltage represented by the contents of any store location may be calculated as follows.

   Voltage = Contents (−128 to +127) *[VERTICAL] *0.032
   + [CENTRELINE]

   In the example shown below the first location represents.

   −36 * 2.00 * 0.032 + 7.232 = 4.928 volts.

2. The time represented by any store location with respect to the first location may be calculated as follows:

   Time = location (0 to 1023) * [HORIZONTAL] * 0.01

   In the example shown below, the time represented by the second shown location is:

   1 * 20E − 6 X0.01 = 200ns.

3. The construction of [BLANKA] & [BLANK B] is such that 0,0 represents all locations brighted-up. If a store had been acquired by expanded real-time, ie: real time above .1ms/Div as in the example, only the brighted-up locations contain valid samples.

   Thus in the example, 0,9 the first valid location is 0, then 10,20 etc:

4. The [MISC] number contains more information than is available on the screen.

   In the example below we have:

   518 = 0000001000000110

   Capture source CH1, TBA, AC Coupled, Real-time capture not inverted , no x 10, no UNCALS.

5. If a store block is being constructed artificialy, it is sufficient to set [BLANKA] = [BLANK B] = 0 and [MISC] = 2

EXAMPLE

ST1= −36,-36..−36CRLF +2.00E+00,+20.0E−06,7.232E+00, 0,9,518 CRLF.

MSS [1 2 3 . . . 8 *] Will cause the contents of the specified machine state stored/store 2 block to be input or output as appropriate as mass data as defined in Appendix A. The store 1 equivalent followed by the Store 2 equivalent is treated as 1024 contiguous bytes. The mass data is followed by the parameters for the store 1 equivalent then those for the store 2 equivalent details as described for ST1.

e.g: MSS 1 = 1,2 . . . . . 127 CRLF MASS DATA

+2.00E + 00, + 10.0E −06,0.000E + 00,0,0,6,CRLF
STORE 1 EQUIV

+1.00E + 00, + 10.0E −06,0.000E + 00,0,0,38CRLF
STORE 2 EQUIV

3.23.12 APPENDIX A

MASS TRANSFER DATA GENERAL

1. A family command e.g.: ST* may be used to read mass data from the instrument but not to write to it.
2. When the instrument outputs mass data, the numeric base and block length will be as specified in separate commands by the user (note: binary is continuous).
3. When mass data is sent to the instrument the numeric base is deduced from the data string (see Mass Transfer Data Format) and block length is irrelevant.
4. If the instrument is sent EOI-true with data byte, the instrument will consider the transfer terminated at that point e.g.: sending ST1 = 2,3 will cause only

   EOI

   the first two store locations to be changed and the store parameters to be left unchanged.

MASS TRANSFER DATA FORMAT

Mass data consists of three main sections:−

1. A header which is specific to the command in operation e.g.: ST1 =
2. A numeric base identifier (where appropriate)
   i.e. #B Binary.
   #O Octal.
   #H Hexadecimal.
   " Opening quotes for text.

   There is no identifier for decimal.

The data itself, which is as follows.

a) Binary

MS1 = #BLLDDDD . . . . CC CRLF

where LL is a byte count of the following data including the two byte checksum.

CC is a two byte checksum of all bytes 'D' (i.e. not including LL)

All eight bit characters are valid between #B and CRLF.

DD . . . . . DD represents data bytes.

Note that upon receipt of checksum CC, the instrument expects ASCII (ISO-7) only and expects LF (with or without CR)

b) Decimal

MS1 = 1,27, − 128 . . . . . +127 CRLF

1. Output is bipolar, in the range −128 to +127 producing zero for mid-screen in the case of store data and +127 at top of screen.
2. Leading zero's are not output but are acceptable when supplied.
3. Leading '+' is output but will be assured if space is supplied.
4. Values are normally separated by comma but

CRLF is substituted at the end of intermediate blocks (Block length non zero) and as the final terminator. Note that a comma preceding the final terminator will cause a syntax error.

5. If the first character following a comma is another comma, the value of zero is assumed.
e.g. 1,,3 is equivalent to 1,0,3.

6. If a value contains both + and – signs, minus will be used regardless of the order in which they appear.

c) Octal

MS1 = #0001,010 . . . . . 377 CRLF

NOTES:

1. The output is unsigned in the range 000 to 377.
2. Leading zero's are output but are not absolutely required on input.
3. Notes: (4) and (5) of decimal also apply.

d) Hexadecimal

MS1 = #H01, 0F . . . . . FF CRLF

NOTES:

1. The output is unsigned in the range 00 to FF.
2. Leading zero's are output but are not absolutely required on input.
3. Notes (4) and (5) of decimal also apply.

3.23.13 APPENDIX B

SERVICE REQUESTS

The following is a list of Service Request Values that can be sent by the 5110.

SRQ VALUE	MEANING
0	OK
16	BUSY
64–73	USER REQUESTS 0–9 (i.e.: USER PRESSED A BUTTON 0–9)
74	COMPLETED
80	BUSY
96	INVALID COMMAND
97	UACG: (UNDEFINED ADDRESSED COMMAND GROUP)
98	SRQ OVERFLOW
99	BUFFER OVERFLOW
100	SELECTION FAILURE
101	NOT ALLOWED WHEN LOCAL
102	SYNTAX ERROR
103	NUMBER OUT OF RANGE/ UNACCEPTABLE
104	LENGTH ERROR
105	CHECKSUM ERROR

In general, SRQ values below 81 can be considered non-fatal and do not affect the function of the instrument. All other SRQ's however hold up the instrument until that SRQ has been correctly serviced. Up to 10 non-fatal SRQ's may be stacked up waiting to be serviced before a fatal "SRQ Overflow" occurs. So as not to lock up the instrument when local, no service requests are sent when local.

3.24 SYSTEM ERROR MESSAGES LISTED BY ERROR NUMBER (ERRV)

1 SELECTION ABOVE AVAILABLE RANGE

2 OPTION DOES NOT EXIST

3 NUMERIC ENTRY NOT APPLICABLE

5 OPTS 3, 4 & 5 REQUIRE "B1" AND/OR "B3"
Must specify which B sweep before using it. (Option 6 or 7)

6 N/A UNTIL CURSOR 1 IS ON
Cannot enable a B1 sweep if cursor 1 is not on

7 N/A UNTIL CURSOR 3 IS ON
Cannot enable a B3 sweep if cursor 3 is not on

9 N/A UNTIL TALK ONLY

12 COUNTER ASSIGNED TO DELAY SYSTEM
Either T/B "B" or "A" is using the delay system. (see TRIGGER mode options 11–19)

15 COUNTER ADDIGNED TO TIMEBASE B
TRIGGER option 15, 16 or 19 already selected

16 COUNTER ASSIGNED TO TIMEBASE A
TRIGGER option 11 already selected

17 COUNTER ASSIGNED TO CURSORS CALCULATION option 12 or 13 already selected

18 ERROR: OUTSIDE AVAILABLE RANGE

19 1–2–5 SEQUENCE ONLY

20 INVALID ENTRY

22 OPTION NOT AVAILABLE
e.g. starting a B sweep on trigger eliminates access to ENABLE B1 and ENABLE B3 in HORIZONTAL menu.

23 "B" TRIG N DOES NOT REQUIRE A START SELECTION

24 PHASE SHIFT ONLY APPLICABLE WITH OPTS 23, 24 AND 39
i.e. either "A" or "B" must be started by trigger divided by N or Time divided by N

25 ALTERNATE NOT AVAILABLE IN X–Y MODE

26 X–Y MODE REQUIRES NO X10 EXPANSION

27 OPTS 16 AND 19 ONLY ALLOWED WITH OPTS 31, 33 AND 39

29 ABORT
Premature termination by Quit

31 SOURCE SELECTION ERROR
Attempting to acquire from a channel not turned on

32 SWEEP SELECTION ERROR
Attempting to acquire from a sweep not turned on

33 N/A UNTIL CURSOR SELECTED

34 CURSORS MUST BE ON SAME TRACE
Cursors are dynamically allocated according to the number of real time traces and stored traces. Consult allocation table.

35 TIMEOUT FAILED
a) Indicates malfunction of ADC or Timebase hardware
b) Interruption of data flow for more than 30 sec in GPIB transfer when local.

36 *** PLOT IN PROGRESS ***
Store contents cannot be modified while a Plot is in progress.

70 "B" SWEEP ERROR: "A" ONLY SELECTED
Caused by switching from a "B" sweep which does not involve cursors to one which does when the relevant sweep is not enabled.

3.25 COMMAND SUMMARY

COMMAND		PARAMETERS	SPECIAL NOTES
AD	"A" sweep Delay	T / N / A/N / CLK	
*ALL	output machine state in ASCII		
*ARM	ARM single shot		
AS	"A" sweep Started by	TRIG / DELAY	
AV	no of AVerages	(NR3)	1,2,4,8,16 . . 256
B	1 / 3 enable "B" sweep	0 / 1	
BD	"B" sweep delay	[AS / BTR / C / C+BTR / ATR / C+ATR], [T / N]	comma only required if both fields specified
		OR TR/N	
BL	Block Length	(NR3)	0 to 80
BS	"B" sweep Started by	C / C+TR / D / D+TR / BTR / AS / C+D / TCAL	
*CA	CAlculation	CP1 / CP2 / CP3 / CP4 / CS1 / CS2 / CS3 / CS4	
		OR	
		DIFF / MAX / MIN / P–P / PER / TR , C1 / C2 / C3 / C4 , C1 / C2 / C3 / C4	
CA	1 / 2 / 3 / 4 / * Cursor Active	1 / 0	
*CAL	CALibrate	A / B / CH1 / CH2 / P1 / P2	Further parameters required as Calibration sequence continues
CD	Capture Destination	S1 / S2 / DUAL	
*CLS	CLear Screen		
CM	Capture Mode	RT / REP	
CP	1 / 2 / 3 / 4 / * Cursor Position	(NR1)	0.0 to 11.46
CS	Capture Source	[CH1 / CH2 / DUAL], [A / B/B1 / B3]	comma only required if both fields specified

CS {1 2 3 4 *}	Position of Cursor on Store	(NR1)	0.0 TO 10.23
DC	Data pod Coding	{0 1}	
DD	Data pod Display	{0 1}	
DN	Delay Number	(NR3)	0 TO 999999999
DS {1 2 *}	Display of Store	{0 1}	
DSN	Delay Step Number	(NR3)	1 TO 999999999
DST	Delay Step Time	(NR1)	IE–8 TO 343.597
DT	Delay Time	(NR1)	0 or IE-8 TO 343.597
**ERRV	ERRor Value	(NR3)	
*GET	Initialise for G.E.T.		
HD	Horizontal Datum	{A B AUTO}	
HE	Horizontal Expansion	{0 1}	
HM	Horizontal Mode	{A B DUAL INTEN XY}	
HP	Horizontal Position	(NR1)	0.0 TO 11.46
HS {A B *}	Horizontal Scaling	[>] [(NR1)]	50E-9 TO 0.5 in 1, 2, 5 sequence
MS {1 2 3 4 5 6 7 8 9 *}	Machine State	(MASS TRANSFER)	

MSS {1 2 3 4 5 6 7 8 *}	Machine State Store	(MASS TRANSFER)	
NB	Numeric Base	{BIN DEC HEX OCT}	
P {1 2 *}	Probe scaling	{0 1}	
*PH+	PHase advance		
*PH–	PHase retard		
PLOT		{OFF ON}	
*PLX	PLot output to X full scale		
*PLY+	PLot output to Y +full scale		
*PLY–	PLot output to Y –full scale		
PR	Plot Rate	(NR1)	in 1, 2, 5 sequence
PS	Plot Source	{S1 S2}	
PT	Pre-Trigger	{0 50}	
*RESET	recall machine state zero		
**RS	ReSult of calculation		format depends on previous "CA" command
*RS {1 2 3 4 5 6 7 8}	Recall machine State		
SM	Sweep Mode	{AUTO NORMAL}	
SRQ	SeRvice reQuest	{0 1}	
**SRQV	SeRvice reQuest Value	(NR3)	

*SS {1 2 3 4 5 6 7 8 *} [, {Y N}] Save machine State

ST {1 transfer 2 STore *} (MASS TRANSFER)

TC Time-Cal ON/OFF {0 1}

TP Time-cal Period (NR1) 40E-9 TO 343.597

TV Trigger View {0 1}

TXT "(ASCII STRING)"

U {12 34} User datum value [(NR1)] , [(NR1)] , [(NR3)] comma's not optional

*UB Update Both user datums

UD User Datum on/off {0 1}

*UNC delete software calibration (UNCal) {H P V}

*UT Update user Time datum

*UV Update user Voltage datum

VC {1 2 *} Vertical Coupling {AC DC GND}

VM Vertical Mode {CH1 CH2 ADD ALT CHOP DUAL}

VP {1 2 *} Vertical Position (NR1) –32.7 TO 32.7

VS {1 2 *} Vertical SCaling [{+ –}] [>] [(NR1)] 2E-3 TO 5 in 1, 2, 5 sequence

XC X tracks Cursor {0 1}

XP X Parameter {AUTO EVNT XTAL}

*ASSERTIVE ONLY [OPTIONAL]

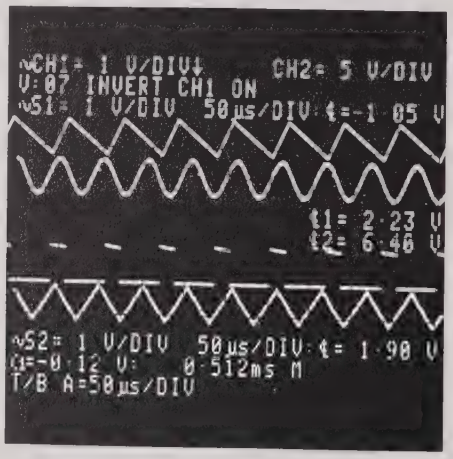
**INTERROGATIVE ONLY {ALTERNATIVES}

This indicates that the horizontal mode menu was displayed prior to obtaining the mixed display and that the mode selected was option 04 – A Alternate B.

CH1 & CH2 sensitivity settings indicating that Dual Display was selected for the Vertical Mode.

∿ indicates that CH1 is AC coupled and its absence indicates that CH2 is DC coupled.

GND appears here when the channel input is grounded. > instead of = indicates uncalibrated (ie centre variable control is in use).
:= instead of = indicates x10 probe scaling.
↓ indicates the displayed trace is inverted.


∿CH1= 1 V/DIV↓ CH2= 5 V/DIV
V:07 INVERT CH1 ON
∿S1= 1 V/DIV 50µs/DIV ℓ=-1·05 V
ℓ1= 2·23 V
ℓ2= 6·46 V
∿S2= 1 V/DIV 50µs/DIV ℓ= 1·90 V
Δ=-0·12 V: 0·512ms M
T/B A=50µs/DIV

Voltage Levels of Sweep Centre Lines

A & B Timebase settings
> instead of = indicates uncalibrated (ie centre variable control is in use).
:= instead of = indicates X10 expansion.

Current Cursor Information.

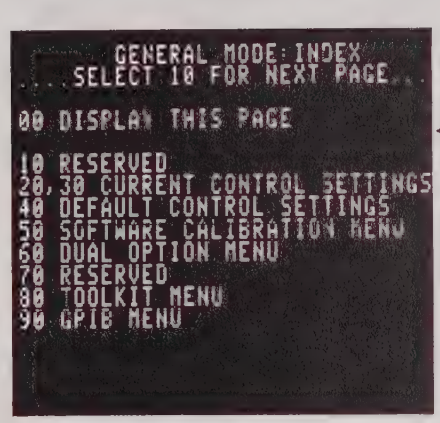
The 3-digit readout for time indicates that the X parameter measurement is in auto-time mode.

The A indicates that the Horizontal Datum is the start of the A sweep.

X would appear on this line if the Timer/Counter was being used for the time measurement, and E if time was being measured as "Number of Events" U would also appear if "User Datums" had been selected for the calculation mode.

Fig. 3.1 Typical Mixed Display

This form of instruction appears on every menu page except the last, when
.....Final Page.....
appears instead.



Keying instructions (Options) for obtaining menu pages. eg Key 20 to obtain page 1 of Current Controls Settings (see Fig. 3.3).

Fig. 3.2 General Mode : Index

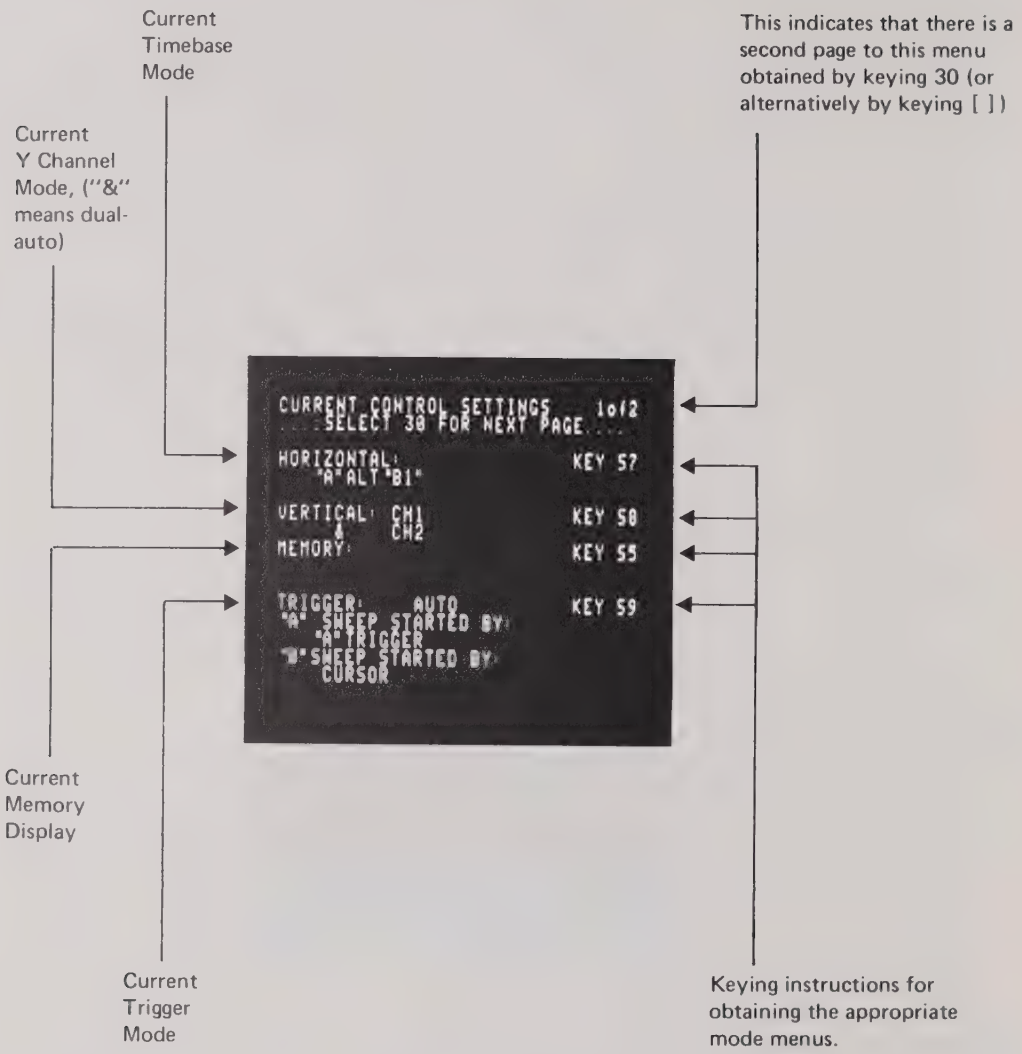


Fig. 3.3 Current Control Settings

Default conditions have been selected as No Operational Modes have been specified

Software Calibration Required

Press "Quit" in order to obtain Page 1 of Current Control Settings. (see Fig. 3.3).

Fig. 3.4 Power Up Report

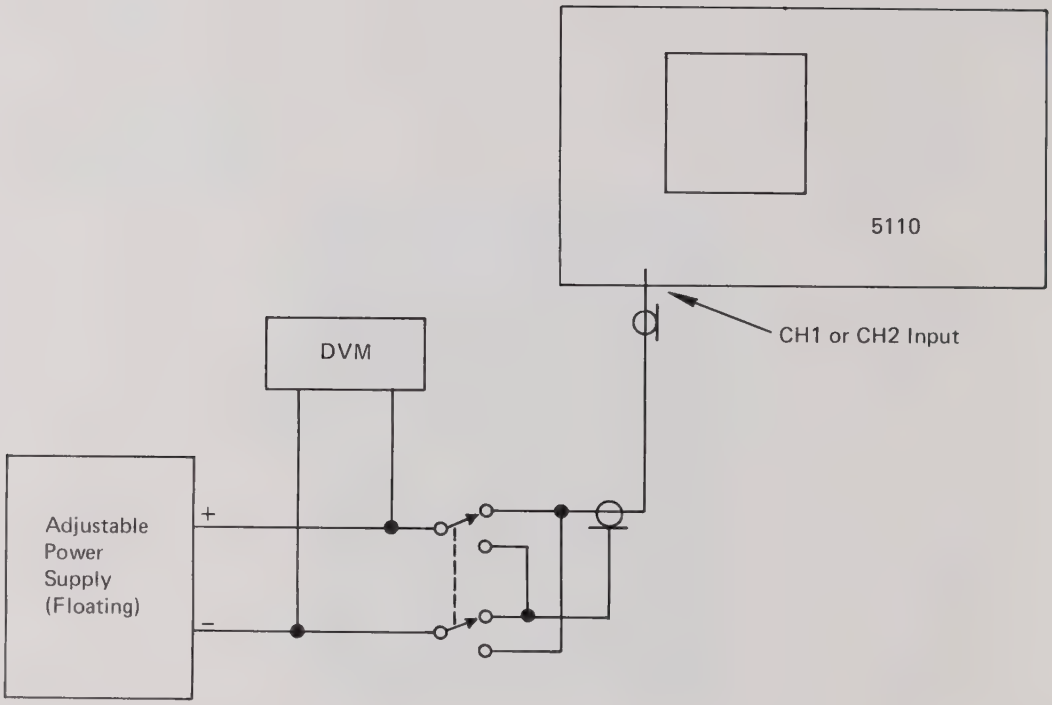


Fig. 3.5 Vertical Calibration : Connection of External Test Equipment

4.1 CIRCUIT DESCRIPTION OVERVIEW

The instrument is a 100MHz real time oscilloscope with added facilities. Those familiar with convential oscilloscopes will recognise many of the building blocks in Fig. 4.1.1.

Because of the complexity of switching required to implement the many different modes of operation, microprocessor controlled latches replace hardware switches normally found. Circuit complexity is also increased by the display of alphanumerics and stored traces simultaneously with real time traces on the CRT. Extra beam switches in the X, Y and brilliance signal paths enable alphanumerics to be independent of real time X, Y shift and brilliance controls.

Contained below is a synopsis of the instrument operation with enlargement in the areas of interaction between circuit blocks. For detailed descriptions of any part readers are directed to the relevant section.

4.1.1. Y SIGNAL PATH

The Y signals are input to the CH1 and CH2 preamplifiers via conventional X1, X10, X100 manual attenuators. After buffering, independent shift voltages are injected via a dc amplifier in each channel. Shift voltages are outputs of the voltage generator circuit which are appropriately scaled to give a software calibrated shift for all attenuator settings. The composite Y signal is applied to the 1, 2, 5 step attenuator, and then made differential. A trigger 'pick off' is taken from each channel at this point. A variable gain stage and signal inverting facilities for each channel are provided before the signal reaches the beam switches. The trigger-view signal from the trigger amplifier, and the Y portion of the alphanumeric display are taken to two more beam switches. The output of all four beam switches connect to a common differential bus and may be considered as a 1 of 4 selection in all cases except add mode where CH1 and CH2 are engaged simultaneously.

Vertical display modes (dual channel, add etc) are determined by the action of the display management logic on the beam switch drivers (E.C.L.). An overriding "force alpha" signal can cause these drivers to enable only the alpha beam switches, but normal control is via a shift register. By changing the clock rate, and serial bit pattern, as well as the shift register length, any or all of the beam switches can be sequentially (or simultaneously for add) enabled. It should be noted that the alpha beam switch is used to display stored traces as well as character data. In chop mode the register is clocked many times per trace, the transitions between channels being blanked to give a clear display. In alternate mode, each timebase sweep clocks the register to sequentially display realtime channels, Alphanumerics (including stored traces) are inserted by asserting the force alpha line and inhibiting the start of sweep. The rate at which the realtime display is interrupted to display alphanumerics, is determined by the display management logic. However, certain acquisition conditions need to override the display of alpha (so that no trigger events are lost) and also may require reconfiguration of the beam switch register.

The differential output to the four beam switches is taken to a delay line buffer and then to the differential delay line, which also acts as the interconnection between Y preamplifier and Y driver circuit boards. Delay inserted at this point allows fast trigger events to be viewed on screen. The delay of 100ns approximates to the accumulative X delay, (and bright-up delay) consisting of the trigger route, timebase start and X amplifier deflection. A buffered drive to the acquisition sampling circuit is taken from this point, allowing equal access to both Y channels. A hybrid Y deflection amplifier is coupled via low value resistors directly to the CRT, Y plates.

In A alternate B modes an unbalanced current; determined by the front panel "TRACE SEPARATE" control, may be drawn from the input of this hybrid amplifier to produce trace (Y) offset in B sweeps.

4.1.2. THE X SYSTEM

The X signal path has a beam switch, driven by the Y beam switch controller, so that alphanumeric X data is displayed synchronously with the alpha Y signal.

The horizontal mode of operation is configured directly by the microprocessor via write ports on the timebase board. Additionally the display management logic provides a system clock and can inhibit realtime sweeps (to insert alpha characters). The processor write ports initialise local logic for fast events, such as single shot trigger, where direct control would be too slow. System signals produced by the timebase (such as A gate) are relayed to the display management circuit as fast signals for immediate use. Relatively slow detectors are triggered by these signals and these detectors can be interrogated by the microprocessor to determine the display status.

The "A" and "B" timebase switches are independent front panel controls that set the speed of two identical ramp generators. A selected capacitor is charged by a constant current, and connected to a high impedance buffer. Variable speed is made possible by altering the value of charge current. The ramp is ended by switching in a constant current sink at a ramp voltage equivalent to approximately 11cms of X deflection. Although both ramp generators are independent it should be noted that B cannot run without A, nor can it exist outside it (i.e. A ends B when B ramp would continue after A has finished). Both ramps can be triggered (started) by either a conventional trigger amplifier or various combinations of the delay system output and/or trigger. Additionally for B sweep, cursors may be used, alone or again in combinations. A bright line "A" auto-trigger circuit provides a trigger in the absence of applied trigger in AUTO mode: (trigger preamplifier circuit).

X deflection is provided by a discrete component voltage amplifier in a bridge configuration, the outputs being d.c. coupled to the CRT X plates. The differential virtual

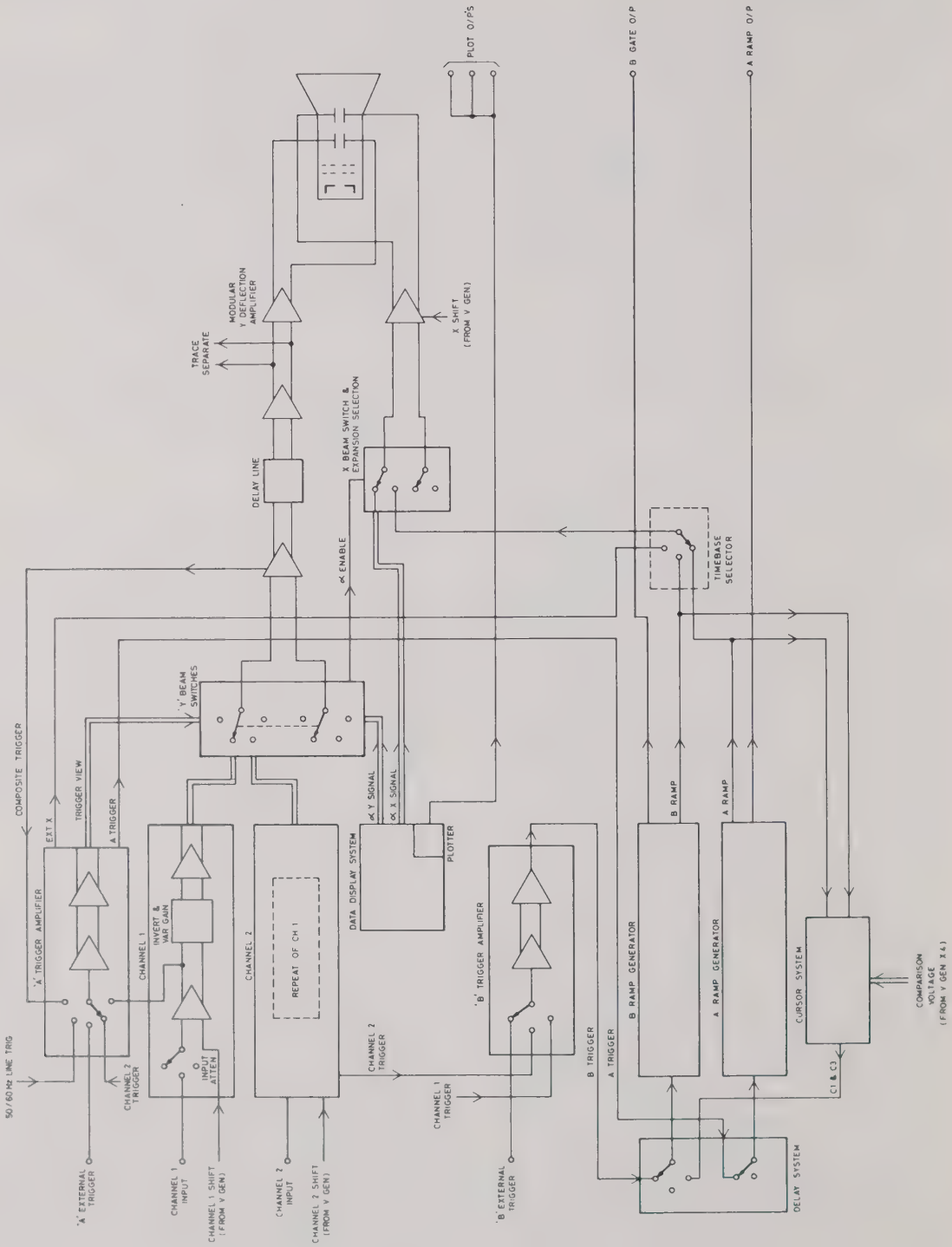


Fig. 4.1.1 Block Diagram

earth inputs of the voltage amplifier are connected to 3 current "tails". These form the X beam switch, giving in realtime two positions; normal (X1) gain and expanded (X10) gain. Additionally in the realtime signal path there is a 1 of 3 timebase selection. This is used to dynamically select, (i.e. for alternate sweeps) A or B ramp displayed in such modes as A alternate B. External X is selected only in X-Y mode, when X deflection is sourced from the A trigger amplifier, the X10 realtime beam switch being engaged.

Cursors are a result of a comparison between the selected ramp and individual outputs from the voltage generator. A bright up signal is provided from the timebase board which is equivalent to approximately 1mm of trace length. The four cursors also provide signals to the delay system; for use as start/stop events. This enables the delay system to be used to accurately measure X parameters without reliance on "A" ramp using the 100MHz crystal as reference.

Each cursor can also be selected to initiate a Y sample to be taken; giving extensive acquisition and measurement facilities.

Cursors 1 and 3 can also be used to either start or gate the start of B ramp, or again in combination with the delay system, start "B".

4.1.3 THE PROCESSOR SUB-SYSTEM

The microprocessor resident in the instrument is used to make control of many of the complex modes of operation simple for the operator to use. A typical sequence involving the microprocessor in this sort of task would be when, via the trigger menu, the operator requires an easily alterable delay. First the processor is interrupted from the keypad, and via write ports on the display management circuit forces alpha, to display the required menu. The operating conditions are then selected by the operator and temporarily stored. In this example a number representing the required delay (time on event) would then be converted into internal format and loaded into the delay system. A suitable delay increment would be specified to be implemented on turning spin-wheel control. The microprocessor then implements all of the multiway switching required to select the new mode of operation. Finally the display control ports are re-addressed to reform the display to include realtime.

Turning the spin-wheel results in a change of delay; the microprocessor detects the change in spin-wheel status, receiving an interrupt when the first valid movement occurs. The new value of delay is calculated and the delay system updated. The table of Fig. 5.6.1 Section 5 lists the control ports, and a general description of the function of each. Further Table fig. 5.6.2 lists each software port control line.

As well as control features the microprocessor provides data gathering and manipulation features. The positions of the front panel controls are monitored and displayed on the CRT. Calibrated shift voltages are introduced into the Y channels and any displayed voltage can be measured by the acquisition system. From these two data sources the microprocessor calculates the absolute input voltage. Cursor X parameters can be similarly calculated, presenting the operator with calibrated measurement facilities.

4.1.4 THE DIGITAL STORAGE SUB-SYSTEM

The 5110 includes some features of a digital storage oscilloscope, being able to capture two traces of 1024 points with 8 bit Y resolution. These recorded traces are replayed on request, simultaneously with the realtime sweeps, as part of the alphanumeric display phase, using the alpha digital to analogue converters (Data display board). A single follow-and-hold circuit on the Y output board (i.e. after the beam switches and delay line) is used to acquire Y channel analogue data. A successive approximation analogue to digital converter on the acquisition board quantizes this to 8 bit digital data. At slow sweep speeds (5s to 100μs/cm for dual channel) the conversion rate of 1μs per sample is sufficient for a simple clocked system to be used. The Y beam switch is put into chop and a programmable clock source is used with Y beam switch register to provide 1024 sample points across the screen. This represents the analogue timebase, for the acquisition system. For faster sweep speeds (50ns to 50μs/cm) a repetitive sampling technique is employed to extend the sampling system bandwidth. A cursor is used to obtain one data acquisition per "A" sweep. The chosen cursor is repeatedly moved in position relative to the selected ramp. A whole trace is provided after 1024 samples have been acquired, this taking at least 1024 scans of the timebase ramp. Signal averaging is optionally available on both forms of acquisition, the microprocessor being used to perform the data manipulation required.

Plotter outputs are provided by the data display sub system, using an 8 bit (Y) dac and a 10 bit (X) dac, and the programmable clock to control data rate. The processor is interrupted (FIRQ) at data rate: the service routine transfers X and Y data to the DAC latches.

Measurement on stored traces is made possible by recording the setting of front panel controls at the time of capture. Cursors, displayed as blanked portions of the trace, are manipulated by the microprocessor. Data in a 2 bit store addressed simultaneously with the trace data is used to control the blanking.

4.1.5 THE DELAY SUB-SYSTEM

This system is broadly an extension to the trigger facilities normally provided. Clock sources of A or B trigger allow delay by event, or starting of the trace every "Nth event", with a phase advance/retard mechanism allowing slip, so that any position of a cyclic sequence may be viewed. When delay by time is involved a 100MHz oscillator is connected as clock, giving 10ns resolution. The very long counter chain, which extends into software, maintains this resolution for the wide range of delays available.

When not devoted to trigger functions the timer/counter can be used for X measurement, by time or event. Out-

puts from the timebase and cursor sub-systems provide a range of start/stop signals. All stages of the counter chain can be read by the microprocessor.

The delay system can also be configured to give a time-cal-output to the front panel, in a range of values from 40ns to 344s. This allows a variable timebase to be calibrated, or markers to be set when standard timebase speeds are inconvenient to use.

4.1.6 GPIB SUB-SYSTEM

The GIPB assembly makes available a general purpose interface (to IEEE std 488) which can be used to control the oscilloscope or retrieve data from it. (Listener/talker but not controller). The bus is isolated via optical couplers from the main body of the instrument. When used to control the instrument an external system can control all conditions that can be set by the processor. The CRT is also available for message passing to a local operator. Group Execute Trigger (GET) by-passes the processor to initiate an immediate "A" ramp sweep. Both trace stores are accessable from the GPIBus and may be written to or read from, Co-resident on this board is an extra 10K bytes of non-volatile ram which is available for the retention of stored traces and machine set-up information.

4.2 CIRCUIT REFERENCES

4.2.1 INDEXED BY COMPONENT PREFIX

0 – 100	CHASSIS	
100 – 200	Y PRE-AMP CH1	
200 – 400	Y PRE-AMP CH2	
400 – 500	Y PRE-AMP AND POST BEAM-SWITCH	
500 – 600	TRIGGER PRE-AMP AND DAUGHTER BOARDS	
600 – 800	TRIGGER AMP MAIN BOARD	
800 – 900	TUBEBASE	
900 – 1000	POWER SUPPLY	
1000 – 1100	E.H.T.	TIMEBASE
1100 – 1200	A RAMP	TIMEBASE
1200 – 1300	B RAMP	TIMEBASE
1300 – 1400	T/B LOGIC	TIMEBASE
1400 – 1500	DELAY SYSTEM	TIMEBASE
1500 – 1600	CURSOR	TIMEBASE
1600 – 1700	KEYPAD AND ENCODER	
1700 – 1800	X OUTPUT	
1800 – 1900	C.P.U.	
1900 – 2000	DISPLAY MANAGEMENT	
2000 – 2100	VOLTAGE GENERATOR	
2100 – 2200	ACQUISITION AND STORE	
2200 – 2300	DATA DISPLAY	
2300 – 2400	GPIB	
2400 – 2500	Y AMPLIFIER	Y OUTPUT AND SAMPLING
2500 – 2600	SAMPLING	Y OUTPUT AND SAMPLING
2600 – 2700	POD INTERFACE	
2700 – 2800		
2800 – 2900		
2900 – 3000		
3000 – 3100		
3100 – 3200		
3200 – 3300		
3300 – 3400		

4.2.2 INDEXED BY BOARD

TITLE	COMP PRE-FIX	SK NO.
Y PRE AMP (2 SHTS)	100–599	SK2903
TRIGGER	600–799	SK2904
TUBEBASE	900	SK2905
POWER SUPPLY	1000	SK2906
E.H.T.	1100	SK2907
TIMEBASE (3 SHTS)	1200–1699	T/BASE SK2908 DELAY SK2909 CURSOR SK2910
KEYPAD & ENCODER	1800	SK2911
X DRIVER & OUTPUT	1900	SK2912
C.P.U.	2000	SK2913
DISPLAY MANAGEMENT	2400	SK2914
VOLTAGE GENERATOR	2500	SK2915
ACQUISITION & STORE	2600	SK2916
DATA DISPLAY	2700	SK2917
GPIB	2900	SK2918
Y OUTPUT & SAMPLING	3000–3250	SK2919
INTERFACE	3300	SK2920

4.3 POWER SUPPLIES

4.3.1 LOW VOLTAGE SUPPLIES

4.3.1.1 GENERAL

All power to the instrument is derived from the secondaries of a screened toroidal transformer. The primary windings are connected to switches that configure the transformer to match the available line voltage. Input power is applied via an internal socket and filter, both line and neutral being switched to turn the instrument on. Primary fault condition protection is provided by a line fuse, and additionally a thermal cutout set to open at 75°C mounted on the main heatsink. A fan is connected permanently across the primary winding of the transformer, to provide forced air cooling for the power supply components, which are located under a false rear panel. A sinusoidal inverter, driven from a low voltage supply provides the E.H.T. voltages required by the cathode ray tube.

Secondary windings ③ , ④ , and ⑤ on fig. 6.15 provide all the power at low voltage, each being rectified and smoothed then regulated.

"WARNING"
IT SHOULD BE NOTED THAT TRANSFORMER WINDING ⑥ ALTHOUGH ONLY OF 6.3V A.C. OUTPUT IS AT C.R.T. CATHODE POTENTIAL OF −2.2KV.

4.3.1.2 +5 VOLT SUPPLY (See Fig. 6.15)

Secondary winding 3 is full wave rectified by Schottky diodes D1 and D2, then smoothed by C1 and C11. Darlington transistor Q1 acts as a series pass element controlled by U1001. Referring to fig. 4.3.1 this integrated circuit has an internal reference voltage, (nominally 7.15V), on pin 6, which is taken to the non-inverting input of an integral error amplifier, via a potential divider chain R1006 variable, R1005 and R10012. The inverting input of the amplifier, pin 4, senses the output voltage of the pass transistor remotely to compensate for lead resistance. The error amplifier controls a transistor, collector pin 11, emitter 10, which in turn regulates the base current into Q1001, and hence maintains the output constant. Current limiting at 10 amps is provided by sensing the voltage across R1001 and using another transistor in the integrated circuit to remove base drive current from Q1001. Should the output be shorted to 0 volts, zener D1003 conducts and the current limiting circuit is used to shut the regulator down, avoiding considerable power dissipation in the pass transistor.

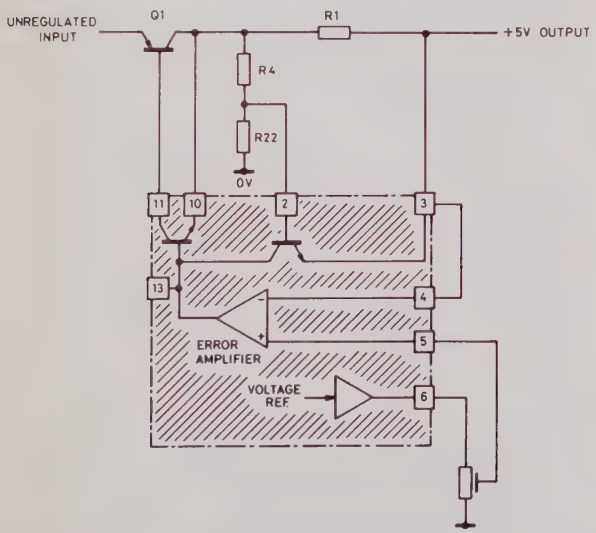


FIG. 4.3.1 +5V REGULATOR SCHEMATIC

The regulator ground reference is sensed remotely again to compensate for lead resistance, R1016 and R1017 tie the sense leads to the appropriate supply terminals, should these lines become disconnected. Stability is improved by local decoupling capacitors C1002, C1005 and C1006, C1003 provides loop compensation for the error amplifier.

The regulated output is protected against over voltage (nominal 6V) by a crowbar SCR, Q1002. Integrated circuit U1002 senses the high supply voltage via R1014, R1015 and provides drive current to the gate of the SCR when an internal reference voltage is exceeded. C1004 provides a time constant (~ 1ms), for fault duration, before the SCR is triggered.

4.3.1.3 -5 VOLT SUPPLY

The secondary winding 3 is rectified by D1010 and D1011 then smoothed by C1010, and fed to regulator U1010. This is an adjustable monolithic voltage regulator, which has internal thermal shutdown and current limiting. The regulator controls an integral series pass element such that the voltage between OUT and A terminals is held constant at approximately 1.2 volts. Potential divider R1010, R1011 and R1013 provides voltage feedback from the output to the regulator control terminal.

Capacitor C1011 provides local input decoupling, C1012 improves both line and load transient response. C1013 with C1014 decouples the output, and improves output impedance. D1012 protects against reverse voltage transients (possible during power up/down) which could cause a latch up condition if they persisted.

4.3.1.4 +12 VOLT SUPPLIES (From Winding 4)

Two regulators are used to provide the total current of approximately 2 amps drawn at +12 volts.

Supply #2 is essentially similar in operation to the -5V supply described above. Supply #1 tracks supply #2 within ±100mV, and is tied with diodes (D1020, D1021) to always be within ±700mV, during power up/down.

Full wave bridge rectifier BR1020, positive output is smoothed by C1020, and taken to the parallel inputs of U1020 and U1021. C1021 and C1024 decouple these inputs locally to regulators U1020 and U1021. The output of U1020 is returned to the control terminal of the regu-

lator by a resistor chain R1020, R1021 and R1022. The regulator is controlled so that the voltage between the A and OUT terminal is near 1.2V, maintaining the potential across the whole chain at 12V. Regulator U1021 maintains this relationship with the output 1.2V higher than the voltage at the A terminal, connected in parallel with U1020. Capacitors C1023, C1026 for U1020, and C1027 for U1021 lower the output impedance and improve stability, whilst C1022 improves transient response. D1022 and D1023 protect against possible negative voltages at the output.

4.3.1.5 –12 VOLT SUPPLY

The negative output of BR1020 is smoothed by C1030 and applied to regulator U1030 input. The output of this regulator is returned to the control input via a tap on potential divider chain R1032, R1031 and R1030. Input decoupling is provided by C1031, output by C1033 and C1034. The transient response is improved by C1032, and the output protected from voltage reversal by D1030.

4.3.1.6 +24 VOLT SUPPLY

This supply is powered from the +60 volt stabilised supply and regulated with respect to +12 volt supply #2. No adjustment is provided, close tolerance components are used to ensure an output voltage is within ±5% of design.
(see schematic cct. Fig. 4.3.2)

Regulator U1040's internal reference voltage (7.15 volt) at pin 6 is taken via R1044 to the non-inverting input of the regulator error amplifier, pin 5. Resistors R1043 and R1042 between the output and +12 volt, are joined at the inverting input of the amplifier. An integral pass transistor, collector pin 11, emitter 10 is controlled to make the error amplifier inputs equal, and hence the output constant at the voltage determined by the ratio of R1042 and R1043. To improve noise performance the reference is decoupled by C1040, and output response improved by C1042. To reduce dissipation, and hence degredation of load response, the supply applied to the regulator is first pre-regulated by R1041 and zener diode D1040. This method has the added advantage that under fault conditions such as output short circuit, current is limited and the device overall voltage is not exceeded.

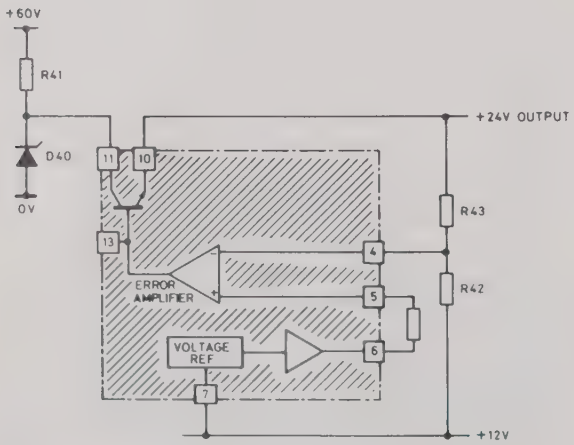


FIG. 4·3·2. +24V SCHEMATIC

4.3.2 HIGH VOLTAGE SUPPLIES

4.3.2.1 +60 VOLT, +120 VOLT, -120 VOLT (Winding 5)

The +60 volt stabilised supply is derived from a half-wave rectifier formed by D1050 and C1052. The diode is fed from the secondary winding of the transformer (5), nominally 55V ac. Conventionally the other end of this winding would be taken to ground, 0 volt. On this circuit the winding is taken to a series regulator, via a rectifier bridge D1055, 56, 57 & 58. The voltage across this regulator element, Q1060 and R1060 is controlled, subtracting from the instantaneous A.C. voltage available to D1050 during conduction. This results in the average D.C. voltage on C1052 being controlled.
(See Fig. 4.3.3 +60 volt schematic).

Operation may be examined by considering the circuit action should the +60 volt output increase. Feedback via R62 raises the base of Q1061, with a consequent increase in emitter current through R1061. Base current in Q1060 will fall, causing a proportional drop in collector current. This current tends to discharge C1060, and less current in Q1060 collector causes the mean voltage across C1060 to increase. Less voltage is now applied to C1052 via D1050 causing the average voltage of the supply to be restored to +60 volts. C1061 and C1062 provide a long time constant on the base of Q1060 to damp fluctuations due to normal ripple voltages on the output rail.

The +120 volt supply is derived from a simple voltage doubler formed by D1052 and D1051 with C1050. C1051 is the reservoir capacitor. As this doubler input voltage is taken from the same a.c. point as the +60 volt supply, stabilisation against input variations is automatically achieved by the +60 volt regulator action. Simi-

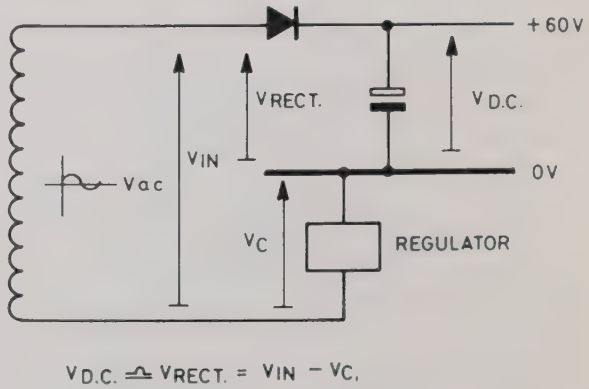


FIG. 4·3·3. +60V SCHEMATIC

larly the -120 volt supply is formed by voltage doubler C1070, D1070, D1071 and C1071. This supply is only very lightly loaded, approx. -10mA, and consequently although the return path is via diode bridge D1055 to 58 it does not interact with the regulator.

4.3.2.2 E.H.T. SUPPLIES (See Fig. 6.16 & Fig. 6.17)

The E.H.T. supplies for the C.R.T. grid, cathode and P.D.A. are derived from +12V and -12V via a 30KHz oscillator. This oscillator consists of transistor Q1103 biased in class C driving transformer T1101. Winding 4–5 provides the positive feedback. From oscillator start up, an increasing class 'C' bias is applied as C1105 is negatively charged through D1105 and R1112. The average charge in C1105 however is controlled by the collector current of Q1102. This transistor thus controls the conduction angle and therefore the output of the oscillator. Q1102 is driven by an error amplifier Q1101 which compares a reference current derived from the +12V supply through R1105, R1106 and R1103 with a current from the -2.2KV output through R1125. The action of the closed loop system is to adjust the -2.2KV output until a current balance is achieved at the base of Q1101.

Should the -2.2KV output become less negative, Q1101 conducts more increasing the base drive to Q1102. This in turn produces a less negative voltage on C1105 increasing the conduction angle of the oscillator and gives a more negative -2.2KV. Similarly if the -2.2KV becomes more negative the system compensates by giving a more negative bias to Q1103. By adjusting the reference current from the +12V supply R1106 acts as a "set E.H.T." control.
Resistors R1101, R1102 and diode D1104 in conjunction with L1101 form a current limiting circuit. If the current through L1101 should increase beyond the normal 250–300mA the voltage drop across it will cause the decoupled +12V supply at the emitter of TR1102 to reduce to the point, determined by the potential divider R1101 and R1102, where D1104 becomes forward biased. The diode shorts the base drive to Q1102. With reduced current drive from Q1102 the oscillator biases itself off so causing an effective current limit.

Pin 6 of the transformer secondary is grounded. Pin 8 drives two voltage multipliers one which supplies the cathode, the other the grid. The cathode multiplier consists of C1114, D1111, D1112 and C1115 acting as a doubler producing –2.3KV at its output across C1115. The 100V zener diode D1114 drops this voltage to –2.2KV which is held constant by the feedback loop. PLF1 feeding the C.R.T. cathode is thus held at –2.2KV.

The grid is supplied from a multiplier consisting of D1107, D1108, C1111 and C1109 and similarly to the cathode supply produces a voltage of –2.3KV at the junction of D1108 and C1111. There can therefore be a maximum of –100V between grid and cathode. R1119 varies this grid bias enabling the C.R.T. to be biased just to cut off. The low end of this multiplier is supplied from the emitter of Q1104. The action of the circuit being to add –2.3KV to the voltage on the emitter of Q1104. The base of Q1104 is driven from the positive going waveform from the bright-up amplifier through, R944. The grid lines on PLF2 thus goes positive turning the C.R.T. on. The fast transistion from the bright-up amplifier is fed via R945 and C945 directly to the grid (Fig. 4.8.1). R1126 supplies the cathode current through the cathode multiplier as well as supplying current to turn on D1115. As cathode current increases at high brightness settings, R1126 can no longer supply it in full. D1115 now turns off and Q1105 turns on. D1116 and Q1105 now act as a limit on the positive excursion of the BRIGHT-UP L.F. signal, restricting grid drive and therefore cathode current which, in turn prevents beam current from damaging the screen phosphor.

A third output from the E.H.T. oscillator is taken from pin 10 of the secondary and applied to a x 6 multiplier module to generate + 14.3KV as a supply for the P.D.A. of the C.R.T.

4.3.3 TUBE CONTROLS

The C.R.T. FOCUS control R3056 is situated on the Y Output and Sampling PCB. It is an element in a voltage divider one end of which is connected to 0V via R3055. The other end is connected through R1124 on the E.H.T. Oscillator PCB to –2.2KV. The wiper of this control can supply from –1.4KV to –1.58KV to the focussing electrode of the C.R.T. (g3).

The Geometry (g6) electrode is taken to the wiper of a potentiometer R1984 on the X Output and Calibrator PCB. This preset has a control range of +100V to –12V. Similarly the Astigmatism voltage which drives (g4) of the C.R.T. is supplied by R1982 on this PCB. The electrode potential is settable from +100V to +45V.

4.3.4 TRACE ROTATION (See Fig. 6.2 & Fig. 6.17)

To facilitate compensation for deflections due to the Earth's magnetic field and for minor misalignment of the deflection plates of the C.R.T. a trace rotation coil is fitted on the neck of the tube. The current through this coil is set by the voltage applied to it from the wiper of R3058, the Trace Rotate preset, via emitter follower Q3050. The coil current can be adjusted through zero when the voltage on the wiper exceeds the voltage on zero D3052 and D3051 conducts. Socket K must be reversed, however, if a large reverse correction current is required. The trace rotate circuitry can be found on the Y Output and Sampling PCB.

4.3.5 SCALE ILLUMINATION

The scale illumination lamps fitted into the plastic moulding around the face of the C.R.T. are supplied from the Y Output and Sampling PCB through plug and socket BB. R3060, the Scale Illumination control via emitter follower Q3051 determines their running voltage and light output. They are 12V lamps running from an unregulated –12 supply, R3059 is therefore necessary to drop the unregulated supply to a maximum of 12V across the lamps.

4.4 Y AMPLIFICATION

4.4.1 ATTENUATORS & PRE-AMPLIFIERS

NOTE: CH1 attenuators, preamplifiers, trigger preamplifiers and logic PCB's are idential to those in CH2. Accordingly only CH1 is described.

CH1 Y input signal is routed through the GROUND switch S11a and S13a AC/DC switch to the high impedance X1, X10 and X100 input attenuators. When the GROUND switch is pressed the signal path is disconnected and the input to the attenuator grounded. When AC coupling is selected S13a switches C53 into the DC signal path. R71, R73, C61, C65 (X10) and R75, R77, C67, C63 (x100) form 1MΩ input resistance attenuators. C69 C71 and C73 set the input capacitance on X1, X10 and X100 respectively to 25pF. The other components in the attenuators are fast rise-time damping components. S9 selects the required attentuation. The high frequency component of the signal passes through C83 and protection circuit consisting of C111, R106, D104, D100 and D107 to the gate of the F.E.T. Q101.

Q101 and Q103 form an impedance converter between the 1MΩ attenuators and the low impedance attenuator consisting of resistor network N83. The Y amplifier input stage is an AC coupled source-follower emmiter-follower stage handling frequencies from 1Hz to 100MHz. It is enclosed in a DC stability loop which handles frequencies from DC to 1Hz.

The input signal is also applied to an inverting amplifier with a 1:1 gain consisting of R93, U101 and R103. The high frequency component of this signal is removed by the integrating action of C102. A voltage comparison is made by U105 between the output of U101 through R194, and the emitter of Q103 through R195, R178 and R193 an error voltage being produced at its output. This error voltage controls the F.E.T. source current (via Q102) and hence the source voltage and Q103 emitter voltage. The DC/low frequency circuit thus forms an accurate closed loop while the high frequency component is supplied as stated previously through C83 to the gate of Q101. R178 is set such that the DC/low frequency gain of the system to the emitter of Q103 is exactly equal to its H.F. gain. R197 corrects for DC offset in IC101, thus acting as the low impedance attenuator balance control.

Processor controlled shift to CH1 is implemented by summing V4 from the Voltage Generator with the input signal at U101 input. This in turn produces a DC offset (or shift) in the output of U101. With zero shift voltage applied and zero input to R93 R179 is adjusted to give zero output from U101.

The output from Q103 emitter drives the low impedance attenuator network N83 which provides the 1–2–5 sequence of gain steps between the X1, X10, X100 steps of the input attenuator. The 2mV/cm range uses the 5mV/cm attenuator settings but the basic amplifier gain is increased by shunting the emitter circuit of dual transistor IC102. The following table shows the complete range switch sequence:-

	FILM NETWORK N83			
INPUT ATTENUATOR	PIN 7	5	4	1
X1	*2mV/5mV	10mV	20mV	
X10	50mV	0.1V	0.2V	
X100	0.5V	1V	2V	5V

*S9df closed.

Q103 also drives positive and negative peak detectors consisting of D101/C115 and D102/C118 respectively. Comparators U501b and U501d are biased to detect levels outside the range +1.6 volts and −1.6 volts (equivalent to ±80cm with S9 set to 20mV/cm), giving a low output (overload CH1) under those conditions. This signal informs the processor that the input amplifier consisting of Q101 and Q103 is about to be overloaded and will thus not maintain DC integrity.

The long tailed pair stage consisting of U102 provides the first stage of amplification and converts from single ended to push-pull drive. R183 sets the 2mV gain with the A.O.T. capacitor C107 adjusting pulse response. R180 is adjusted for DC balance in the 2mV range switching. Gain on all other sensitivity ranges is set by R119 and pulse response achieved by C330. T101 reduces high frequency common mode collector current. This stage current drives the following P–N–P grounded base amplifier. R182 corrects the current balance in the following inverting stage to prevent a DC shift when INVERT is applied. Two differential outputs are taken from Q105 and Q104 collectors, one via R87 and R89 to the trigger amplifier, the other to the following stage of the pre-amplifier.

The balanced modulator stage U103 serves a dual purpose as an inverting switch and as a variable gain control. The upper section consists of two emitter coupled switches driven by the collectors of section a and b of U107. When the CH1 INVERT line is low, the collector of section a of U107 is high with the collector of section b low. U103 sections b and c are therefore turned on with sections a and d off, steering the signal from U103f to pins 13 & 12 of U103 and that from U103e to pins 10 & 9 of that IC. With the CH1 INVERT line high section a and d of U103 are on with section b and c off. The signal from U103f is now directed to pins 10 & 9 of U103 and from U103e to pins 13 & 12 thus inverting the pre-amplifier signal. When R420, Variable Gain, is in the Cal position current is at a maximum through U107d, the voltage between pins 5 and 1 of U107 is therefore at a maximum and the transistor switch is fully in the Normal or Invert mode. As the Variable Gain is turned anti-clockwise however, the off transistors in the switch are turned progressively on. As equal DC currents are added to both sides of the amplifier by this process no

DC offset is produced. This introduces an anti-phase at the switch output reducing the signal (by 2.5:1 when the Variable Gain is fully anti-clockwise). When this control is not in the Cal position S207 on its rear turns D215 on through R203 warning the operator that CH1 is not calibrated. U107e temperature compensates for the base-emitter voltage of 107d.

Transistor U107e provides the DC off voltage for the transistor switch. Preset R181, between the emitter of the lower section of U103 sets the overall calibration of this channel with A.O.T. capacitor C142 controlling its pulse response.

The following grounded base stage U104 sections c and d is current driven from the transistor switch and provides further amplification before the beam switch. Sections a and e convert the Shift Bal. voltage to a differential current which is added into the grounded base emitters. R163 (Shift Bal) balances the DC output of the amplifier at the delay line with the shift voltage input at zero.

4.4.2 Y TRIGGER PRE AMP

A current differential signal is taken through R87 and R89 to the Y Trigger Pre-amplifier PCB and injected into a differential feedback amplifier based on U420. R425 in parallel with R427 and R426 in parallel with R429 act as loads for these currents converting them to voltages. Gain of this stage and DC output level is determined by the ratio of R425 to R427, and R429 to R429. The following stage has its gain defined by R495. R184 (Trig Bal.) sets the voltage at the junction of Q420 collector and Q433 (CH1 Trig I/P) to zero with the trace at the screen centre.

4.4.3 Y PRE AMPLIFIER MONITOR VOLTAGES

Various monitor voltages are provided throughout the Y Pre-amplifier to inform the processor of the state of various front panel controls.

With CH1 Position S201 depressed applying +5V to SKM9, the spinwheel is assigned to CH1 as Shift Control. Likewise with S251 depressed it is assigned to CH2.

OV on PLCV3 indicates that CH1 is DC coupled while OV on PLCV4 indicates that DC coupling has been selected on CH2.

PLCV1 is at OV when CH1 is Ungrounded and PLCV5 at OV when CH2 is Ungrounded.

Uncalibrated gain on CH1 is indicated by +5V on SKM10 on CH2 by +5V on SKN10.

Wafer c of S9 and S10 generate a binary code on SKM and SKN whose value depends on the attenuator settings of CH1 and CH2 respectively. Section section 4.16.

4.4.4 Y BEAM SWITCHES

The four beam-switch inputs, CH1, CH2, TRIG. VIEW and ALPHA are multiplexed to common base amplifiers Q503 and Q504 by the beam switches U503–U506. The beam switches are similar in action, so only CH1 is described in detail.

The beam switch control signal from the display management system is applied to the paired bases of U503 sections a, b, c and d at a differential ECL level. To switch on CH1, pins 1 and 7 of U503 are held at a low level, and pins 8 and 14 high. This allows sections a and d to be active, and b and c are cut off. In this condition, sections e, a and f, d form a differential pair of cascode connected amplifiers, with the analogue signal applied to the bases of c and f.

Emitter components R568, C541, R569 and C542 provide compensation for losses at high frequencies. Preset C534 allows for individual adjustment of CH1 pulse response. The output of the cascode at pins 13 and 9 of U503 is routed via R560 and R563 to the common bus which connects all beam switch outputs to the next amplifier stage (Q503 and Q504 emitters). Note that the tail current of the cascode pair is switched into the bus along with the signal current. When CH1 is switched off, sections b and c of U503 conduct, and a and d are cut off. Since the collectors of b and c are connected together, the differential signal is cancelled. The common mode signal (i.e. the tail currents of sections e and f) passes via R561 to the emitter of Q507, where it is subtracted from the bias current through R522. Thus the current from Q507 via R517 and R516 is reduced by an amount equal to the tail current of the cascode pair. Switching off sections a and d of U503 removes an equal and opposite common mode current from the lines, thus making the nett common mode current independent of beam switching.

The other three beam switches are similar except for the following details:-

1. The TRIG VIEW input has an A.O.T. resistor R599 to adjust the channel gain to approximately equal CH1 and CH2. Preset R582 adjusts the D.C. Offset, so that centre screen corresponds to the actual trigger point.
2. The ALPHA input does not require 100MHz bandwidth, and therefore has no frequency compensating components.

The current output from the beam switches is converted to a voltage signal by common-base amplifiers Q503 and Q504. Q508 acts as a buffer for potential divider R534 and 5, which set the base potential of Q507. A further divider from this point, R562 and R523, set the base potentials of Q503 and Q504.

4.4.5 DELAY LINE DRIVER

The output of Q503/504 drives a differential cascode amplifier based on U502. Section e provides a constant current tail, to improve common mode rejection. C513 provides common adjustment for pulse response of all Y channels, further compensation being provided by the fixed RC networks between emitters.

R541 compensates for the D.C. offsets of all components from the beam switch outputs upto, and including the CRT deflector plates. This control is effectively the ADD

mode balance control as this is the most sensitive indication of when all offsets have been removed.

The collector loads R542 and R543 are shunted by R557 and R590. R542 and R543 are chosen to meet the supply current requirements, while R557 and R590 make the total resistance equal to the characteristic independence of the delay line. Note that R542 and R543 supply both the collector currents of U502c and d, and the emitter current of the common base stage after the delay line.

Also, since the input impedance of the common base stage is lower than R542 and R543, it is mainly the base voltage of Q3001 and Q3002 (Y output and sampling circuit) which controls the operating conditions of U502.

A further output from U502 is taken via R548 and R547 to long-tailed pair Q505 and Q506 to provide the composite trigger output. R556 sets the trigger point to centre screen.

The delay line provides a 90ns delay to allow pre-trigger information to be displayed, and also acts as the signal transmission path from the pre-amp to Y output PCB's.

4.4.6 Y OUTPUT

The delay line output is received by common base amplifiers Q3001 and Q3002. Series resistors R3001 and R3003 raise the emitter impedance to the characteristic impedance of the delay line. At high frequencies, the emitter impedance becomes partly inductive, which is compensated by bypass capacitors C3001 and C3003, so that the delay line is correctly terminated to as high a frequency as possible. Potential divider R3008 and R3007 sets the base voltage of this stage. R3012 and R3013 form the collector loads, while R3009 and R3010 drop the emitter/collector voltage to approximately half the effective supply voltage between the emitters and the junction of R3012 and R3013, to reduce distortion due to thermal effects. C3009 and C3010 bypass these resistors at high frequencies to reduce losses via the base/collector capacitances.

The output of this stage is buffered by emitter followers Q3007 and Q3008 to drive the next Y amplifier stage, and also by emitter followers Q3005 and Q3006 to drive the sampling system.

Common emitter stage Q3003 and Q3004 is driven via base resistors R3036 and R3037, which are bypassed at high frequencies by C3036 and C3037 to reduce losses due to the Miller capacitances of Q3003.and Q3004.

The collector loads of Q3003 and Q3004 are similar to those of Q3001 and Q3002 already described, except for A.O.T. resistor R3042, which adjusts the common mode current into the virtual earth of the next stage, and thus sets up the mean Y plate potential of the C.R.T. The emitter components of Q3003 and Q3004 provide compensation for the effect of the CRT Y plates on the output module.

4.4.7 OUTPUT MODULE

The output of Q3003 and Q3004 is taken to the output module via resistors R36 and R37, which are bypassed by C36 and C37 to reduce high frequency loss into the output capacitance of the previous stage.

The output module, U471 a Mullard OM504 consists of a differential pair of shunt feedback amplifiers driving open collector cascode outputs. To improve the drive capability at high frequencies, the shunting effect of collector load resistors R473 and R474 is relieved by RF chokes L471 and L472. The output of U471 passes via series resistors R38 and R39 to the Y plates of the CRT. The output module requires + 7 volt supply, which is derived locally from the +12V supply via three terminal regulator U3002. R3024 and R3025 form a potential divider on the reference of U3002 to increase its nominal 5V output to 7V. A.O.T. resistor R3025 provides a fine adjustment for the 7V supply. This also sets the virtual earth input potential of the module, which is one Vbe below the 7 volt supply.

4.4.8 TRACE LOCATE

The tail current to the Q3003/Q3004 stage is normally supplied via D3001 and S3001 from the −12V supply. When the trace locate button S3001 is operated, this supply is disconnected, and the tail is supplied via R3039, which does not pass sufficient current to allow the trace to be driven off screen.

4.5 TRIGGER (See Fig. 6.5)

4.5.1 TRIGGER SOURCE SELECTION

Trigger source circuitry and selection switches for both A & B Timebases are mounted on the Trigger Source P.C.B. which is in turn mounted as a 'daughter' board on the Trigger Pre-amp P.C.B. Electrical connection between these boards being made through board mounted plug and socket BJ.

Composite, CH1 and CH2 trigger signals are generated on the Y Pre-amp and are sent via 50Ω co-axial cable to S604, S602 and S605 respectively. The Line trigger signal is derived from a winding on the mains transformer and is fed on co-axial cable through the Power Supply P.C.B. to pins 601 and 602 on the Trigger Source where it is attenuated by R611 and R612. Noise spikes are removed by the action of C612. The External signal from the front panel "A External X/External Trigger" socket is fed through Pin 653 to a 2.5:1 attenuator on Ext X Attenuator on Ext X Attenuator P.C.B. (mounted on the front panel across the A & B External sockets) and via pins 604 and 603 to S601. The above attenuator consists of R601 in series with R602 across C601 as the series element and C602 across R623. (mounted on Trigger Conditioning P.C.B.) as the shunt element. Frequency compensation of attenuator is by adjustment of C602. The B External X/External Trig. signal is similarly attenuated and fed through to S608.

Selection of Timebase A trigger source is by the operation of one of the interlocked switches S602, S603, S604 and S605 which connect CH2, CH1, Composite or Line signals respectively to pin 8 SKBJ. Selecting S602 and S603 together with S601 not selected connects the

External signal from pin 603 to pin 8 of SKBJ giving an External X sensitivity of 50mV/cm. If S601 is now selected the signal is routed through a further ÷ 10 attenuator giving an External X sensitivity of 500mV/cm. The above attenuator consists of series elements R607 and C607 with shunt elements R608, R609, and C608.

When S604 is selected, Pin 5 of PLBJ is grounded, sending a COMP TRIG signal to the system via PLAJ11.

B Trigger source selection is similar to A with S606, S607 and S608 as selection switches. There is no Line or Composite selection for B.

4.5.2 TRIGGER CONDITIONING

The Trigger Conditioning P.C.B. is mounted on the Trigger Pre-amp P.C.B. electrical connections between these boards being through plug and socket BH. The selected A trigger signal is passed from SKBJ2 to SKBH12. Three independent switches S609, S610 and S611 are involved in the signal conditioning. With no switch selected the source is wideband A.C. coupled through capacitor C623. Selecting S611 directly couples the signal through the switches from SKBH12 to SKBH13. When A.C. L.F. Reject is selected by S610 a smaller capacitor C622 is inserted into the signal path to act as an L.F. Filter. On selecting A.C. H.F. REJ. with S609, R624 is introduced into the signal path and along with C694 acts as an H.F. filter.

B Trigger conditioning is similar to A but does not have A.C. H.F Reject.

A & B Slope switches and Level controls are also mounted on this P.C.B. but are dealt with in section 4.5.3. The 0 to -12V Var Hold Off voltage from the wiper of R620 is passed from SKBH10 to PLAJ5.

D601 and D603 in series are connected between the A signal out on SKTBH13 and the -12V rail. This arrangement protects the input F.E.T. Q701 on Trigger Pre-amp P.C.B. from overload in the negative direction. The B channel is similarly protected by D602 and D604.

4.5.3 TRIGGER AMPLIFIER

The trigger circuit is required to produce a fast positive going signal at the output whenver the selected input signal crosses a voltage set by the Level control in a direction set by the Slope switch. The Schmitt trigger maintains a fast output edge eliminating uncertainty on a slow moving signal.

The input to the A Trigger Amplifier is through Pin 13 of PLBH. The first stage is formed by a dual F.E.T. in a D.I.L. package Q701/Q702. Q701 acts as a source follower, its running current being determined by a matched transistor Q702. As they are matched devices running at the same current their gate to source voltages will be the same. The voltage between gate of Q701 and the base of Q703 will therefore be zero as the voltage between the base of Q702 and the lower end of R705 is zero and R703 is equal to R705 in value. The signal applied to the gate of Q701 is limited in the negative direction by D601 in series with D603 and in the positive direction the breakdown of its gate to drain junction diode.

Q703 is an emitter follower driving both the base of Q705 and the emitter of Q714.

Q714 and Q715 form a feedback amplifier whose output gives an EXT X O/P on PLAJ7 to be used as an External X or an X-Y signal source. The gain of the amplifier is determined by the ratio of R713 to R714 + R715 with the gain being set by R715. R712 generates a separate current drain through R713 to offset the output at Q715 emitter to +2V. The A.O.T. capacitor C709 is selected to give the correct X-Y pulse response. The gain of this amplifier when set is approximately 2.

When the X-Y function is not in use an EXT X INHIBIT signal is applied through PLAJ9 to R772 turning Q713 off. This turns D703 on and the current through R718 bottoms Q715 and cuts-off Q714 thus preventing any output from the amplifier. With Q714 cut-off R711 tail current will flow through R703.

During trigger operation the signal is applied to the base of Q705 which forms a long-tailed amplifier with Q706. The base of Q706 is driven from the A Trig Level Control R625 through diode-connected Q704 which compensates for the base emitter voltage of Q703. The incoming trigger signal is thus compared against the voltage level set by this control. R720, "A Trig Bal", balances the amplifier when the A Level Control is centralised. The gain of the stage is determined by R735 and frequency compensation provided by C735, R736 and C736. When in X-Y operation, the EXT X Inhibit signal on PLAJ9 is low and turns on Q716. The tail current provided by R738 is removed and stage Q705/Q706 is cut-off, preventing the Trigger amplifier from interfering with the Ext X signal at the emitter of Q703.

The trigger signal is now passed from the collectors of Q705 and Q706 through emitter followers Q707 and Q708 to drive the Trig-View output on PLBM and the bases of Q709 and Q710. When Trigger View is not being used, the Inhib. Trig. View signal on Pin 10 PLAJ11 is high turning Q717 off and permitting the current through R732 to turn on D704 and D705 short circuiting the Trig. View signal path.

Q709 and Q710 form a differential amplifier with gain determined by R745 and R750 and frequency compensated by C745. The next stage is a further differential amplifier consisting of Q711 and Q712. Its gain is defined by R757 and R760 frequency compensation being provided by C758. With the amplifier balanced, the transistor Q712 is biased such that its collector is at the 3.9V Emitter Coupled Logic threshold level of U701. Section c of E.C.L. line receiver package U701 is employed as the Schmitt trigger in the trigger system.

The trigger signal is applied to the non-inverting input

of section c. The inverting input is supplied through R764 with the 3.9V threshold voltage from the Vbb on Pin 11 of the I.C. The degree of hysterisis applied to the Schmitt is determined by the ratio of R762 to R764 and the output voltage on Pin 14.

The output from Pin 15 is applied to the non-inverting input of U701a and U701b. As a positive transition at 'A' Trig O/P initiates the Timebase, U701b is used to detect negative trigger slopes while U701a detects positive going ones. When the A Trigger Slope Switch S612 on the Trigger Conditioning P.C.B. is set to positive, Pin 9 on SKBH is disconnected. The potential divider action of R771, R770, R769 and R768 sets Pin 10 low disabling U701b. These resistors also set the potential of Pin 5 to the E.C.L. threshold voltage. The output Pin 2 is therefore low until a positive going edge on Pin 4 crosses the threshold sending the output high. On switching the A Trigger Slope Switch to negative, +5V is connected to the junction of R770 and R769. This sets Pin 5 high disabling U701a while placing the E.C.L. threshold voltage on Pin 10. Output Pin 7 is therefore low until a negative transition on Pin 9 crosses the threshold to send it high.

The trigger amplifier for the B Timebase is similar in operation to that of A. There are, however, no Ext X or Trig. View outputs.

4.5.4 TRIGGER DETECTOR

When the circuit consisting of Q780, Q781, Q782 and Q783 detects trigger pulses at the 'A' Trig O/P it switches the timebase from the free-run to the triggered mode and lights the Triggered L.E.D.

Refer to the waveform diagram Fig. 4.5.1. 'A' trigger pulses on being differentiated by C780 and amplified by Q780 are a.c. coupled to a diode detector circuit consisting of D508 and D509 with bias provided by D510. The remaining negative transition is coupled via D508 to the monostable Q781 and Q782. In the absence of an input, both transistors are cut-off. A single trigger pulse will turn both Q781 and Q782 rapidly on due to regeneration. Q782 discharges C783 and C784 through D784. Should no further trigger pulses occur, Q781 turns off and C783 and C784 proceed to recharge through D783 and R792. The voltage on Q781 collector, Q782 base and Q782 emitter drops as the capacitors change. This process continues for about 30 ms until the emitter of Q782 reaches -6.5V when all the current supplied by R796 is removed through R795. Q783 now turns off, free running the timebase (Auto Trig Line high) and switching off the Triggered L.E.D. A succession of trigger signals above approximately 40Hz will maintain Q782 emitter above -6.2 Volts. Q783 will therefore be on, lighting the Triggered L.E.D. and preventing the timebase from running (Auto Trig line low).

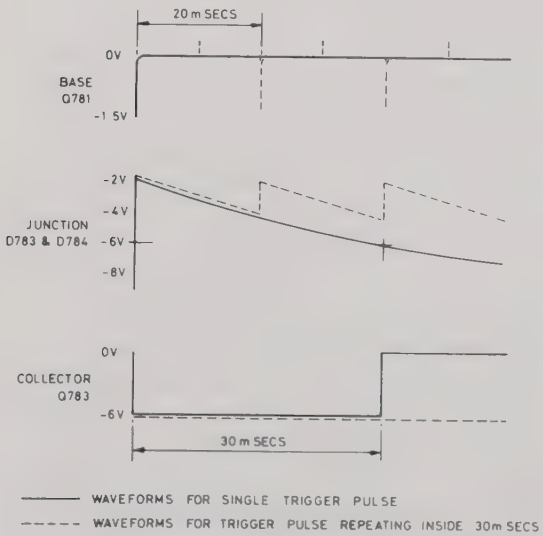


Fig. 4.5.1 Trigger Detector Operation

4.6 DELAY AND TIME/EVENT MEASUREMENT SYSTEM

4.6.1 BLOCK DIAGRAM AND GENERAL OVERVIEW

Fig. 4.6.1 shows the block diagram of the Delay System. The prescaler, start/stop control logic and associated processor interface are part of the Timebase Assembly (with component prefix 1500), while the 16 bit TTL counter and remaining processor interface are part of the CPU PCB, (component prefix 2000).

The delay System counter is divided into three distinct sections: Prescaler; 16 bit TTL counter; 16 bit software counter. The table below shows which sections are used for the three count lengths.

MODE	RANGE OF N COVERED BY		
	PRESCALER ONLY	PRESCALER + TTL COUNTER	ALL 3 SECTIONS
Divide	N<17	16<N<524297	N>524296
Delay	N<16	15<N<524296	N>524295

Note that for some modes with N = 0, 1 the delay system counter may not be used at all – see Tables in Figures 4.6.3, 4.6.4 and later descriptions. The value N referred to is the actual count length (in clocks) required of the delay system counter and thus where for example a time delay is required, N becomes so many cycles of the 100MHz clock frequency. For example if T = 320ns then N = 320/10 = 32. The prescaler although basically 4 bit provides only an effective 3 bits when used with the TTl counter.

The counter always decrements, i.e. to count N, the counter is parallel loaded (by the processor) with N and clocked until it reaches zero. The counter may be configured to aprallel load itself when zero is reached. When the TTl counter reaches zero, $\overline{\text{LONG CARRY}}$ is produced and this allows the next

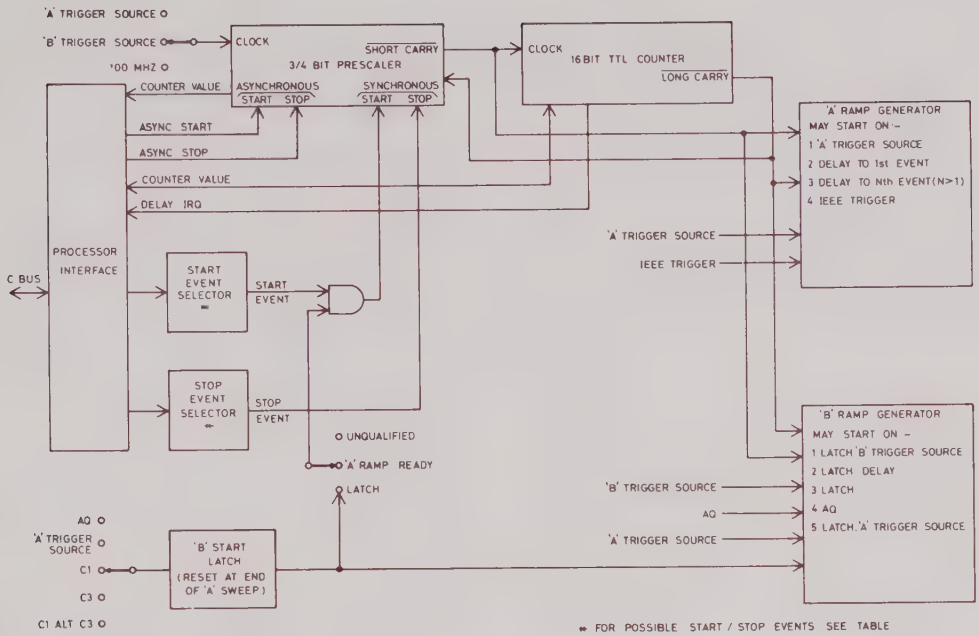


Fig. 4.6.1 Delay System Block Diagram

START/STOP EVENT	COMMENT
'A' TRIGGER SOURCE	Actual output from 'A' trigger amplifier
'B' TRIGGER SOURCE	Actual output from 'B' trigger amplifier
AQ	High to indicate 'A' ramp running
BQ	High to indicate 'B' ramp running
$\overline{AQ}$	Used to detect end of 'A' sweep
STOP ON N	High when delay counter reaches zero
C1	Basic cursor comparator output
C2	" "
C3	" "
C4	" "
C2.B1	Cursor 2 in B1 sweep only
C4.B3	Cursor 4 in B3 sweep only
C1 ALT C3	C1 and C3 when both B1 and B3 are selected
BQ.Φ1	BQ of B1 sweep only
BQ.Φ2	BQ of B3 sweep only
IEEE TRIGGER	IEEE Group Execute Trigger

Fig. 4.6.2 Possible Delay System Start/Stop Events

MODE	START EVENT	START QUALIFIER	CLOCK	STOP EVENT	'A' RAMP STARTS ON
Trigger 12 & 21 T>0	'A' TRIG	'A' RAMP READY	100MHz	STOP ON N	'A' TRIG DELAYED BY N>1
" 12 & 22 N=1	'A' TRIG	'A' RAMP READY	'B' TRIG	AQ	'A' TRIG DELAYED BY N=1
" 12 & 22 N>1	'A' TRIG	'A' RAMP READY	'B' TRIG	STOP ON N	'A' TRIG DELAYED BY N>1
" 12 & 23 N>1	ASYNC	–	'A' TRIG		'A' TRIG DELAYED BY N>1
" 12 & 24 N>1	ASYNC	–	100MHz	–	'A' TRIG DELAYED BY N>1
"STOPWATCH"MODE	AQ or BQ			C1,C2,C3orC4	
	BQ.Φ1 or BQ.Φ2	NONE	100MHz or 'B'TRIG	C2.B1orC4.B3	

Fig. 4.6.3 Delay System Parameters for 'A' Delay Modes and 'Stopwatch' Modes

TRIGGER MODE	'B' RAMP STARTS ON	LATCH* SET BY	START EVENT	START QUALIFIER	CLOCK	STOP EVENT
13	LATCH	C1,C3 or C1 ALT C3	–	–	–	
14	LATCH.BTRIG	C1,C3 or C1 ALT C3	–	–	–	
15,31 N=0 T=0	USES MODE 18					
15,31 N=1	USES MODE 17					
15,31 N>1 T>0	LATCH	END OF DELAY	AQ	NONE	BTRIG or 100MHz	STOP ON N
15,32 N=0 T=0	USES MODE 17					
15,32 N=1	LATCH	END OF DELAY	AQ	NONE	BTRIG or 100MHz	STOP ON N
15,32 N>1 T>0	LATCH.DELAY	AQ	BTRIG	LATCH	BTRIG or 100MHz	STOP ON N
15,33 N=0 T=0	USES MODE 13					
15,33 N=1	USES MODE 14					
15,33 N>1 T>0	LATCH	END OF DELAY	C1,C3 or C1 ALT C3	NONE	BTRIG or 100MHz	STOP ON N
15,34 N=0 T=0	USES MODE 14					
15,34 N=1	LATCH	END OF DELAY	C1,C3 or C1 ALT C3	NONE	BTRIG or 100MHz	STOP ON N
15,34 N>1 T>0	LATCH. DELAY	C1,C3 or C1 ALT C3	BTRIG	LATCH	BTRIG or 100MHz	STOP ON N
15,35 N>1 T>0	LATCH.DELAY	AQ	ATRIG	LATCH	BTRIG or 100MHz	STOP ON N
15,36 N>1 T>0	LATCH. DELAY	C1,C3 or C1 ALT C3	ATRIG	LATCH	BTRIG or 100MHz	STOP ON N
15,39 N=1	LATCH. BTRIG	AQ	–	–	–	–
15,39 N>1	LATCH. DELAY	AQ	ASYNC	–	BTRIG	–
16,31 N=0 T=0	USES MODE 17					
16,31 N=1	LATCH	END OF DELAY	AQ	NONE	BTRIG or 100MHz	STOP ON N
16,31 N>1 T>0	LATCH. BTRIG	END OF DELAY	AQ	NONE	BTRIG or 100MHz	STOP ON N
16,33 N=0 T=0	USES MODE 14					
16,33 N=1	LATCH	END OF DELAY	C1,C3 or C1 ALT C3	NONE	BTRIG or 100MHz	STOP ON N
16,33 N>1 T>0	LATCH. BTRIG	END OF DELAY	C1,C3 or C1 ALT C3	NONE	BTRIG or 100MHz	STOP ON N
16,39 N=1	LATCH. BTRIG	AQ	–	–	–	
16,39 N>1	LATCH. DELAY	AQ	ASYNC		BTRIG	
17	LATCH. BTRIG	AQ		–		–
18	LATCH	AQ	–	–	–	–
19,31 N>1 T>0	LATCH DELAY	C1,C3 or C1 ALT C3	AQ	NONE	BTRIG or 100MHz	STOP ON N
19,33 N=0 T=0	USES MODE 13					
19,33 N=1	USES MODE 14					
19,33 N>1 T>0	LATCH	END OF DELAY	C1,C3 or C1 ALT C3	NONE	BTRIG or 100MHz	STOP ON N
19,39 N=1	LATCH. BTRIG	C1,C3 or C1 ALT C3	–	–	–	–
19,39 N>1	LATCH. DELAY	C1,C3 or C1 ALT C3	ASYNC	–	BTRIG	STOP ON N

* B START LATCH

Fig. 4.6.4 Delay System Parameters for 'B' Delay Modes

occurrance of $\overline{\text{SHORT CARRY}}$ (produced by the prescaler) to produce overall terminal count (zero).

In divide modes (for example "A Starts Every Nth "A" TRIGGER") the processor parallel loads N into the counter, sets the clock source accordingly (say 'A' Trigger Source) and asserts ASYNC START. The counter counts down through N clocks to reach zero when it produces both $\overline{\text{LONG CARRY}}$ and $\overline{\text{SHORT CARRY}}$ as an output (to start 'A' timebase say). Additionally the counter automatically parallel loads itself with N (held statically in port latches) so that counting may be continuous.

In delay modes, the processor once again parallel loads the counter with N but the counter only starts when a particular programmable start event occurs (but subject to the programmable START QUALIFIER – see Fig. 4.6.1 and Figures 4.6.3, 4.6.4). When the counter reaches zero it parallel loads itself but does not start counting until the start even occurs again. The start events used are shown in Table 4.6.2. (Not all start events are used in delay modes).

In 'stopwatch' mode (current cursor time) the whole counter is parallel loaded with maximum count by the processor, which also sets the start event as AQ or BQ (see Figure 4.6.2) and the current cursor as the stop event. It then arms a single shot circuit to allow counting between the two events. When complete, the counter stops (does not automatically parallel load) and the processor reads the value left in the counter. This value is subtracted from maximum count to produce the value for conversion and display. The start/stop events are again taken from Figure 4.6.2.

Trigger modes for 'A' timebase start are summarised in Figure 4.6.3 whilst those for 'B' timebase appear in Figure 4.6.4. The details of these modes will be further discussed in later descriptions.

4.6.2 GENERAL LOGIC

100MHz CRYSTAL CLOCK GENERATOR

The 100 MHz oscillator is formed around Q1540 and is a crystal controlled grounded base configuration with L1541 C1542 and C1543 forming the tank circuit. XL1501 is actually a fifth overtone 20MHz crystal and L1542, R1541 are included to ensure oscillation at the 100MHz overtone. L1541 may be adjusted so that the tank circuit resonant frequency is that of the crystal, whereupon optimum output amplitude is obtained. The 100MHz signal at Q1540 collector is coupled into amplifier U1591c via C1541. U1591c is an ECL line receiver biased for linear operation, with sufficient gain to ensure correct logic levels at its output. Its 'complement' input is fixed at Vbb. Vbb is also supplied to the 'true' input along with the 100MHz oscillator signal.

CLOCK SELECTION CIRCUITRY

U1596 allows the processor to program the delay system clock as 100MHz, 'A' trigger or 'B' trigger. Bits Do, D1, D2 of Port U1570 determine which clock source is selected and the processor ensures that only one bit is low at a time. The input to gate e is the WIRE-OR function of the outputs of gates a, b, d so that only that gate selected will drive this point. D1571, 2, 3 form simple CMOS/ECL interfaces.

U1596e passes the selected clock to the remainder of the delay system and is included as a line driver.

PRESCALER COUNTER

The prescaler counter (U1583) is a fully synchronous 4 stage counter. When $\overline{C}$ is low the counter counts down (S2, the up/$\overline{\text{down}}$ control input is internally pulled low) assuming that S1 (parallel load control) is high. When S1 is low, C is ignored and data is loaded from the D inputs.

TTL COUNTER AND INTERFACE

The clock for the TTL counter is obtained from monostable U1587b. When this is clocked by the prescaler logic, its Q output goes low, $\overline{Q}$ goes high. The set input rises towards the ECL logic high level of $\overline{Q}$ with a time constant determined by R1584 and C1574. When approx. 30ns has elapsed, Q will start to rise as S takes effect. Positive feedback via C1573 couples this change into the S input to produce a clean back edge to the pulses at Q and $\overline{Q}$.

The 30ns pulse clocks the TTL counter via line receiver U2019a and common-base switch Q2060.

The 16 bit TTL counter is formed from U2063, 4, 5, 6 which are fully synchronous and connected for count-down operation.

When all 16 bits of the counter reach zero, all four TC outputs go low and U2059b output goes high since all three outputs of U2058a, b, d will then be low. The effect of this depends on the logic of write port U2049, U2062 and U2058c, U2059c. If O3 at U2049 is high, the processor has allowed a DELAY IRQ to occur via U2062a when count zero is reached. The processor may cancel this interrupt by taking U2049 O3 low to reset U2062a. If left low this will prevent a further DELAY IRQ occurring. (As in counts less of then 16).

For counts involving only the prescaler the latter requires that $\overline{\text{LONG CARRY}}$ be held permanently low. This is achieved by the processor leaving U2049 Oo high and O1 low. U2062b is thus reset with Q low and U2058c output is low since that of U2059c is low. The processor also leaves O7 high to enable U2019c to pass the logic low from U2058c output (via U2019b) to $\overline{\text{LONG CARRY}}$ and thus back to the prescaler. Hence the TTL counter is eliminated.

To enable automatic parallel load the processor holds U2049 Oo and O1 low. This resets U2062b and allows the terminal count output of U2059b to pass through U2059c and U2058c. This takes the $\overline{\text{PE}}$ input of all counters low to load data from write only ports U2060, 1.

At any time the processor may force the counters to parallel load by holding O1 low and pulsing Oo high. This has the same effect as terminal count.

To prevent automatic parallel load the processor holds O2 low which sets U2062b and holds $\overline{PE}$ high via U2058c.

Normally when $\overline{PE}$ occurs, $\overline{LONG\ CARRY}$ occurs by virtue of line drivers U2019b, c. However under some conditions, the processor requires $\overline{PE}$ to occur without $\overline{LONG\ CARRY}$. When U204907 is high, D2090 is cut off leaving U2019c 'complement' input at Vbb and $\overline{LONG\ CARRY}$ will occur. When O7 is low, D2090 conducts and pulls U2019c input below the ECL logic low threshold. This holds $\overline{LONG\ CARRY}$ high. $\overline{LONG\ CARRY}$ returns to the prescaler via line receiver U1591b.

START/STOP CONTROL & PRESCALER COUNTER

The TTL and software sections of the counter can only change state in response to the prescaler output and so the Start/Stop Control logic need only control the prescaler.

For many modes $\overline{MODE\ 3}$ is high (see later descriptions) and U1583 C is controlled by U1584a Q, which in turn follows U1585a Q re-timed by a clock pulse. U1585a along with U1581 and U1582 form a toggling system to select the START or STOP event as the clock input to U1585a as appropriate. U1585a is thus the Start/Stop Control bistable and its Q output is low to enable counting. The clock input of this bistable is the START/STOP EVENT as selected by the 16 line to 1 line multiplexer formed by U1581 and U1582.

Port U1571 contains the 4 bit codes for the required Start and Stop events. (Detailed in Fig. 4.6.5).

	U1571 OUTPUTS				
	D3	D2	D1	D0	START
EVENT*	D7	D6	D5	D4	STOP
BQ.Φ2	0	0	0	0	
BQ.Φ1	0	0	0	1	
C4.B3	0	0	1	0	
C2.B1	0	0	1	1	
IEEE TRIGGER	0	1	0	0	
AQ	0	1	0	1	
BQ	0	1	1	0	
AQ	0	1	1	1	
STOP ON N	1	0	0	0	
'B' TRIGGER	1	0	0	1	
'A' TRIGGER	1	0	1	0	
C4	1	0	1	1	
C3	1	1	0	0	
C2	1	1	0	1	
C1	1	1	1	0	
C1 ALT C3	1	1	1	1	

* See description in Fig. 4.6.2

Fig. 4.6.5 Start/Stop Event Truth Table

Which of these bit groups (i.e. Start or Stop event) appears at the outputs of Quad 2 line to 1 line multiplexer U1580 depends on the state of U1585a. When $\overline{Q}$ is low (counter stopped) U1580 passes the Start event through to its outputs. When U1580 Qd is low, U1599e 'true' output is low and U1582 is enabled. Similarly, U1597e 'complement' output is high disabling U1581. The Qa, Qb, Qc outputs of U1580 select the Start/Stop event from the particular multiplexer enabled.

Potential Start events may still be blocked by the programmable START $\overline{QUALIFIER}$ whose function depends on specific mode and is generated by the logic of U1599a, b, d and U1597d. A full description will be found in section 4.6.4.

The timing of the Start/Stop circuitry under typical conditions, shown in Fig. 4.6.6 will now be discussed. Starting with the counter not running, U1585a $\overline{Q}$ is low selecting the start event from U1581, 2. A start event occurs but since START $\overline{QUALIFIER}$ is high U1585a D is high and the bistable does not change state. When the start event is qualified (at A) it clocks U1585a $\overline{Q}$ high so that CLOCK 6 takes U1583 $\overline{C}$ low to enable counting. Feedback from U1585 $\overline{Q}$ to D via U1598e is provided so that when the stop event occurs, U1585a is clocked back to the 'stop' state. However, this feedback is delayed by about 7ns by R1580 and C1570 so that the transition glitch caused by changing the status of U1580, 1, 2 is not construed as a stop event. Any clocks at U1585a during this time will merely clock it into its existing state.

When the stop event does occur U1585a $\overline{Q}$ returns low and CLOCK 14 disables U1583 from further counting.

Certain start/stop events require additional logic for their production and are detailed below.

The Q4 and $\overline{Q4}$ outputs of U1616 (Cursor Management) define the current B sweep phase when the instrument operates with both B1 and B3 enabled. Under these conditions Φ1 is low for B1 sweep and Φ2 low for B3 sweep (See section 4.9).

The event BQ.Φ1 (see Table 4.6.2) is generated by U1579. When both Φ1 and $\overline{BQ}$ are low the output of this gate is high. Similarly, U1597d produces BQ.Φ2 when both Φ2 and $\overline{BQ}$ are low.

The event C2.B1 is generated by U1579b. When both C2 and Φ1 are low, the output of this gate is high. Similarly, U1579a produces C4.B3 when both C4 and Φ2 are low.

The WIRE-OR connected gates U1597a, b produce the event C1 ALT C3. These gates produce C1 during B1 phase and C3 during B3 phase only. See Figure 4.6.7.

'A' & 'B' RAMP TRIGGER SELECTORS

U1578 controls trigger selectors U1593, 4 whose outputs drive the trigger inputs of 'A' and 'B' timebase ramp generators. At any time only one OR gate of each device

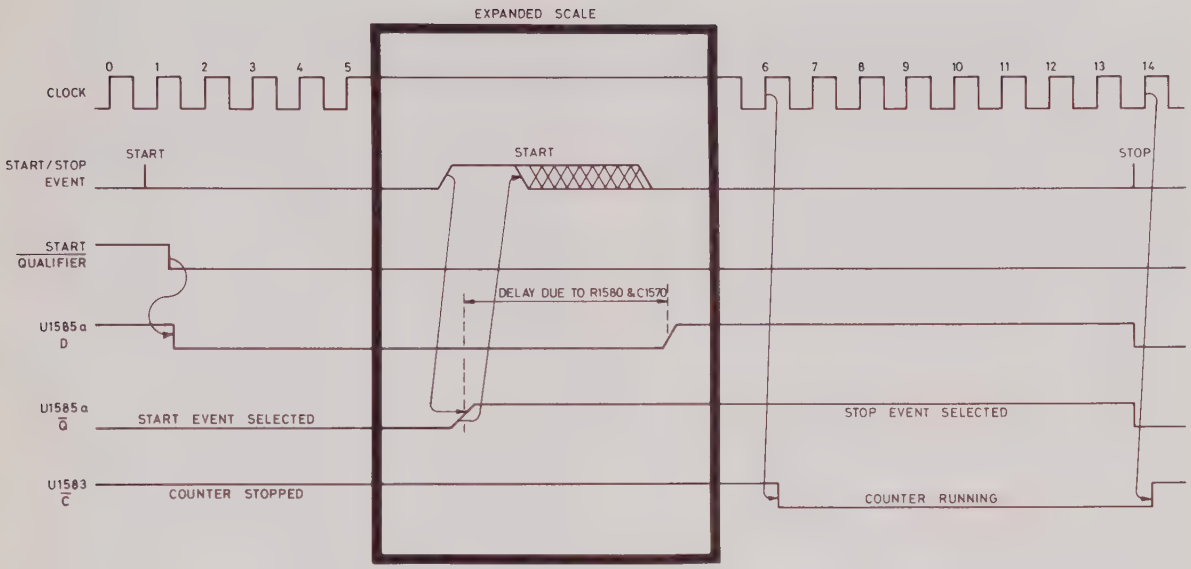


Fig. 4.6.6 Start/Stop Control Timing

C1	C3	Φ1	Φ2	C1 ALT C3
0	0	0	1	1
0	0	1	0	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

Figure 4.6.7 Truth Table for production of C1 ALT C3 Event

will be enabled so that the trigger output function is that of the selected OR gate inputs. For example if 'A' ramp is to start at the end of delay and the count N is >1, the processor will take $\overline{\text{SELECT}}$ 'A' TRIG DELAYED BY N>1 (Q2 of U1578) low so that when the whole counter reaches zero, $\overline{\text{SHORT CARRY}}$ and $\overline{\text{LONG CARRY}}$ go low and U1593 'complement' output goes high to trigger 'A' timebase.

Note that 'A', 'B' and IEEE trigger inputs are received with line receivers U1592a,c,d.

'B' START LATCH

This latch, referred to in Fig. 4.6.1 is actually U1610a (Cursor Management). The output of this latch may be used as one method of starting 'B' timebase, and may be 'set' by a combination of cursors via part of selector U1606, by end of delay via the remainder of U1606, or by AQ (indicating 'A Start'). The latch is always reset at the end of A sweep. The particular 'set' event is programmed by the processor via write only port U1624.

If the latch is to be 'set' by C1 or C3 (Single B Start) then D4 or D5 will be left low by the processor, to enable C1 or C3 to clock U1610a. At the end of 'A' sweep, AQ goes high on U1610a S input forcing Q low until the next 'A' sweep.

If the latch is to be set by C1 ALT C3 (C1 during B1 phase and C3 during B3 phase when both B1 and B3 are enabled), then U1624 D4 and D5 are left low, and D1 (DUAL B START) high by processer. U1606 combines both C1 and C3 signals with Ø1 and Ø2 from timebase phase register U1616 to produce C1 ALT C3 to clock U1610a. For truth table see Figure 4.6.7.

If the latch is to be 'set' by the 'End Of Delay' then $\overline{\text{ENABLE}}$ DELAY B START will be set low by the processor so that when both $\overline{\text{LONG CARRY}}$ and $\overline{\text{SHORT CARRY}}$ are low (at end of delay), U1606 pin 3 goes high clocking U1610a.

If the latch is to be set by start of 'A' sweep (AQ), D7 of U1624 will be set low. When AQ goes low U1610a S input goes low and R input high shortly after due to U1601c being enabled. This allows AQ to start B timebase with the minimum of gate delays.

PRESCALER LOADING

The prescaler counting loop consists of the fully synchronous 4 stage counter U1583; U1595a and U1584b.

To load the prescaler, the processor places the required 4 bit code on bits Do, D1, D2, D3 of U1576 ('N DATA' lines). U1586a has Q low and Q high as its normal state (see description of operation in 'Divide' mode) and so the

four gates of U1588 are enabled to pass NDATA through to following circuitry. The processor also asserts FORCE S1 and MODE1 (U1572) so that U1587a is reset with Q low enabling gates U1590 to present NDATA to U1583. As will be seen later D1 and D2 of this data are inverted by U1590b, d so that when U1587a Q is high a particular value may be automatically loaded by hardware. To compensate for this, bits D1 and D2 of NDATA are written inverted into U1576 by the processor.

With FORCE S1 high, U1584b $\overline{Q}$ is low and parallel load occurs with the next clock pulse (the clock source is set as 100MHz by the processor).

For counts that involve both the TTL counter and prescaler, the latter cycles with a count of 8 clocks but has a different length for its first count. This is compensated for by the processor when loading the counter.

To allow counting to commence in this mode, the processor takes both FORCE S1 and MODE $1/\overline{2}$ low.

4.6.3 DIVIDE-BY-N MODE OPERATION

This description covers the trigger modes: "A starts every Nth A trig (÷N)" (Trigger Mode selections 12 and 23); "A starts every T secs (clock)" (selections 12 and 24); "Delay to next of B trig ÷ N" (every mode using selection 39).

The parameter 'N' refers to the delay system division ratio and where time 'T' is involved the value of N represents a number of 100MHz clock cycles (10ns). For example if T = 320ns then N = 320/10 = 32.

The processor configures the Clock Selection Circuitry for the required clock (see Figures 4.6.3, 4.6.4 and section 4.6.2) and asserts ASYNC START (U1570 Q6). This resets bistables U1584a, U1585a so that U1583 C (low to enable counting) is held low, allowing the counter to free-run.

As will be seen, two clock cycles are required to generate $\overline{\text{SHORT CARRY}}$ and to parallel load the prescaler and thus the counter of the latter is loaded with two less than N.

OPERATION WHEN N<17

For the trivial case N = 1 the delay system is not used but direct trigger routing is selected.

When 1<N<17 only the prescaler is employed and Fig. 4.6.8 shows timing when N = 10.

Mode $1/\overline{2}$ is set high by the processor (U1572 Q3) so that U1587a is reset and each OR gate of U1590 is enabled to pass N DATA (8) from Qo-Q3 of U1576 to the parallel load inputs Do-D3 of counter U1583. (U1586a will be in its normal state with Q high, $\overline{Q}$ low disabling U1589 gates and enabling those of U1588).

Each clock decrements the count by one until Qo-Q3 are all low when U1595 pin 14 goes high. Clock 8 takes U1584b $\overline{Q}$ ($\overline{\text{SHORT CARRY}}$) low and since U1583 S1 input (parallel load control) will be low, clock 9 causes parallel load of the value 8 into the counter ready for the next count. It will thus be seen that there is one $\overline{\text{SHORT CARRY}}$ pulse for every (8+2) = 10 clocks.

OPERATION WHEN N>16

These counts involve both the TTL counter and prescaler and timing for N = 21 is shown in Fig. 4.6.9.

Prescaler operation is similar to that for N<17 with U1595 pin 14 going high at count 0 and $\overline{\text{SHORT CARRY}}$ occurring with the following clock. The difference is that (as described in section 4.6.2) MODE $1/\overline{2}$ is low and so when $\overline{\text{LONG CARRY}}$ is low the prescaler parallel loads with data from NDATA held in U1576 (value 11), but when high the data loaded is fixed at value 6, for a prescaler count of 8.

Since division mode is selected, $\overline{\text{STOPWATCH MODE}}$ is high and the 2 line to 1 line selector formed by U1577 passes $\overline{\text{SHORT CARRY}}$ to clock (positive going edge) monostable U1587b which clocks the TTL counter (see section 4.6.2).

Fig. 4.6.12 shows that the 'Delay System Output' occurs only when both $\overline{\text{LONG CARRY}}$ and $\overline{\text{SHORT CARRY}}$ are low. This represents the combination of these two signals at U1593, U1594 or U1606 but is functionally identical to the signal at U1565d output (LC.SC).

Since $\overline{\text{LONG CARRY}}$ is valid considerably earlier than $\overline{\text{SHORT CARRY}}$, the system timing is defined entirely by the fast logic $\overline{\text{SHORT CARRY}}$. A similar property exists for the 'carry' from the software count – see section 4.6.7.

4.6.3.1 PHASE SHIFT CONTROL

To achieve phase shift control, on command of the processor, the division ratio is changed by one for just one count cycle. For example if N = 7 and phase advance is required then N will be increased to 8 for one count cycle. Similarly for phase retard N will be reduced to 6 for one count cycle.

Phase advance operation when N = 7 is illustrated in Fig. 4.6.10. The processor loads 5 into N DATA (U1576 Qo-Q3) and one more than this, 6, into AUX DATA. (For phase retard the processor would load 4 into AUX DATA). A single shot circuit, on the command of the processor, allows AUX DATA rather than N DATA to be loaded into the prescaler counter.

The choice of N DATA or AUX DATA is under the direct control of bistable U1586a. Normally Q is high and the NOR gates of U1589 are disabled. Q low enables those of U1588 to pass N DATA to the parallel load inputs of U1583. When Q is low, AUX DATA passes through rather than NDATA. U1586a is in turn controlled by the single shot circuit formed by U1586b, U1565a, b and associated components.

When $\overline{\text{PHASE SHIFT}}$ is high (U1570 Q5), U1586b Q will be high (due to a previous phase shift sequence, say) and so the rising edge of $\overline{\text{SHORT CARRY}}$ merely clocks U1586a Q high to allow parallel loading of N DATA. With U1586b in this state U1565b is disabled and U1565a (WIRE-OR connected with U1565b to produce the clock for U1586b) is enabled.

Thus when phase shift is required, the processor takes

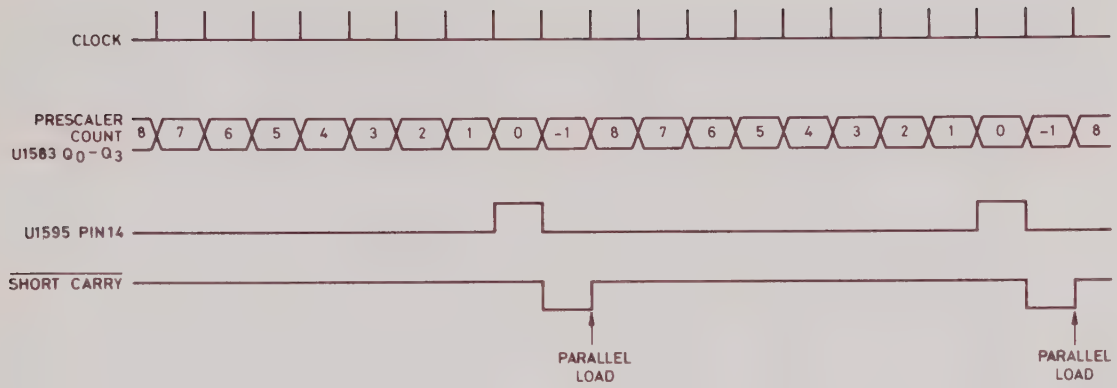


Fig. 4.6.8 Divide Mode Timing when N = 10

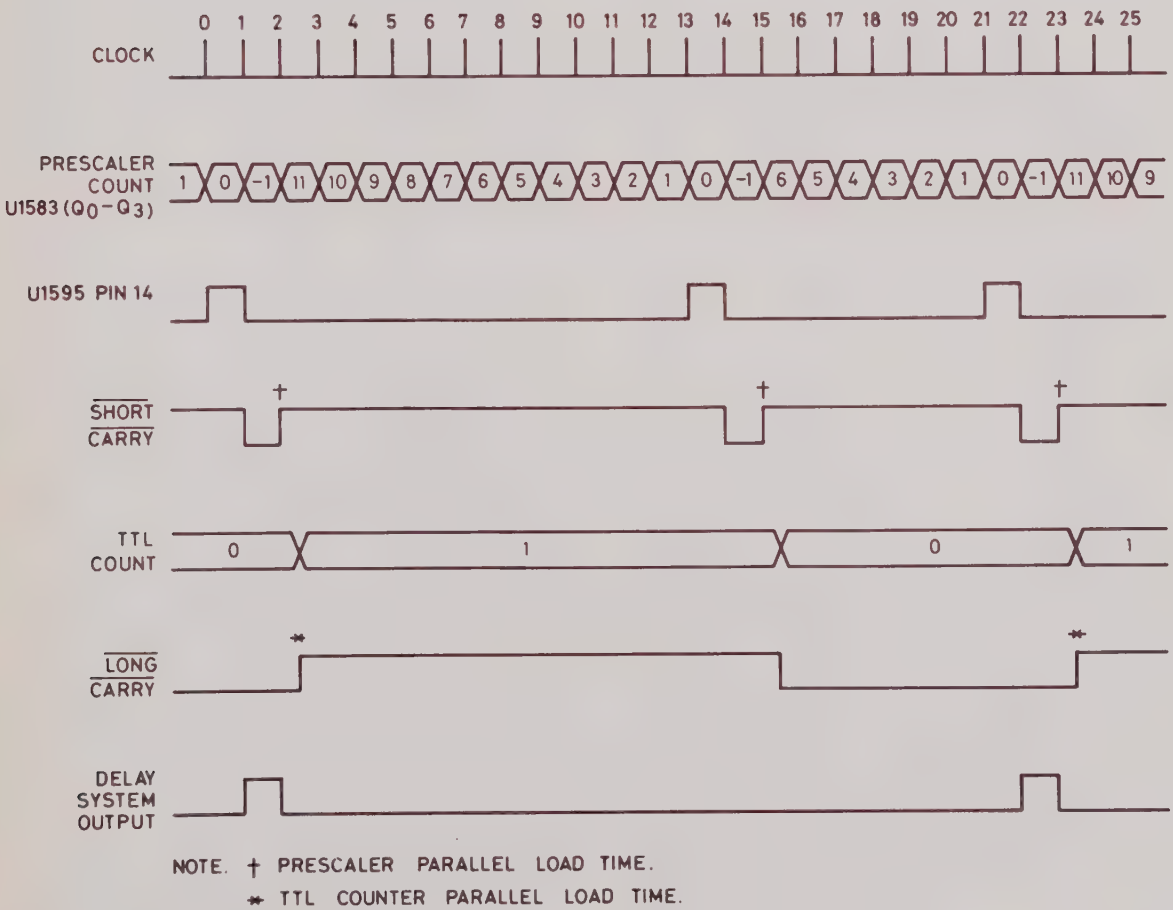

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
CLOCK
PRESCALER COUNT U1583 (Q_0-Q_3)
1 0 -1 11 10 9 8 7 6 5 4 3 2 1 0 -1 6 5 4 3 2 1 0 -1 11 10 9
U1595 PIN 14
SHORT CARRY
TTL COUNT
0 1 0 1
LONG CARRY
DELAY SYSTEM OUTPUT
NOTE. † PRESCALER PARALLEL LOAD TIME.
* TTL COUNTER PARALLEL LOAD TIME.

Fig. 4.6.9 Divide Mode Timing when N = 21

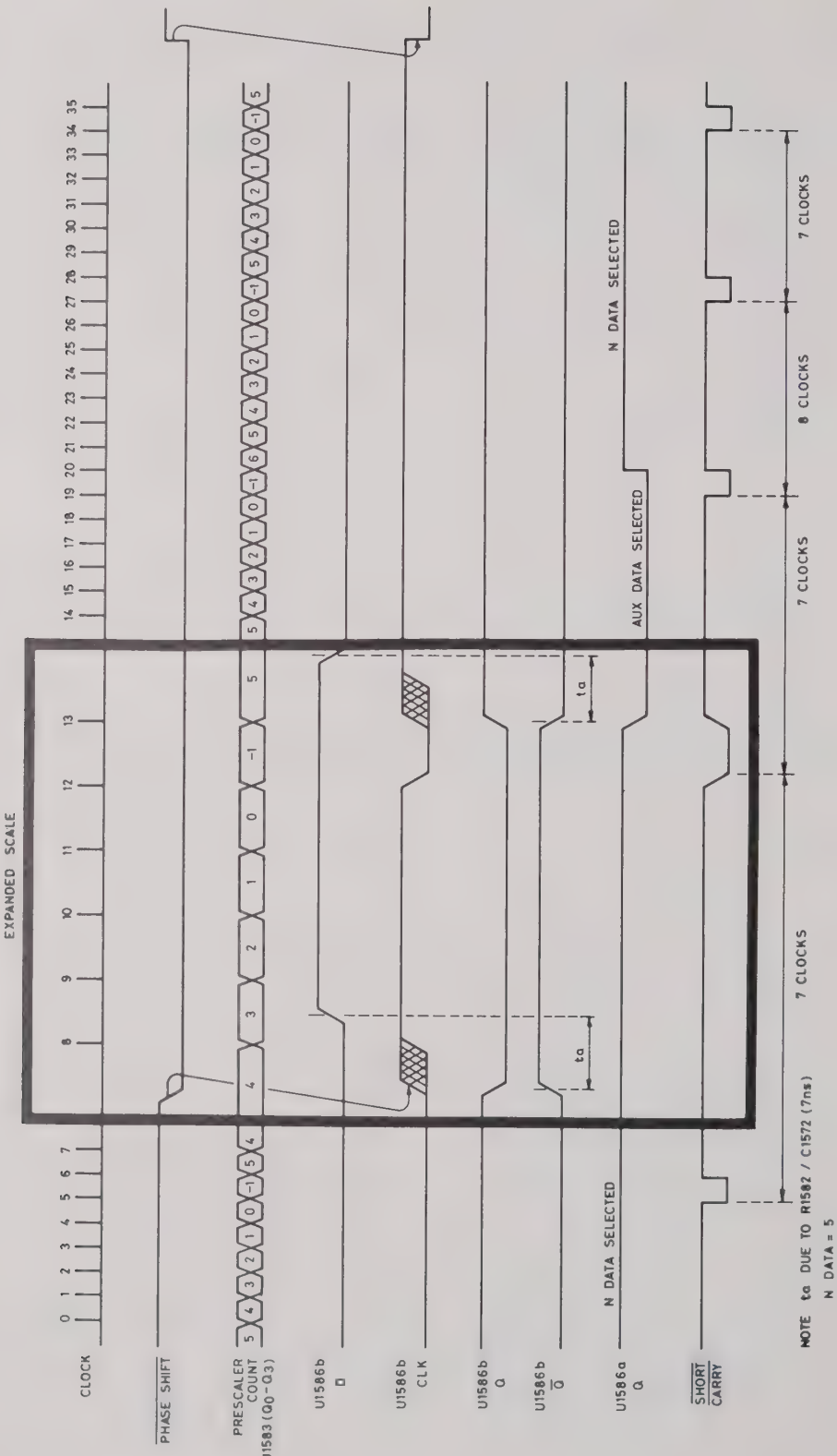


Fig. 4.6.10 Phase Advance Operation when N = 7

PHASE SHIFT low and U1586b clock input goes high taking Q low. ($\overline{Q}$ was low, holding D low). The effect of this is to enable U1565b (rather than U1565a) so that LC.SC may clock U1586b. However, this change-over may cause a transition glitch which, if $\overline{Q}$ were connected directly to D, would immediately clock U1586b back before LC.SC became true. Therefore the path from $\overline{Q}$ to D is delayed by about 7ns with R1582/C1572 so that if a transition glitch does occur U1586b will merely by re-clocked into its existing state.

An U1586a D is now low the next rising edge of SHORT CARRY clocks U1586a Q low to select AUX DATA for the following parallel load. The same SHORT CARRY edge takes LC.SC low so that U1586b is clocked back into the normal state with Q high and is ready for another phase shift sequence.

During this count cycle although AUX DATA is selected it is not loaded until the end of the cycle which consequently occupies 7 clock cycles as normal. At the end of this cycle AUX DATA is loaded and with the rising edge of the same LONG CARRY pulse U1586b Q (high) is clocked through U1586a, so that after the count cycle of 8 clocks (due to loading AUX DATA = 6) the normal division ratio of 7 is re-selected.

Before another phase shift sequence can commence the processor takes PHASE SHIFT high which returns U1586b CK low.

4.6.4 DELAY MODE OPERATION

This description covers all trigger modes where a delay by time or events is specified – see Figures 4.6.3 and 4.6.4.

In delay mode the delay system counter is started by a programmable event according to the particular menu selection, and is stopped when the selected number of clocks has been counted; the counter is then automatically re-loaded with delay value data stored in latches which are in turn set up by the processor.

The details of start/stop control are discussed in section 4.6.2 which shows that a start event will be ignored when START QUALIFIER is high. In delay modes bistable U1585b is reset by INHIBIT SINGLE SHOT COUNT being high (eliminating it as a qualifier) and so the qualifier is generated by NOR gates U1599a, b which are WIRE-OR connected. For an unqualified start even both Q4, Q5 of U1572 will be high so that START QUALIFIER is forced low. Otherwise only one of Q4, Q5 will be low for dynamic qualification.

For trigger modes where 'A' start is delayed from 'A' Trigger ENABLE A0 QUAL is low and the start qualifier function is 'A ramp ready', or, more explicitly 'A ramp not running and not held off'. To detect this valid A start condition, NOR gates U1597d, U1599d combine AQ and HOLD OFF so that START QUALIFIER may only go low when AQ is low and HOLD OFF high.

Some 'B' timebase delay modes require the start qualifier to be the 'B' Start Latch (See Figures 4.6.4 and 4.6.1). For those modes ENABLE B0 QUAL is low enabling START QUALIFIER to go low only when U1610a $\overline{Q}$ (Cursor Management) is high.

OPERATION WHEN N<16

For N = 0, as no delay is required the delay system is not used. For example if the user has selected 'A' start delayed (by N = 0) from A trigger, the processor selects 'A' trigger direct (U1593) rather than A trigger delayed.

For 'A' trigger modes with N = 1 the delay counter proper is not used since a delay of only one clock is required. For example if 'A' start is to be delayed by one clock then the processor takes SELECT A TRIG DELAYED BY N = 1 low (U1578 Qo, Q2, Q3 all high). When the start event is accepted it clocks U1585a low (see section 4.6.2) for the first clock after that to clock U1584a Q low.(MODE 3 is low for N = 1 and so U1598a is disabled). Thus the 'A' TRIG output (U1593 pin 3) goes high to start A timebase. For 'B' trigger modes with N = 1 the 'B' Start Latch is used in a similar way (see Figure 4.6.4).

U1591c eliminates a possible latch up condition when N = 1. In those modes SELECT A TRIG DELAYED BY N = 1 being low leaves R1529, 31, 33 to hold U1591c pin 9 at Vbb. Thus when U1585a Q and U1584a Q high again. Hence only a brief negative going pulse is produced at U1584a Q.

For 1<N<16 only the prescaler is employed, and timing is shown in Fig.4.6.11 when N = 9. Since the prescaler counts one more (in Delay mode) than the value of NDATA (U1576 Qo-Q3) the processor loads the latter with 8 and configures the prescaler to load this value (see section 4.6.2 for details).

To allow counts of N = 1 in some modes the clock delay incurred by U1584a is eliminated. MODE 3 is used to bypass U1584a by resetting the latter and enabling U1598a so that U1583 $\overline{C}$ is controlled by U1585a. Hence, when the start event occurs (see section 4.6.2 for details of start/stop control) it clocks U1585a Q low and $\overline{C}$ low to enable counting. Subsequent clocks decrement the prescaler count until zero is reached when U1595a pin 15 goes low to take STOP ON N (U1595b output) high. (LONG CARRY will be low – see section 4.6.2). STOP ON N, being the selected stop event, clocks U1585a high which takes U1583 C high to inhibit further counting. When clock 10 occurs it clocks the logic high from U1595a pin 14 through U1584b to produce SHORT CARRY which triggers the appropriate timebase ramp generator or 'B' start latch. When clock 11 occurs, since U1583 S1 is low, U1583 is once again loaded from N DATA for the next delay cycle. This sends U1595a pin 14 low and clock 12 clocks SHORT CARRY high again via U1584b.

OPERATION WHEN N>15

These delays involve both the prescaler and TTL counters and timing for N = 20 is shown in Fig. 4.6.12.

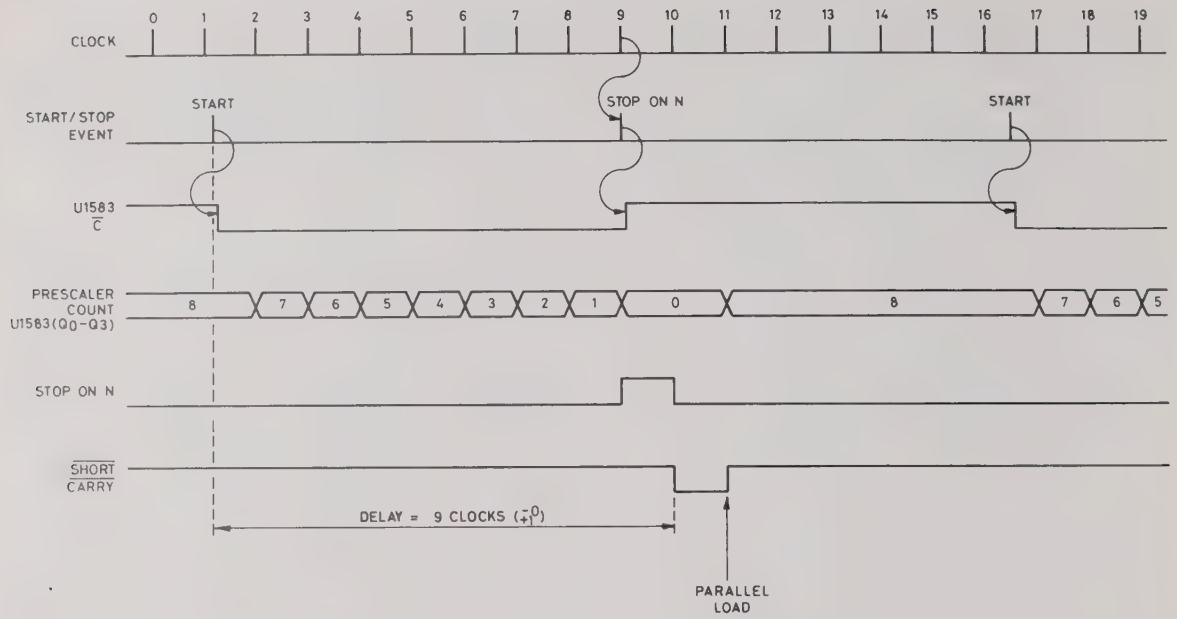


Fig. 4.6.11 Delay Mode Timing when N = 9

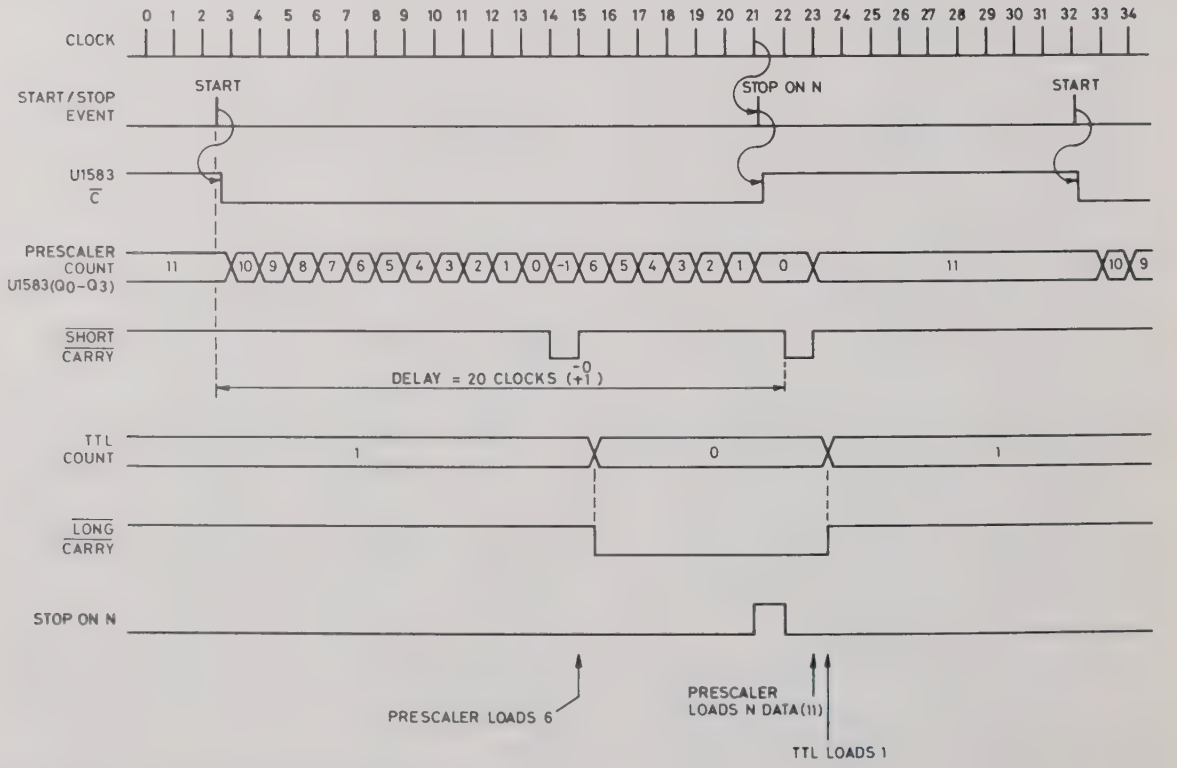


Fig. 4.6.12 Delay Mode Timing when N = 20

When the particular delay mode is requested by the user the processor loads the TTL counter with 1 and that of the prescaler with 11 (see section 4.6.2 for details). This gives the required total count of 8 +(11+2) = 21. The processor then allows counting to start and the parallel load sequence is automatically executed by hardware when each delay phase is complete.

STOPWATCH MODE being high allows the 2 line to 1 line selector formed by U1577 to pass SHORT CARRY to monostable U1587b (described in section 4.6.2). The TTL counter is thus clocked shortly after the rising edge of SHORT CARRY.

Prescaler operation is essentially similar to that for N<16 but the terminating signal STOP ON N can only be produced when both LONG CARRY and SHORT CARRY are low. After the start event, clocks 3–13 decrement the prescaler to zero and SHORT CARRY occurs at clock 14 (which decrements the TTL count). This takes U1583 S1 low to allow prescaler loading on clock 15. However, since MODE 1/2 is low, the rising edge of SHORT CARRY clocks LONG CARRY (high) through to U1587a Q. This forces the D0–D3 inputs of U1583 to assume the value 6 via the gates of U1590.

Thus SHORT CARRY clocks the TTL counter to zero and LONG CARRY goes low. Hence when the prescaler count next reaches zero (at clock 21) both inputs of U1595b are low and STOP ON N goes high. Thus clock 22 takes SHORT CARRY low to trigger the appropriate timebase ramp generator of 'B' start latch. At clock 23 the rising edge of SHORT CARRY clocks LONG CARRY (now low) through to U1578a Q. This enables the gates of U1590 to pass N DATA (11) through to U1583 which is thus loaded for the next delay sequence. The TTL counter is also re-loaded shortly after the rising edge of SHORT CARRY at clock 23.

4.6.5 'STOPWATCH' MODE OPERATION

In 'stopwatch' mode (current cursor time) the time between start of sweep and the current cursor is measured in units of 10ns using the 100MHz clock, or in terms of the user-supplied 'B trigger events'. The delay system start and stop events depend on the machine horizontal datum, current cursor and horizontal mode and the possibilities are shown in Figure 4.6.3.

Fig. 4.6.13 shows Stopwatch mode timing when the datum is 'A' start. To allow the processor time to read the delay counter value after the measurement a single shot circuit formed by U1585b, U1598b, d is employed. The operation of this circuit is identical to that for Phase Shift control and full details appear in section 4.6.3.

Before the measurement commences the processor loads the whole counter with maximum count (see section 4.6.2) and takes INHIBIT SS COUNT high to reset U1585b.

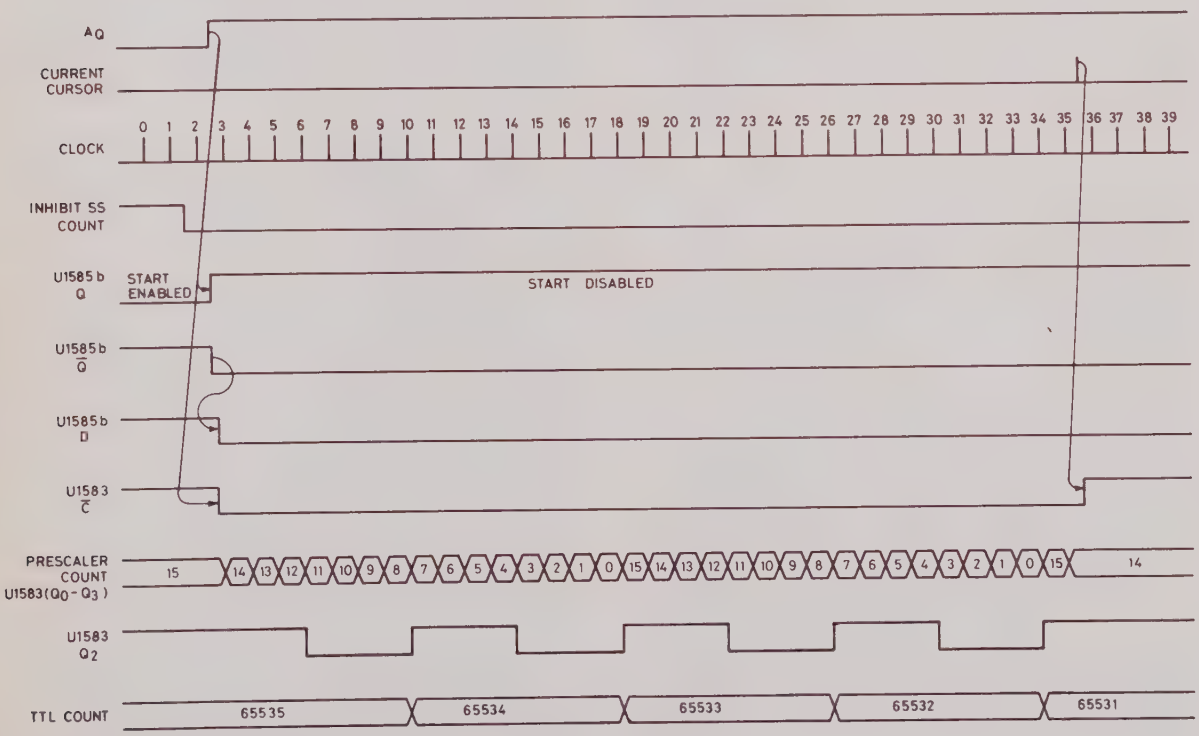


Fig. 4.6.13 Stopwatch Mode Timing (Typical)

To initiate the measurement the processor takes this line low but this leaves Q low and since write only port U1572 Q4, Q5 are both high in 'Stopwatch' mode (unqualified start) U1585a D is low to enable the start event, AQ. (For full details of start/stop control see section 4.6.2).

In 'Stopwatch' mode MODE 3 is high and thus U1584a is reset allowing U1583 $\overline{C}$ to be controlled by U1585a via U1598a. U1598a. Thus when AQ goes high $\overline{C}$ goes low enabling counting and also clocks U1585b Q high. Thus when the stop event (current cursor) occurs U1585a D will remain high to inhibit further counting until the processor takes $\overline{\text{ARM SINGLE SHOT}}$ low to clock U1586b back into the 'ready' state with Q low.

In 'Stopwatch' mode the 2 line to 1 line selector formed by U1577 allows Q2 of U1583 to clock the TTL counter via monostable U1587b. Moreover CLEAR S1 is high and thus U1584b $\overline{Q}$ is high and the prescaler never parallel loads. Hence the TTL counter is clocked once every 8 prescaler clocks.

Once the counter has started, counting continues until the current cursor stop event occurs when U1583 $\overline{C}$ goes high to freeze the whole counter.

U1574, 5 form inverting ECL to CMOS level translators with their non-inverting inputs connected to the Vbb threshold produced by R1585/N1585 pin 9. It is thus possible for the processor to read the prescaler count, U1583 $\overline{C}$ and U1585b Q via U1573, 4, 5. The processor determines when the measurement is complete by waiting until $\overline{C}$ is high with U1585b Q high. (Counter not running AND single shot circuit not armed). It then reads the prescaler count via U1573, 4 and the value left in the TTL counter via U2067, 8. The processor then subtracts this value from maximum count to obtain the true period between AQ and current cursor.

4.6.6 TIME-CAL OPERATION

To produce the Time-Cal output, the delay system free runs, dividing down the 100MHz clock by the ratio appropriate to the selected period. However the delay system output is a pulse with width only equal to that of $\overline{\text{SHORT CARRY}}$ (10ns). To convert this ECL output to a bipolar square wave a bistable connected to divide by 2 is employed.

The processor selects the clock source as 100MHz (U1596) and asserts ASYNC START. Counter operation is then as for Divide mode operation (described in section 4.6.3) where only the prescaler is employed for periods of less than 340ns, and TTL counter and prescaler for periods of more than 320ns.

The Time-Cal output is taken via the 'B' trigger source selector where $\overline{\text{SELECT B TRIG DELAYED}}$ is low to allow the simultaneous occurrence of $\overline{\text{SHORT CARRY}}$ and $\overline{\text{LONG CARRY}}$ low to take U1594 pin 3 high. $\overline{\text{ENABLE TIME}}$ is also low so that U1565c passes the 10ns wide pulse to the ÷2 circuit (U690b) which is part of the Trigger Amplifier assembly.

4.6.7 SOFTWARE EXTENSION OF COUNTER

To achieve count lengths greater than available from TTL plus prescaler counters a 16 bit software counter is employed. The 'clock' for this counter is effectively the Delay IRQ (see CPU circuit diagram) and so the software count decrements once for every $\overline{\text{LONG CARRY}}$.

The 'carry' output from the software counter can be identified with the processor control of the $\overline{\text{LONG CARRY}}$ output from the TTL counter. Only when the software count reaches zero is $\overline{\text{LONG CARRY}}$ enabled to the prescaler where the critical timing of $\overline{\text{SHORT CARRY}}$ produces the final overall carry output from the system.

The 'carry' output from the software counter occurs a minimum of 5ms before the TTL counter reaches zero and thus software response time is uncritical. Timings are therefore as shown for TTL plus prescaler.

Note that all timings are absolutely controlled by the prescaler.

4.7 CURSOR GENERATION AND CONTROL

4.7.1 GENERAL

This section deals with real-time cursors and does not include cursors found on stored traces; these are part of the acquisition system.

In operation, cursors appear as brightups approximately 1mm long only on real time traces. With X expanded this becomes 1 centimetre. Cursors are not available in X-Y mode. Cursors are produced by the comparison of a timebase ramp and a voltage supplied from the voltage generator system.

The circuit described below is on the timebase board, and except where otherwise noted component references are prefixed by 16xx. Outputs from the timebase board go at E.C.L. logic levels to the tubebase (brightup circuit) and the acquisition board (sampling).

4.7.2 BLOCK DIAGRAM DESCRIPTION (See Fig. 4.7.1)

Voltage generator outputs at ±4V dc are transmitted as a differential voltage (one side being referenced to the voltage generator ground) to the timebase board. Some noise filtering is provided by the action of C53, C63 etc. with two of the resistor network elements. A local +2 volt reference is provided by U34 (pin 10 output) adjusted by R13. The regulator connects to the inputs of the differential amplifiers in U32, producing an offset at the output of -2V. All network resistors are of equal value resulting in a differential gain of ½, and hence an output control voltage of 0 to +4V.

The four cursors are generated by dual high speed comparators U31, U41, U51 and U61; each is connected in an identical configuration as a window comparator. U31 and U51; for cursor 1 and 3, have inputs connected, via emitter followers in U1222, to A ramp only.

Comparators U41 for cursor 2 (C2 and U61 (C4), can be

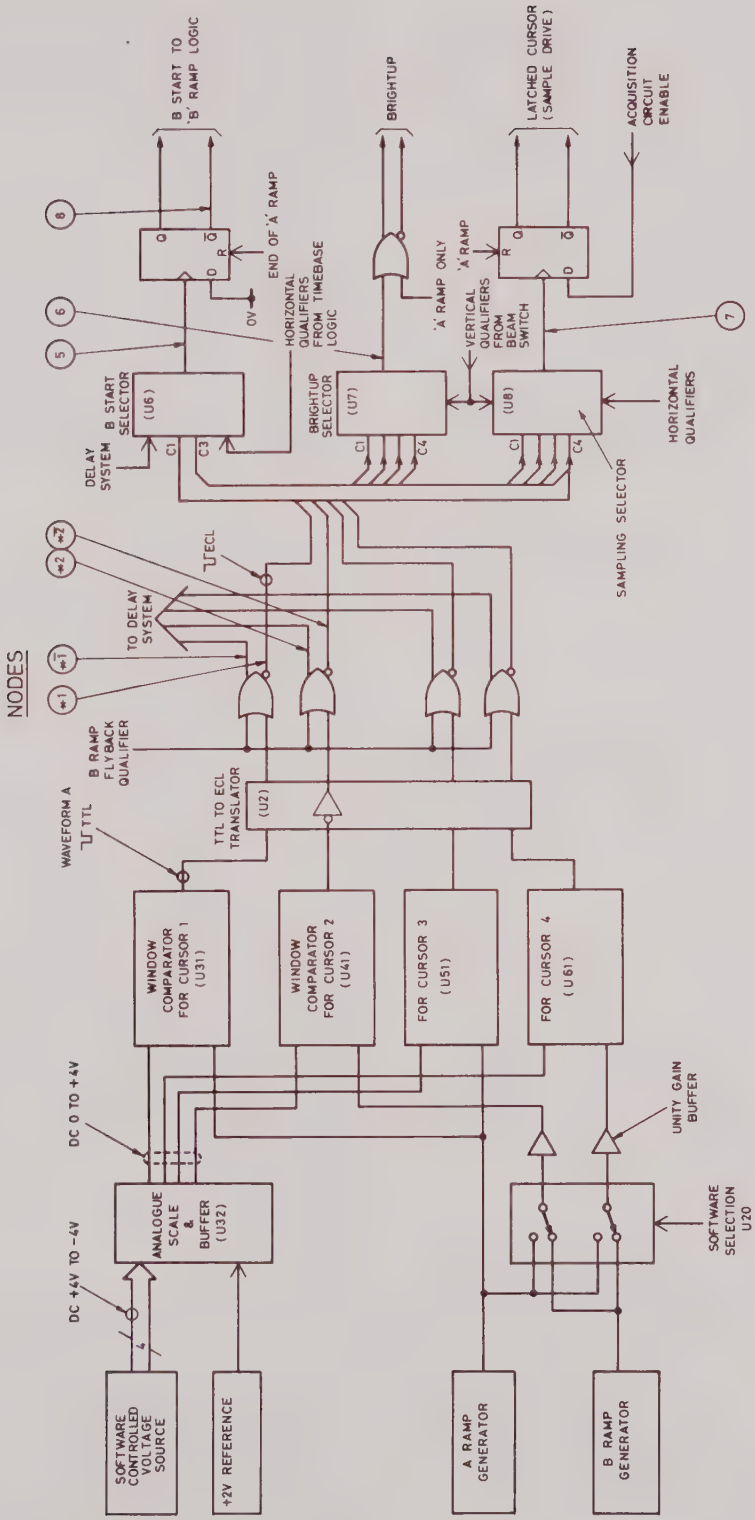


Fig. 4.7.1 Schematic of Cursor System

selected by analogue gate U21 to have an input from either A or B ramp.

4.7.3 CURSOR GENERATION (See Fig. 4.7.2 and 3)

As all comparators are identical only U31 will be described in detail: for Cursor 2 U41 can be substituted, C3 U51 etc. Similarity exists to component level e.g. R34, 44, 54 etc. serve the same purpose.

The ramp input to pins 2 and 11 increases from 0 to approximately +4volts, and is simultaneously compared with two very closely related voltages on pins 7 and 12. The voltage on pin 12 (VH) is a scaled and offset output from the voltage generator and as such is under microprocessor control. A transistor in array U33 passes a constant current through R32 to maintain the voltage at pin 1 (of U31) at a constant offset of 40mV from pin 12. This offset remains constant irrespective of absolute voltage.

The first transition (negative going) of the comparator output on PIN 4 occurs when the ramp voltage on PIN 2 is greater than input voltage on PIN 1. Positive feedback via R34, ensures a stable transition at slow ramp speeds.

The output on Pin 4 remains low until the ramp voltage has increased and exceeds that on pin 12. This causes the comparator (b) to change state and hence pin 9 to go low, in turn forcing pin 4 high some nanoseconds later. Positive feedback is again applied to stabilise this transition; via R35, C35. Because at the fastest timebase speeds delays in the comparator become important, C34 is employed on the output of the second comparator. This ensures that cursors remain substantially constant width and similar under these conditions.

4.7.4 SELECTION

The only selection that is made for the input to the comparators is that of ramp to cursors 2 and 4. In dual ramp timebase mode U20, a software driven port, addresses the analogue gate U21, independently selecting C2 or C4 to have an A or B ramp input. The output of the analogue gate is buffered in each case by voltage followers U40 and U60, to provide a low impedance drive to the comparator. Due to the selection components, ramp inputs to the comparators are delayed, typically by 15nS.

The output of each comparator is taken via a 100Ω resistor R37, R47 etc. to one inverting input of an ECL line receiver,in a quad package, U2. The resistor allieviates edge effects and the receiver translates the TTL logic swing to ECL above ground. (Note all the ECL logic is powered from the +5 volt supply). Outputs from the receiver are taken to U5 for C1 and C2, and U1 for C3 and C4.

Gates U4 and U5 have an input from B ramp logic, (BQ) which can be disabled by the processor, via D1, D2 etc. When a cursor is selected to be on B ramp the BQ qualifier becomes active, causing any cursor output during B flyback to be suppressed.

Complementary outputs from U4 and U5 are taken directly to the delay system start/stop multiplexer. Use of these signals is described fully in SECTION 4.6, but briefly they can be used to start the delay counter in such modes as "B sweep starts after CURSOR + DELAY". Stop functions are required for current cursor on crystal timebase, and for calculation modes. The negative going outputs, from pins 3 and 14 are taken to selectors for B start event (U6), brightup (U7) and sample circuit drive (U8).

Cursors can be selected to cause B start, brightup or sampling action independently, and although all cursors may be causing a brightup it is unusual for more than one to be enabled for sampling. It should be noted that, for B start or sampling, the first output transition is latched. The occurence of transitions caused by later cursors have no effect, only one cursor per A timebase sweep can cause a B start or sample to be taken.

4.7.5 QUALIFICATION-GENERAL

Fig. 4.7.4 Cursor assignment in multimode displays gives details of the assignment of cursors in all real time trace selections. This becomes necessary to avoid ambiguity of cursor measurement and position. Qualifiers, appearing as low-going signals, are applied at the selector inputs, enabling the selected cursor function to occur only when all vertical and horizontal conditions are correct.

Modes that include both B1 and B3 traces use local logic to group C1 with C2 and C3 with C4. At fast timebase speeds successive sweeps can occur at a rate too fast for the processor to distinguish.

4.7.6 VERTICAL QUALIFIERS (by channel) – See Fig. 4.7.5

These are required in all trace selections to eliminate the appearance of cursors on either trigger view or alphanumeric traces. Complementary signals are taken directly from the beam switch control logic on the Y pre amplifier to PLB2. In the case of channel 1 (CH1) signal, R11 and R12 together with C28 form a delay of about 300nS into the line receiver U12, this produces an output $\overline{\text{CH1}}$ at pin 2. A delayed form of CH2 beam switch drive, $\overline{\text{CH2}}$ is produced in the same way and output on U12 pin 6.

Delay inserted at this point in the system ensures that beam switch transitions are not sampled and brightup does not occur.

In single channel operation, port U24 pin 15 is latched low, and U9 pin 9 follows. This enables output low transitions on both pin 2 and pin 15 when either $\overline{\text{CH1}}$ or $\overline{\text{CH2}}$ is low: i.e. when either channel is displayed. These two, now identical outputs, enable both pairs of cursors C1 and C2, from pin 2, C3 with C4 from pin 15, when either single channel mode is requested. In dual channel modes D11 is driven high, and U9 becomes two separate halves. Output low transitions on pin 2 only occur when an input low on pin 5 occurs, thus only C1 and C2 are enabled on selectors U7 and

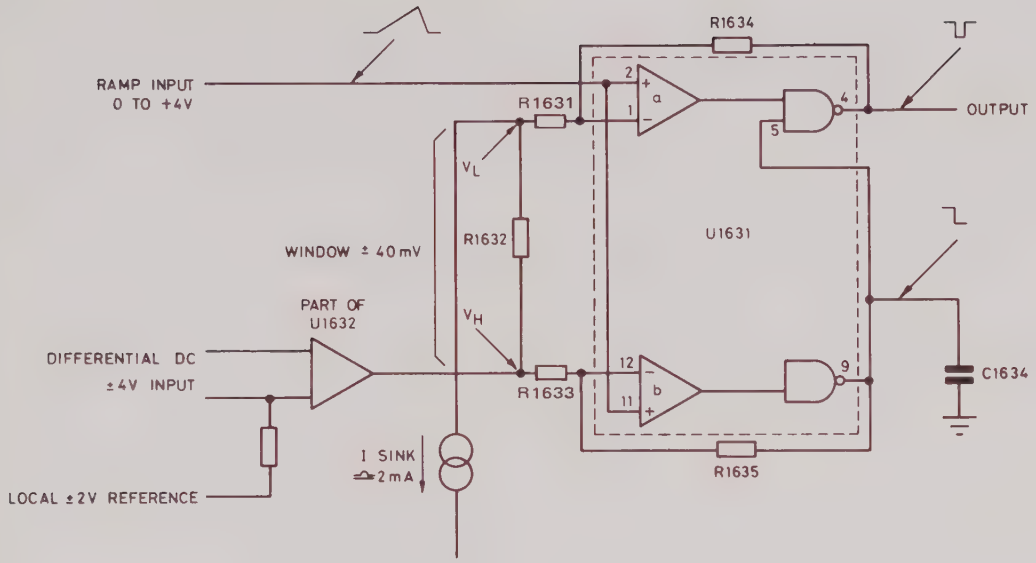


Fig. 4.7.2 Comparator Schematic

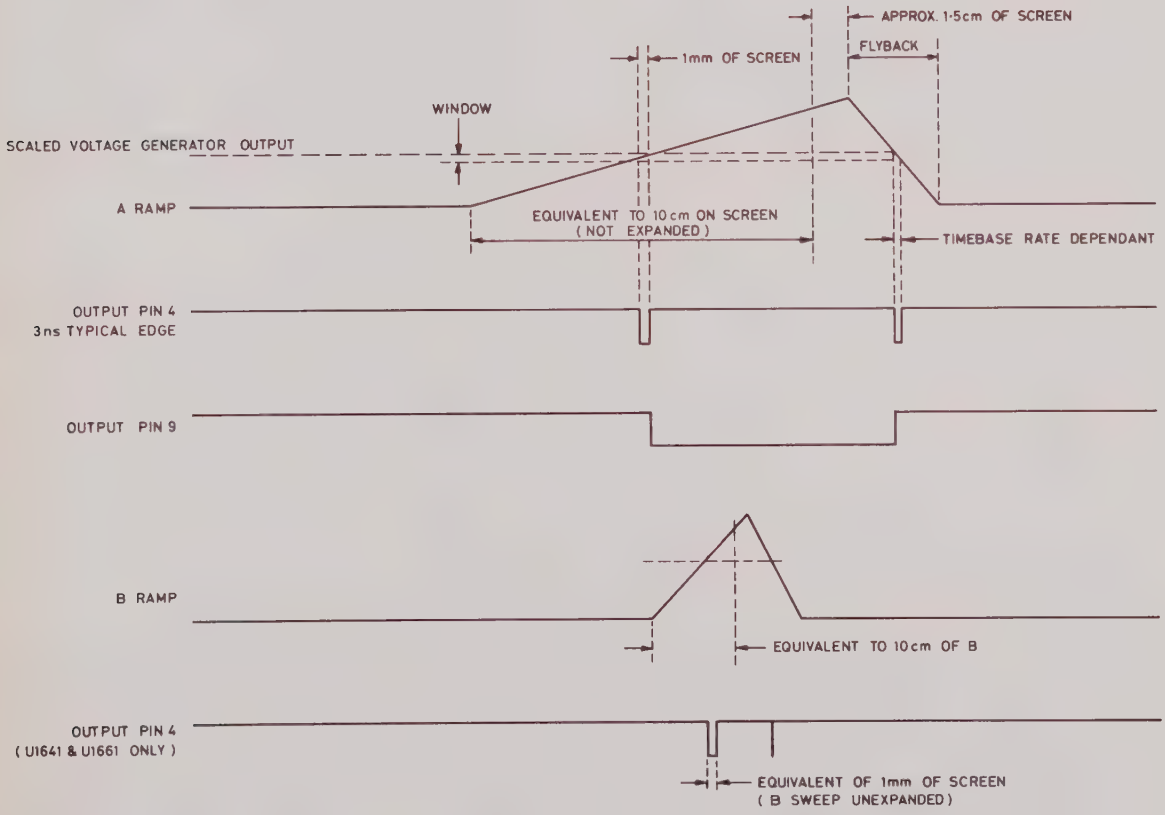


Fig. 4.7.3 Comparator Voltages

CHANNEL SELECT	A RAMP ONLY	A INT. B OR A ALTERNATE B				B RAMP ONLY		
		B RAMP						
				DUAL			DUAL	
		A RAMP	SINGLE	C_1 START	C_3 START	SINGLE	C_1 START	C_3 START
SINGLE CH1 or CH2	ALL	1 & 3	2 & 4	2	4	2 & 4	2	4
DUAL CH1	1 & 2	1	2	2		2	2	
CH2	3 & 4	3	4		4	4		4

Fig. 4.7.4 Cursor Assignment in Multimode Displays

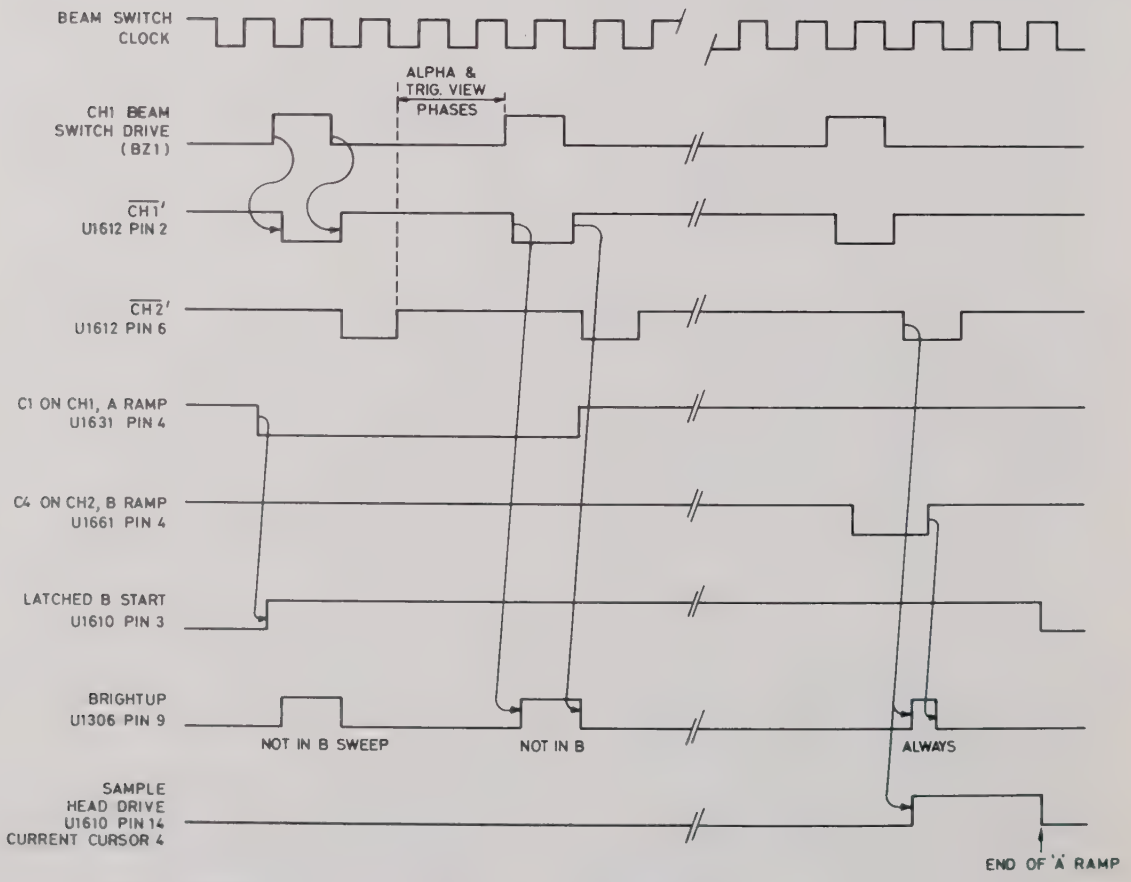

BEAM SWITCH CLOCK
ALPHA & TRIG. VIEW PHASES
CH1 BEAM SWITCH DRIVE (BZ1)
CH1' U1612 PIN 2
CH2' U1612 PIN 6
C1 ON CH1, A RAMP U1631 PIN 4
C4 ON CH2, B RAMP U1661 PIN 4
LATCHED B START U1610 PIN 3
BRIGHTUP U1306 PIN 9
NOT IN B SWEEP
NOT IN B
ALWAYS
SAMPLE HEAD DRIVE U1610 PIN 14 CURRENT CURSOR 4
END OF 'A' RAMP

Fig. 4.7.5 Vertical Qualifiers & Outputs (In Chop) A ALT B, Dual Channel.

U8 for this channel displayed. C3 and C4 become enabled when pin 15 goes low, pin 12 of U9 causing this to occur, as channel 2 is displayed. The scheme adopted is valid for both alternate and chop modes of display. The delayed form of channel qualifier is a system requirement in chop; alternate mode beam switch transitions occur at the end of trace whilst the display is blanked. In chop beam switch transitions occur at a 1MHz rate and must have settled before bright-up or sampling can occur.

4.7.7 HORIZONTAL QUALIFIERS (by ramp displayed) - See Fig. 4.7.6

These are derived from the timebase logic dual D-type U1405. The latch U16 re-synchronises the signals with a clock derived from the back edge of A timebase gate. Comparator U14 produces this signal on pin 7, a CMOS compatible output which is taken to U16 clock pin 9, so that output transitions of U16 only occur during flyback of A ramp, when cursors are universally disqualified. The action of U1405 is described fully in section 4.9, but essentially a reapeated sequence of traces is displayed. The sequential pattern is of variable length but always contains one phase for each unique combination of all possible X and Y modes.

Referring to FIG. 4.7.6 the horizontal qualifiers can be split into two pairs of signals. One pair A displayed, complement B displayed, act on the X beam switch, causing the appropriate ramp to be displayed. The A displayed signal is used by the cursor system U17 pins 1 and 6 to qualify cursor 1 and C3 brightup, enabling these only when A is displayed, via pins 3 and 4.

The other pair of signals from U16 are $\Phi 1$ and $\Phi 2$, from pins 15 and 14 respectively, these are also complementary. In any dual B ramp mode, the outputs of U23 are enabled by a high from control port U24 pin 9. In the mode shown (ref. Fig. 4.7.6) $\Phi 1$ and $\phi 2$ are A displayed $\div 2$. They are used via D22 and D33 to qualify the delay system start events and also by the cursor system to pair C1 with C2 and C3 with C4. The output of U23 pin 3 goes low to enable C1 to clock the B start latch; in the same phase C2 is enabled to sample or cause a brightup in the B trace. Similarly U23 pin 4 qualifies C3 B starts and enable C4 on U7 and U8 via U26 in $\phi 2$, (high).

Latched B start is produced by U10a, a clock on pin 6 being selected by U6 causing only one transition, (Q PIN 2 $\downarrow$) per A ramp sweep.

As well as C1 and C3 being available as clock sources, the delay system terminal count can be selected. Pin 10 of U6 goes low and the coincidence of long carry and short carry cause +ve output at U6 pin 3. A forcing mode, whereby B ramp is started with A ramp is also available when U1 pin 10 is low, via the reset pin 4 of U10. The latched B start is cleared at the end of each A ramp by a high on pin 5 of U10.

Note latched B start can be used by the timebase logic, either as a trigger event, or as a qualifier and that only one B start can occur per A timebase ramp.

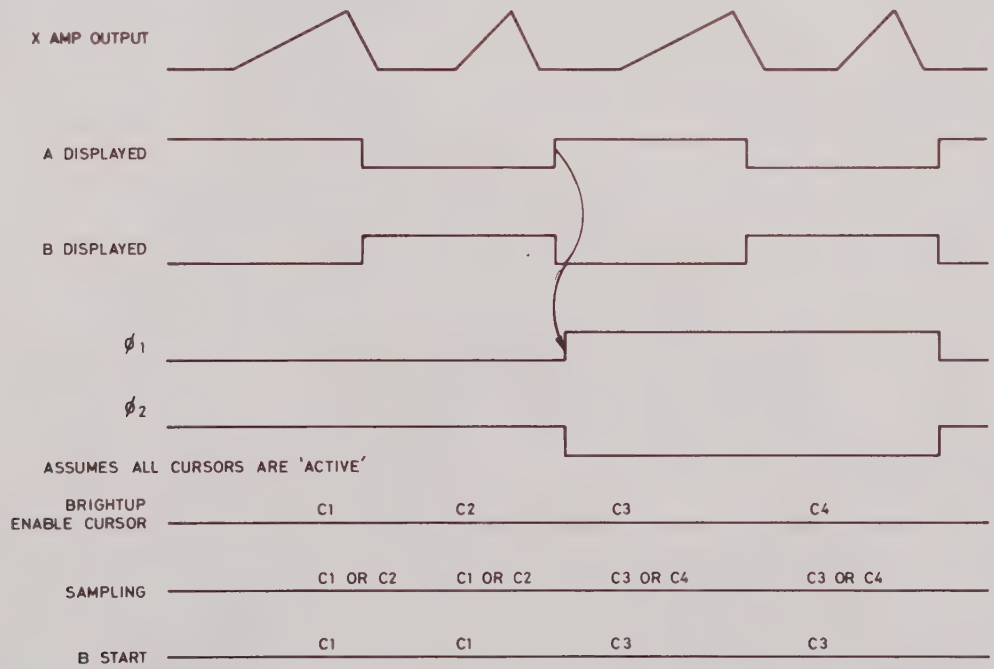


Fig. 4.7.6 Horizontal Qualifiers (A ALT. B)

Qualified brightup is output on U1306 pins 9 and 15 as a complementary signal having been produced by the selector U7 pin 2, as a negative transistion; an additional qualification is obtained from A timebase gate to stop any possible brightup during flyback.

Sample head drive is produced from the second element in U10, on pins 15 and 14. The output is again reset at the end of A ramp, only one transition occurring per sweep. The D of this latch is however controlled by the acquisition system and when this input is taken high, output transitions are inhibited. The sample head drive signal is usually active every timebase sweep, independent of which ramp is being displayed. (see also Acquisition).

4.8 BRIGHT-UP AND BLANKING SYSTEM

4.8.1 BASIC FUNCTION

The bright-up and blanking system controls all aspects of trace brightness, including alpha and real-time brill controls, timebase bright-up and contrast, Z mod, trace-locate bright-up, chop blanking (ref display management) and fly-between blanking (ref data display).

4.8.2 OPERATING MODES

The system has two basic operating modes, alpha (ref display management) and real-time, which may be sub-divided as detailed under 'operating modes' in the timebase section. Alpha mode switches from real-time to alpha brill. controls and enables the fly-between blanking from the data display system, which blanks the display between individual dots of the alphanumeric characters.

4.8.3 GENERAL SYSTEM

Fig. 4.8.1 shows a block diagram of the system. Trace brightness is controlled by a signal to the CRT grid derived from the output amplifier (a positive signal increases brill). The A.C. component of the signal is connected via a capacitor to the tube grid. As the tube grid is at -2.2KV, special arrangements are required to couple the D.C. component. A floating supply in the EHT unit maintains a constant voltage of approximately 2.2KV between the lines marked BRIGHT-UP L.F. and GRID BIAS.

The output amplifier is a shunt feedback amplifier, providing a virtual earth point as a summing junction for the various inputs. The bright-up limit prevents the total signal input from overloading the output amplifier.

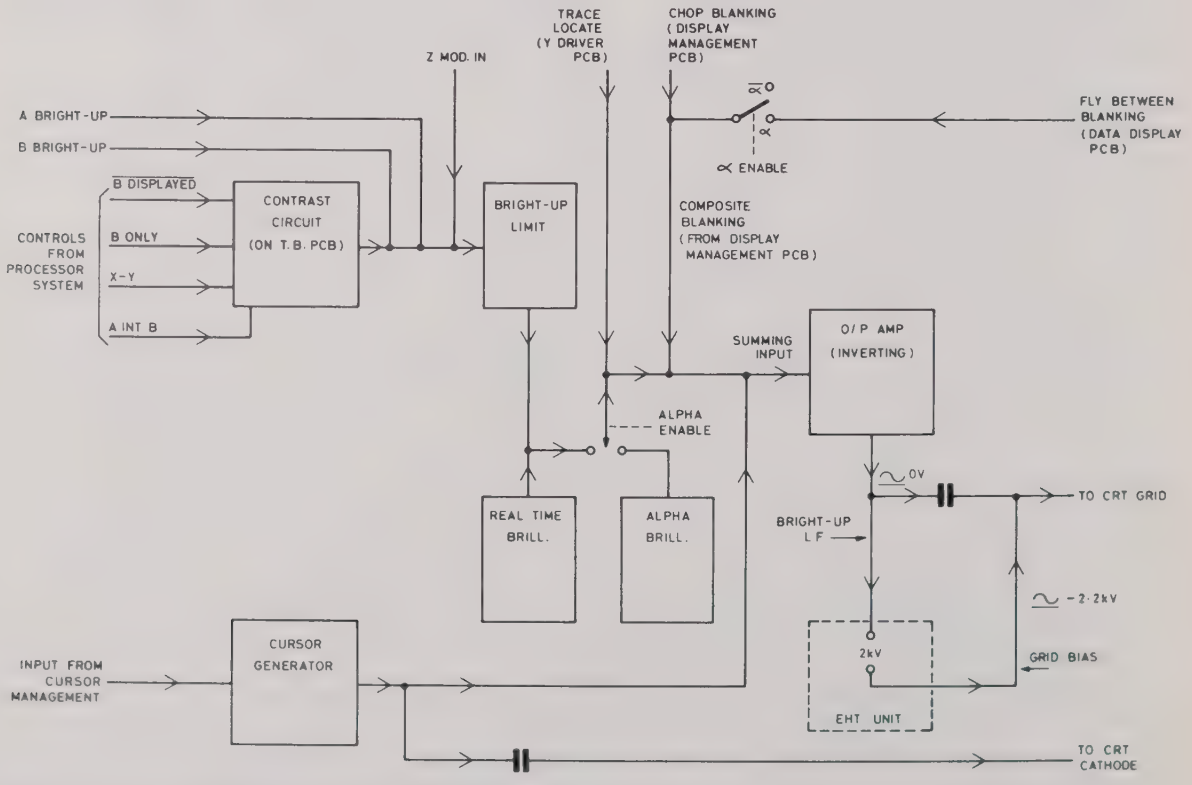


Fig. 4.8.1 Block Diagram Bright-up & Blanking System

The contrast circuit controls the relative intensities of A and B bright-ups in each timebase operating mode by working in conjunction with the bright-up limit. Four inputs; A gate B gate, contrast, and the real-time brill control, can each provide a current sinking signal equivalent to the working range of the output amplifier. This quantity has been designated 1 brill unit in figs. 4.8 2a,b,c. The bright-up limit is equivalent to 2 units, and the output amplifier is biased back by 2 units, so an input equal to bright-up limit brings the brill control to its normal working range. In 'A intensified by B' mode, or the A displayed phase of 'A and B alternate' mode, the current contribution from the contrast circuit is determined by the contrast control, and forces a variable amount of the B bright-up signal beyond the bright-up limit, which clips it, and so varies the ratio of A to B bright-up, see fig.4.8 2b. In 'A only' mode, the contrast control is bypassed, giving a constant output of 1 unit, which brings the A bright-up to the threshold of operation, see fig. 4.8 2a. In 'B only' mode, or the 'B displayed' phase of 'A alt B' mode, contrast current is inhibited, but, since B ramp only occurs within an A ramp, the A ramp contribution brings B bright-up to the threshold of operation, see figs. 4.8 2a and 2c.

The cursor generator amplifies the control signals from the cursor management system, providing a 12 volt signal of ~2ns rise-time. Note that the transistors of the output amplifier, which are required to deliver ~60V swing, cannot handle pulses of 2ns rise time and so the high frequency components of this signal are coupled to the C.R.T. cathode via a small high-voltage capacitor. The low frequency (including D.C.) components are inverted by the output amplifier, and applied to the tube grid.

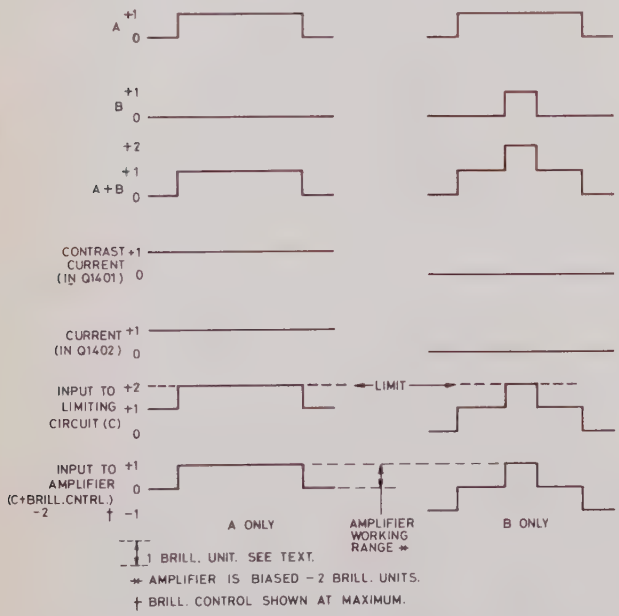


Fig. 4.8.2a Interaction of Bright-up Signals and Operation of Limit.

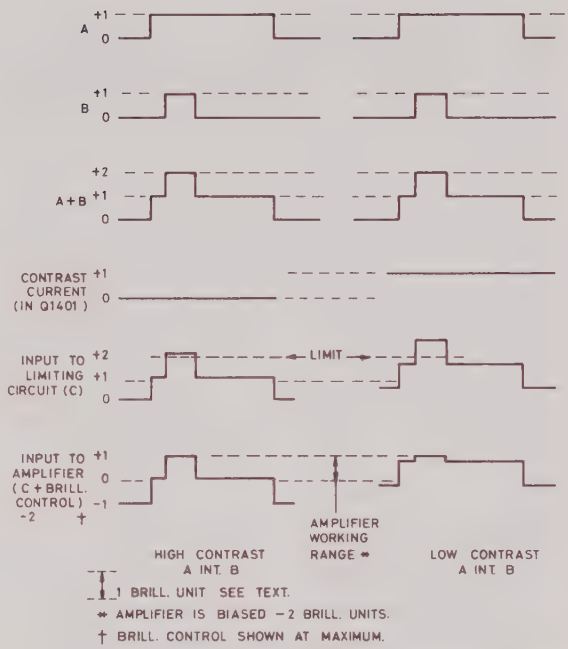

A
B
A+B
CONTRAST CURRENT (IN Q1401)
INPUT TO LIMITING CIRCUIT (C)
LIMIT
INPUT TO AMPLIFIER (C + BRILL CONTROL) -2 †
AMPLIFIER WORKING RANGE ↔
HIGH CONTRAST A INT. B
LOW CONTRAST A INT. B
1 BRILL. UNIT SEE TEXT.
↔ AMPLIFIER IS BIASED −2 BRILL. UNITS.
† BRILL. CONTROL SHOWN AT MAXIMUM.

Fig. 4.8.2b Interaction of Bright-up Signals and Operation of Limit.

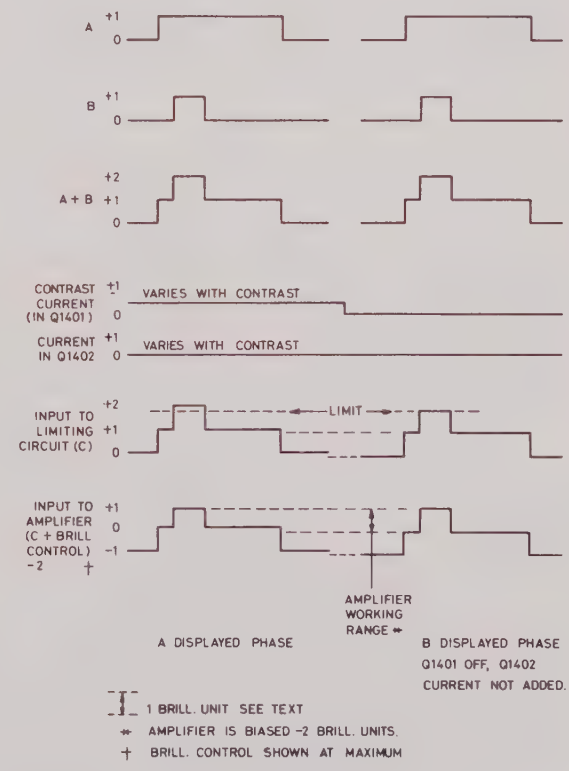

A
B
A+B
CONTRAST CURRENT (IN Q1401)
VARIES WITH CONTRAST
CURRENT IN Q1402
VARIES WITH CONTRAST
INPUT TO LIMITING CIRCUIT (C)
LIMIT
INPUT TO AMPLIFIER (C + BRILL CONTROL) -2 †
AMPLIFIER WORKING RANGE ↔
A DISPLAYED PHASE
B DISPLAYED PHASE Q1401 OFF, Q1402 CURRENT NOT ADDED.
1 BRILL. UNIT SEE TEXT
↔ AMPLIFIER IS BIASED −2 BRILL. UNITS.
† BRILL. CONTROL SHOWN AT MAXIMUM

Fig. 4.8.2c A ALT. B

4.8.4 OUTPUT AMPLIFIER

Emitter follower Q933 drives common emitter stage Q932, with R941 providing shunt feedback around both stages. At low frequencies, cascode pair Q930 and Q931 act as a constant current load for Q932, but, at high frequencies, Q930 base is driven by C934 to improve the positive slew rate when Q932 is cut off.

When the system is in real-time mode (see alpha/real-time switching below) the effective circuit is as shown in fig. 4.8.3a. The combined effect of signal sources shown to the left of D934 is only to sink, not source currents to the virtual earth, and so they cannot drive the amplifier output negative. The value of R939 is such that, with D934 cut off, the output is held at approximately +15V, thus keeping Q932 well away from saturation. Composite blanking which is received at ECL level by long tailed pair Q903 and Q904 cannot be applied via D934, since the high slew rates require a current pulse into the virtual earth when the output is driven negative. However, it is permissible to bypass D934 and drive Q932 much closer to saturation during the short (~200nS) composite blanking pulse than would be allowable during the indefinite timebase blanking period. D936 and D937 prevent complete saturation during the composite blanking pulse. When the collector of Q932 falls to +one Vbe, the base current which normally passes through D936 is diverted into the collector via D937, preventing any further positive base drive.

Bright-up current from the contrast system is opposed by I BIAS, applied via R935 and Q934, which buffers the virtual earth from the coax cable impedance. R932 and R933 hold the base of Q934 at +2.4 volts, therefore its emitter is at +3 volts, which defines the operating voltage of the contrast system.

Bright-up currents up to IBIAS reduce the current through D933, allowing the brill current through R954 to drive the amplifier output positive. The action of the contrast circuit is limited by D933, which is cut off if the bright-up current exceeds I BIAS.

The processor can blank the real-time display by driving R965 positive via port U2411. Z mod input is applied via R930 and D930.

In alpha mode, a current I DISable which is greater then the maximum current through R954, cuts off D934, isolating the real-time system from the output amplifier.

The circuit is then effectively as shown in fig.4.8.3b. Alpha intensity control current from R903 is applied to the virtual earth input via D902, which prevents currents being injected into the virtual earth and saturating Q932.

This function is provided by D934 in the real-time section. In real-time mode, I DIS is applied to D902 cathode, thus isolating the alpha intensity input.

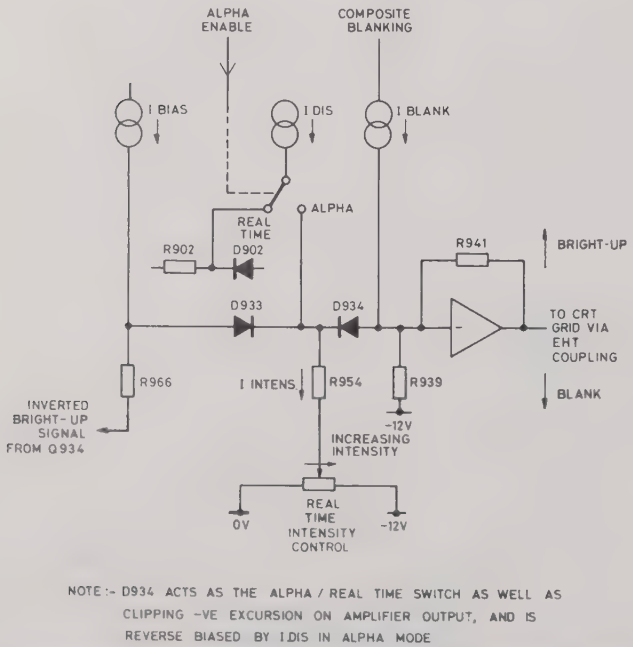


Fig. 4.8.3a Equivalent Circuit of Bright-up in Realtime Mode.

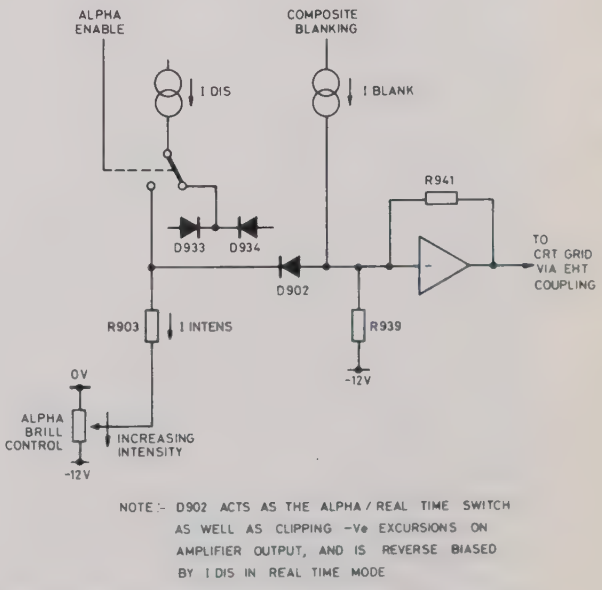


Fig. 4.8.3b Equivalent Circuit of Bright-up System in Alpha Mode.

4.8.5 ALPHA/REAL-TIME SWITCHING

The alpha/real-time switching is controlled by the alpha enable line, which is received as a differential ECL signal by long tailed pair Q901 and Q902. Thus the tail current of this pair (I DIS) is switched to D934 or D902, disabling real-time or alpha intensity.

Contrast current (see Fig. 6.3, Timebase circuit) is provided from a -10V zener supply via analogue multiplexer U1404a, Q1402 and Q1401 on the timebase PCB. Fig.4.8. 3 of the timebase section shows the control inputs to U1404a. If the 'A int B' line is high, and X-Y is low, input 1 (pin 5) of U1404a is active, routing the current via the contrast control. If 'A int B' is low, input 0 (pin 1) of U1404a is used, thus bypassing the contrast control and giving a fixed "1 brill unit" of current. With X-Y high, inputs 2 or 3 are active, R1407 being chosen to give 2 "brill units" of current, thus producing bright-up in the absence of timebases. In 'B displayed' modes, the timebase commutation system applies a low logic level to R1404, cutting off Q1401 and diverting the control current from Q1402 into ground via D1413.

Processor steady-state blanking is provided via R965 and D939 (real-time) or D938 and R964 (alpha). Z mod input is routed via D930, which prevents saturation of Q931 if a negative signal is applied.

Cursor bright-up input is applied as an ECL differential signal to long tailed pairs Q920 and Q921, and Q922 and Q923. The long tailed pairs provide level translation, and drive the output transistors Q924 and Q925 in opposite phase. Schottky diodes D920 and D921 prevent saturation of the output transistors. The high frequency components of the output are fed through C960 to the cathode of the CRT, which is tied to the EHT supply by R961. The low frequency components are filtered by R970 and R955 and C980 and passed to the blanking amplifier, which inverts and applies them to the CRT grid. R970 and R955 in series are approximately equal to the feedback resistor R941, giving unity gain. The parallel value of R955 and R970 forms, with C980, a time constant equal to C960 and R961, so that the differential grid/cathode signal is independent of frequency. See fig. 4.8.4.

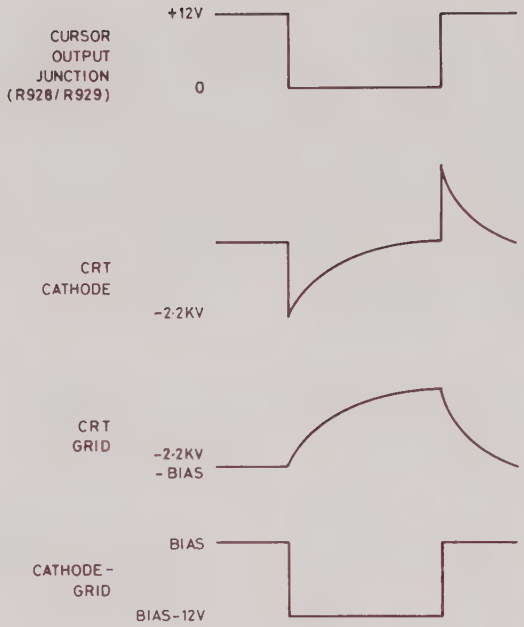


Fig. 4.8.4 Cursor 'Bright-up' Signals

4.9 TIMEBASE

4.9.1 BASIC FUNCTION

The timebase provides a voltage ramp to drive the X amplifier in T-Y modes. Two ramps are provided; 'A', which is the master timebase, and 'B', which is started at, or delayed from, a user specified point on 'A' ramp. 'B' is normally set to a higher speed than 'A', its primary function being to magnify a selected portion of 'A' sweep. 'B' sweeps can only occur during 'A' sweeps and only one 'B' sweep per 'A' sweep is allowed.

Cursor drives are produced by comparing the ramp voltage with outputs from the voltage generator system. See Section 4.7.

The timebase system also provides "bright-up" information to the tube base board to control the flyback blanking, and contrast in 'A' intensified by 'B' mode, see below:

4.9.2 OPERATING MODES

1. **A ONLY.** This is the simplest operating mode; the X amplifier is permanently connected to the A timebase and 'B' is held in rest.
2. **A INTENSIFIED BY B.** The X amplifier is permanently connected to the 'A' timebase, but B ramp is allowed to run, and the trace brightness is increased during the 'B' ramp, so that the portion of 'A' ramp corresponding to the 'B' ramp may be identified.

   The degree of extra bright-up is set by the contrast control.
3. **A AND B ALTERNATE.** The X amplifier is connected to A and B timebase on alternate 'A' sweeps. During the 'A' display sweep, intensification is applied as in (2). The Trace Separate control produces a vertical offset of the 'B' trace in this mode.
4. **B ONLY.** The X amplifier is permanently connected to the 'B' timebase. 'A' timebase is not displayed, but runs in order to produce the starting conditions for 'B'.
5. **X-Y.** In this mode, both timebases are reset, and the X amplifier is connected to the 'A' trigger amplifier (see Section 4.5).

4.9.3 B START MODES

The 'B' ramp may be started by, or delayed from 'A' start, (B not affected by cursors, see menus) cursor 1 or cursor 3 (B1 or B3 see menus) or B trigger. If B1 and B3 are selected (Dual B Mode) 'B' start is controlled by cursor 1 and cursor 3 on alternate 'A' sweeps (As only one B sweep may be generated per A sweep, B1 and B3 do not co-exist). Jitter in 'B' start may be reduced by using 'B' gated modes (B starts after cursor plus trigger or B starts after delay plus trigger) in which the above start events, instead of directly starting 'B' ramp are used to qualify the next B trigger.

4.9.4 GENERAL SYSTEM

Figure 4.9.1 shows a block diagram of the timebase system. The section within dotted lines is identical for 'A' and 'B' ramps. The basic ramp is produced by a programmable constant current generator (Iu) feeding a capacitor system, which can be switched to three values of capacitance. Another current generator (Id) which can provide more than the maximum ramp current, is switched on to produce the flyback by resetting 'A' timebase Gate.

The output of this gate "AQ" is also a major control signal to the rest of the instrument, since many functions are referred to the start of 'A' sweep.

The output buffer consists of a FET input voltage follower with separate outputs for each cursor and for the X amplifier.

At the start of sweep a trigger pulse from the delay system, or the auto input, sets the timebase gate, allowing the ramp to run. During the sweep the end of sweep (E.O.S.) circuit compares the ramp voltage with a preset limit, and, when this limit is reached resets the gate, causing flyback. The hold-off circuit inhibits further sweeps to allow time for the ramp to settle at OV, after which the next trigger pulse causes the process to repeat.

In the absence of trigger pulses a detector on the trigger amplifier sets the auto-line high.

This signal, if selected, re-starts the ramp at the end of the hold off period.

See Section 4.5 for details of trigger.

The single shot circuit, when enabled allows only one sweep following each 'arm' pulse from the processor system.

'B' ramp has no hold off circuit, since it is held off in the absence of 'A' ramp, and also reset if 'A' ends before 'B'.

If 'B' starts after delay is set, a LATCHED 'B' START signal starts 'B' ramp. If 'B' STARTS AFTER DELAY is low (gated B Mode) latched 'B' start qualifies the next 'B' trigger event to start 'B' ramp.

The commutation system controls the switching of the X amplifier source, and provides cursor switching information.

Its dynamic functions are clocked by a signal (timebase clock) from the display management circuit, which provides a clock pulse for every complete sequence of real time channels Ref Section 4.11.

4.9.5 RAMP CURRENT GENERATOR

The ramp current is provided by the collector of Q1234, and controlled by the switched resistor network between pins 1 and 7 of PLV. The voltage across this network is controlled by the level at Q1234 base. This is set by R1272 and R1274 and trimmed by R1275 (which acts as the primary calibration control) via emitter follower Q1235. The variable sweep speed control (R7) modifies the voltage at Q1235 base via R1277, D1236, D1237 and Q1236. In the calibrated position, the wiper of the control connects PLV pin 3 to 4. Q1236 acts as an emitter follower providing current in R7 without appreciably loading the emitter of Q1235 and also referring the variable control to the calibrated voltage at Q1234 base. After a small movement of R7 away from the cal position, the voltage between PLV pins 3 and 4 exceeds the voltage drop across the diodes, and current is drawn through R1277. Further movement of R7 causes the current in R1277 to exceed that in R1271. Q1235 is cut off, and the voltage on Q1234 base rises, reducing the voltage across the resistor network, and hence the ramp current.

4.9.6 RAMP CAPACITORS

The ramp capacitors are switched to provide three clusters of timebase speed ranges. At high speeds 2μs – 50ns U1221c and U1221d are switched off and C1250 provides the ramp capacitance. C1251 allows independent calibration of the top cluster, since its effect on the larger, lower cluster capacitors is negligible. On the middle cluster 0.2ms – 5μs, U1221c is switched on, and the ramp capacitor consists of C1246 and C1245 in series, plus the small capacitance of C1250. For the low speed cluster 0.5s – 0.5ms U1221d is switched on, making C1245 the ramp capacitor.

At the same time, D1233 is forward biased, and Q1233 is turned on, applying ground and supply potentials to R1255 (it is left floating on the other ranges). R1255 now affects ramp current with Q1235 and Q1234, thus providing for independent calibration of the bottom cluster.

When switching from low to high clusters the charge on C1245 is allowed to discharge into C1247 and R1247, and the collector/base diode of U1221d, thus avoiding transient distortion of the top ranges.

D1240 and D1241 provide peak rectification of the ramp signal, preventing negative excursions of U1221c or d collectors when they are switched off. R1250 and R1251 are high values (470K) preventing distortion of the ramp by peak rectifier currents.

4.9.7 FLYBACK CURRENT GENERATOR

The flyback current is provided by a constant current circuit consisting of Q1230, zener diode D1229, and

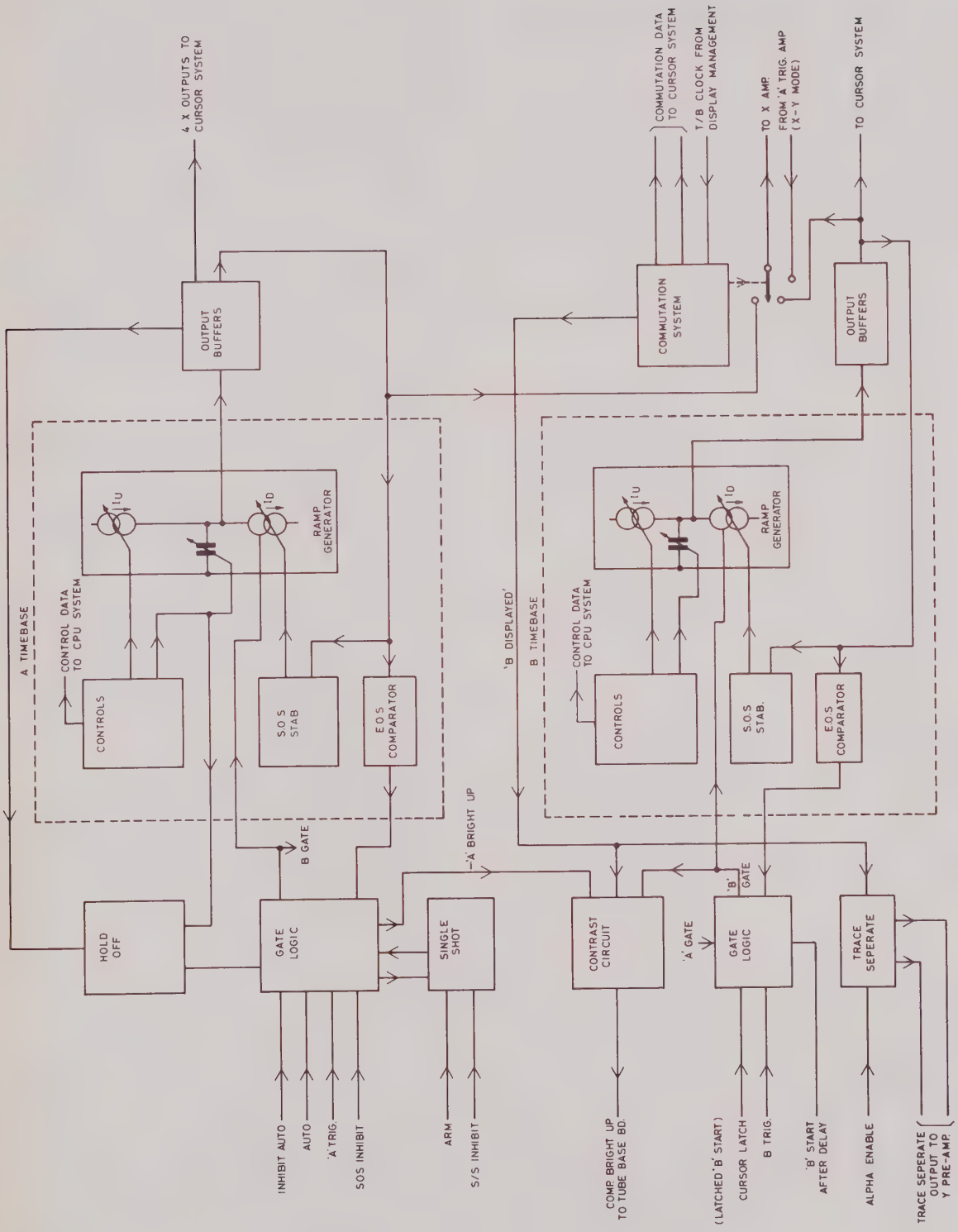


Fig. 4.9.1 Block Diagram of Timebase System

emitter resistor R1237 and may be switched off by diverting the emitter supply of Q1230 into Q1222 via R1277.

4.9.8 OUTPUT BUFFER

The first stage of the output buffer consists of dual FET Q1237/38 connected in "Totem Pole" configuration, in which Q1238 acts as a constant current source for Q1237. Since Q1238 gate and source are joined, and the F.E.T's are matched, the current is just sufficient to maintain the source of Q1237 at the same potential as its gate. Zener diode D1238 is chosen to work the F.E.T.'s at their optimum voltage for minimum distortion. The source follower output is further buffered by emitter follower Q1239, before driving the output stage, a 5 way emitter follower U1222. Four transistors of the array provide the cursor drives, thus buffering the cursor comparators from each other, while providing identical driving conditions for all four.

Cursors 1 and 3 are particularly critical in this respect, since they are used to control the start of B ramp, and any errors are magnified by the ratio of A and B ramp speeds. Since the start of sweep stabilizer (see below) is driven by the fifth transistor in the same pack, all four cursor outputs are accurately stabilized.

The ramp output from U1222 pin 13 is attenuated by R1292 and R1246, and buffered by double emitter follower Q1244 and Q1245. R1269 plus the output impedance of Q1245 provides a 50Ω source impedance for the coax cable which connects the output to a socket on the rear panel.

4.9.9 START OF SWEEP STABILIZER

Q1242/43 form a long-tailed pair comparing the ramp output from U1222 pin 16 with ground. When the ramp is at OV, with 'A' gate (U1201b) reset, part of the current defined by flyback components R1237 and D1229 is diverted from Q1230 emitter, to flow through Q1234 collector, leaving just sufficient current in Q1230 to balance the ramp current from Q1234. Thus the circuit forms a closed loop system, maintaining the ramp output at OV. (When U1201b is reset, Q1230 is switched off by Q1222, so Q1243 has no affect).

Q1231 reduces the loop settling time at high flyback speeds, when the current through C1249 tends to turn on Q1231. At the start of flyback the ramp voltage, attenuated by R1248 and R1249 holds off Q1231, but towards the end of flyback Q1231 turns on, diverting part of the flyback current. This slows the flyback, preventing overshoot (See Figure 4.9.2). R1244 and C1244 are conventional loop stabilizing components.

4.9.10 GATE LOGIC

The gate system is centred on ECL D type latch U1201b, which drives long-tailed pair Q1222 and Q1224. When U1201b is set, Q1222 is turned on, and its collector current, which is greater than the current through R1237, turns off the flyback current from Q1230, allowing the ramp to run.

If U1201b is reset, Q1222 is turned off, enabling the flyback and start of sweep stabilizer circuits and Q1224 is turned on. The current through R1224 produces a signal which is buffered by emitter follower Q1223 to produce the 'A' bright-up signal. The output of U1201b is also buffered by ECL line driver U1208b to provide 'A' gate information to the rest of the system.

4.9.11 START OF SWEEP

Once the hold off circuit has timed out, (see later) U1203 pin 4 is high. If the inhibit start of sweep line (see display management) is inactive, U1203 pin 5 is high, so U1203 pin 2 is high holding the D input of U1201b high via U1202d. A trigger pulse to the clock input of U1201b will now start the ramp.

Feedback from the Q output of U1201b and U1202d holds the D input high, so that trigger pulses do not reset the gate, even when hold off is active. In auto mode, in the absence of trigger pulses, D1205 cathode is high, allowing D1204 to drive the preset input of U1201b. (R1215 and R1218 attenuate the +12V supply to ECL high level) starting the ramp. If normal trigger mode is selected,

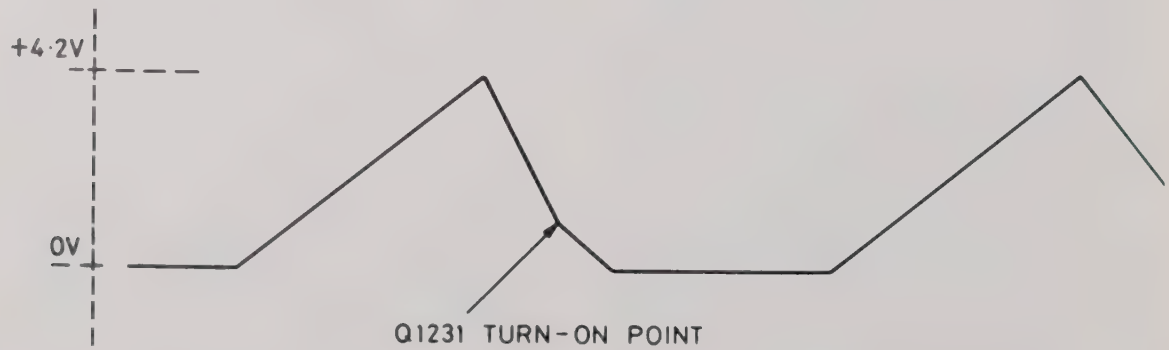


Fig. 4.9.2 Ramp Waveform

BIT	NAME	A ONLY	A INT. BY B	A AND B ALT.	B ONLY	X-Y
DO	RESET B	1	0	0	0	
D2						
D3	A INT. BY B	0	1	1	0	0
D4	A ALT B	0	0	1	0	0
D5	B ONLY	0	0	0	1	0
D6	A ONLY	1	1	0	0	1
D7	EXT X	0	0	0	0	1

Fig. 4.9.3 Output of U1411 Timebase Mode Controls

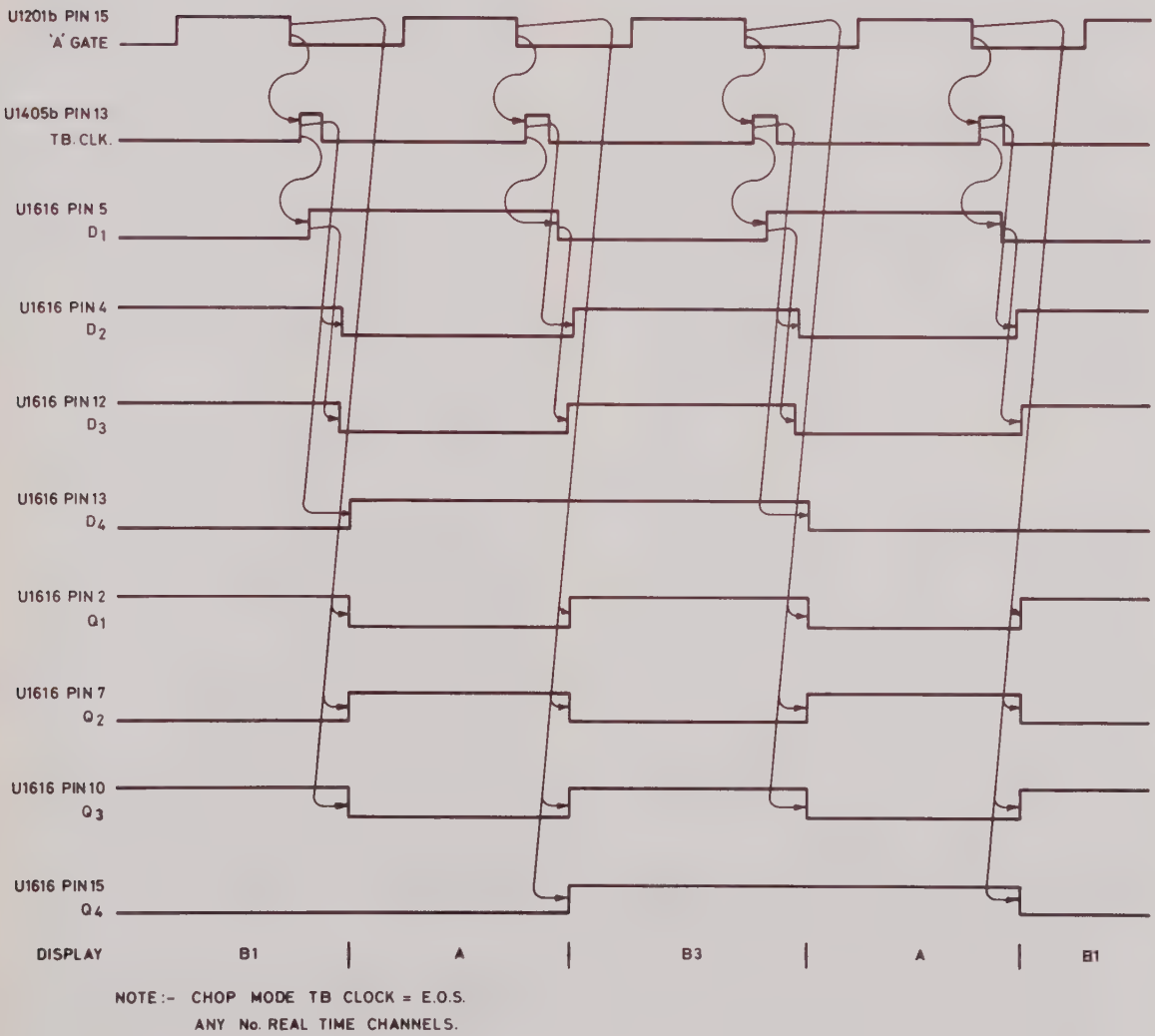


Fig. 4.9.4 Timing Diagram A ALT. B

the inhibit auto trigger from port U1410 pin 6 turns on Q1246 clamping the auto line from the trigger amplifier low. The diodes associated with R1218 form an ECL level AND gate, requiring hold off (D1203) AND SS Set or inhibited (D1207) AND Auto active (D1205) to set U1201b via D1204.

4.9.12 E.O.S. CIRCUIT

During the sweep, a fraction of the ramp voltage is applied to U1202 a Pin 5 via R1213, R1212 and R1211. When this voltage exceeds ECL threshold level, U1202a pin 2 goes high, resetting U1201b via its clear input.

C1212 offsets the effects of delays and stray capacitance, which tends to increase sweep length at high sweep speeds. C1216 provides positive feedback around U1201b to give a clean edge to the "A GATE" signal, particularly at low ramp speeds when a slow edge is received from U1202a.

4.9.13 HOLD-OFF

The basic timing circuit of the hold-off system is similar in principal to the ramp generator. A constant current circuit Q1228 and R1238 charges a switched capacitor system which can be discharged by a greater current from Q1229. The discharge current, which is defined by the -12V supply across R1230, may be modified by the variable hold-off control, via R1229.

The ramp from Q1239 emitter is shifted down towards the -12V supply by R1252 and R1253. When the junction of these resistors goes positive, at about half the sweep period, D1231 is turned on, removing the drive to Q1229 emitter, and allowing the hold-off capacitor to charge, see Fig. 4.9.5. The rising voltage on R1234 cuts off Q1225, and allows R1232 to pull down the hold-off line to U1203 pin 4. This sets the D of U1201b low via U1203a and U1202d, thus preventing trigger pulses from starting

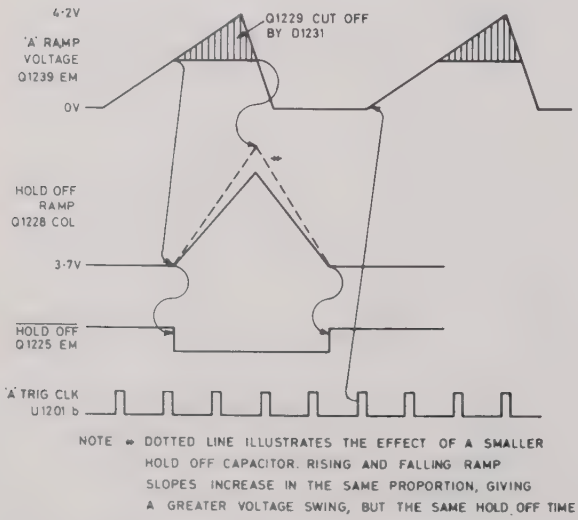

4·2V
'A' RAMP VOLTAGE Q1239 EM
0V
Q1229 CUT OFF BY D1231
HOLD OFF RAMP Q1228 COL
3·7V
HOLD OFF Q1225 EM
'A' TRIG CLK U1201 b
NOTE ⇔ DOTTED LINE ILLUSTRATES THE EFFECT OF A SMALLER HOLD OFF CAPACITOR. RISING AND FALLING RAMP SLOPES INCREASE IN THE SAME PROPORTION, GIVING A GREATER VOLTAGE SWING, BUT THE SAME HOLD OFF TIME

Fig. 4.9.5 Timing Diagram for a Ramp Hold Off Circuit

the ramp. At the same time, the low level on U1203 pin 2 holds down D1203, inhibiting the auto trigger circuit. The hold off capacitor continues to charge until, during the main ramp flyback, D1231 is cut off, turning on the current source Q1229. The hold-off capacitor now discharges at a rate determined by the variable hold-off control. After a time at least sufficient for the ramp to settle at 0V, Q1225 is turned on, pulling up R1232 and allowing the next sweep to start.

D1226 now carries the current from Q1229 collector, clamping the hold-off capacitor voltage, and also preventing saturation of Q1225. Note that the hold-off time does not depend upon the value of the hold-off capacitor since changing the capacitance changes both rising and falling ramp slopes proportionally but is approximately proportional to the sweep time, and dependent upon the ratio of charge to discharge currents.

However, the voltage swing at Q1228 collector depends upon ramp speed, and to avoid saturation of Q1228 at low speeds, and insufficient swing to drive Q1225 at high ramp speeds, the capacitor values are switched by U1221a and b in a similar manner to the main ramp capacitors. At very low ramp speeds, to avoid excessive hold off periods, the proportionality is lost by choosing C1226 so that, in this extreme, Q1228 saturates, preventing any further increase in hold-off time. C1210 provides positive feedback during transitions of the hold-off line, to give a fast edge on the D input of U1201b. The edge speed is further improved by local feedback around U1203a via C1209.

4.9.14 SINGLE SHOT

In single shot mode, the single-shot line from port U1410 pin 10 is low. An 'Arm' pulse from U1410 pin 9 sets U1201a via C1206. U1202a Pin 4 is thus low allowing timebase operation as described above. At the end of sweep, U1201a is clocked by $\overline{AQ}$. The D input of U1201a is low, so its $\overline{Q}$ is clocked high, applying a reset to U1201b via U1202d thus preventing further timebase sweeps until another 'Arm' pulse is received. As single-shot is low R1206 and R1207 maintain the base of Q1201 below ECL threshold level. Thus, when U1201a is armed, Q1201 conducts, turning on the 'armed' LED via R1210. When single-shot is high, U1201a is held permanently set via D1202, allowing unlimited timebase sweeps and Q1201 is turned off via D1208. The time constant of C1206 and R1201 is less then the fastest sweep time, ensuring that the 'arm' pulse on U1410 pin 9, which lasts for several microseconds, does not cause multiple sweeps. D1201 prevents the preset input of U1201a from being driven negative by the back edge of the 'Arm' pulse.

4.9.15 MANUAL TRIGGER

Manual trigger is achieved by selecting single shot and auto mode. When the single shot is armed, the auto circuit

starts the ramp immediately via the preset input of U1201b. The emitter of Q1247 is held at one Vbe above ECL threshold by R1289 and R1290. Thus, when U1201b is clocked low at the end of sweep, Q1247 is turned on, which in turn drives Q1246, inhibiting the auto circuit until the single shot circuit is re-armed.

4.9.16 'B' TIMEBASE

The 'B' ramp generator will not be described in detail, as it is generally similar to 'A'. The output stage does not have the critical requirements of cursors 1 and 3 referred to under 'A' ramp, so the five way emitter follower circuit is simplified to a single transistor Q1340. The start of sweep stabilizer has a fine adjustment, R1391, to allow exact matching to 'A' ramp. No hold off is required, as 'B' ramp is held off by 'A' gate. The main difference from A ramp concerns the method of driving 'B' gate, U1304a, to control 'B' ramp. Since $\overline{AQ}$ from U1201b drives the clear input of U1304a via U1202b, B ramp can never run when A ramp is not running. B ramp has its own reset system via R1313, R1312, C1312 and R1311, but is also reset if 'A' ends before 'B'. 'B' gate is held reset by the 'reset B' line from port U1411 pin 12 in "A only" and X-Y modes.

4.9.16.1 A STARTS B

With A ramp reset, U1304b is set by $\overline{AQ}$ on its preset input. This would drive the $\overline{Q}$ of U1304b low, but is held high by the wired -or connection to U1202b, which also has $\overline{AQ}$ as an input. As $\overline{AQ}$ goes low to start A ramp, U1202 pin 3 goes low putting a low on U1306a pin 4. In this mode, U1306a pin 5 is held low by the $\overline{\text{ENABLE A, STARTS B}}$ signal from port U1410 enabling U1306 pin 2 to go high and as the AQ input to U1203b is already high, 'B' gate is set via its preset input (U1304 pin 4).

4.9.16.2 B STARTS AFTER DELAY

In this mode, B ramp starts when the cursor latch is set. This may be set by cursor 1, cursor 3 or the delay system (ref cursor system, delay system). $\overline{\text{B STARTS AFTER DELAY}}$ from port U1410 is low, driving Q1349. R1385 and R1387 define an ECL high level, holding the D input of U1304a high via U1306c. The clock of U1304a is now driven by the $\overline{\text{LAT B}}$ cursor signal to U1306b pin 6, since U1306b pin 7 is low, starting B on latch.

4.9.16.3 GATED B START

The cursor latch is used to gate 'B' trigger, ie: 'B' starts on the first 'B' trigger pulse after the cursor latch is set. 'B Trigger' may be the output of the 'B' trigger amplifier or the delay system, and the latch may be set by the cursor or delay system, giving a wide range of possible 'B Start' options. (Ref Menus, fig.4.6.1, block Diagram of Delay System) $\overline{\text{B STARTS AFTER DELAY}}$ is high, inhibiting U1306b but enabling 'B' trigger pulses from U1306d wire-or'ed to U1304a clock. U1202c pin 10 is low, so the D input to U1304a is controlled by the 'LATCHED B START' SIGNAL, which thus gates the B trigger pulses on U1304 clock.

Note that the wired-or connection to U1304a clock minimises logic stages and, therefore B trigger propagation delays.

4.9.17 'B' RAMP SINGLE SHOT

'B' ramp is only allowed to make one sweep per 'A' sweep. When 'A' ramp is reset, U1304b is set by the $\overline{AQ}$ signal on its preset input. During 'A' ramp, this input ($\overline{AQ}$) is low and, if a 'B' sweep occurs, the $\overline{Q}$ output of U1304a clocks U1304b. As the D input of U1304b is permanently low, its $\overline{Q}$ is clocked high, putting a clear on U1304d, and preventing further B sweeps, until A ramp resets.

4.9.18 'B' GATE OUTPUT

The 'B' bright-up signal is derived in the source way as 'A' via Q1323, but on the 'B' side, the signal is also taken to the rear panel as the 'B' gate output.

R1389 combined with the output impedance of Q1323 forms a 50Ω drive to the coax cable.

4.9.19 TIMEBASE CLOCK

This signal is derived from the display management circuit. As explained under ALTERNATE mode in the display management section, terminal count indicates the end of a complete cycle of real-time sweeps. In chop mode, all channels are displayed on every sweep, so in this case, End of Sweep represents the end of a real-time sequence. Gates U2406a and b and U2437b produce a signal corresponding to terminal count in ALTERNATE mode, and End of Sweep in Chop.

This signal (timebase clock) thus always represents the end of a complete sequence of Y channel displays.

4.9.20 COMMUTATION CIRCUIT

The commutation system is based on Dual D latch U1405, of which the 'a' section selects A or B ramp displayed (ie connected to X Amplifier) and the 'b' side, in conjunction with the cursor management system, decides which of cursor 1 and 3 controls the start of B ramp. As there is considerable propagation delay in the generation of timebase clock, the outputs of U1405 are re-synchronized to $\overline{AQ}$ by quad D latch U1616. Comparator U1614a converts the ECL gate signal from U1201b (AQ) to CMOS level. As cursors may be enabled on 'A' or 'B' ramps the cursor management requires dynamic information about which ramp is currently being displayed. This is provided by the 'A' DISPLAYED signal from U1616 $\overline{Q1}$. Q4 and $\overline{Q4}$ provide "B to start on cursor 1 or 3" information to the cursor system. Note that toggling this pair of control lines does not necessarily control B by cursor 1 and 3 alternately, the information is sent to the cursor management system, where its use will depend upon whether the user selects B1, B3 or both. The Q1 output of U1616 drives input A of analogue multiplexer U1409b, which selects the X amplifier input signal (U1409a and b are wired in parallel to reduce switch on impedance).

When the SELECT EXTERNAL X signal to the B input of U1409b is low, the A input selects input IN0 or IN1, i.e. A or B ramp. If select EXTERNAL X is high, the inputs selected are IN2 or IN3, both of which are connected to the A trigger amplifier.

The detailed operation in each mode, which follows, should be read with reference to truth table (Figure 4.9.3).

4.9.20.1 A ONLY

U1405a is held in reset, giving 'A' only displayed, U1405 toggles, but is irrelevant as 'B' ramp is held reset.

4.9.20.2 A INT. B

As A only, except that B ramp is not reset, and therefore provides a bright-up signal via R1403.

4.9.20.3 A ALT B TRACE SEPARATE

(See Fig. 4.9.4). Preset and clear of U1405 are both low, J and K are high, so the latch toggles on every timebase clock pulse. U1617c is enabled by the A ALT B line, so U1405b toggles on alternate clocks, to form a ÷ 4 system with the sequence A,B1,A,B3. In A ALT B mode, a Y shift is applied during the 'B' displayed phase, to allow easy visual identification of the two displays. The degree of Y shift is determined by the TRACE SEPARATE control. As the shift is applied after the Y beam switches, it is necessary to disable it during the alpha phase, to avoid a double image of all alpha functions. The output of the trace separate control, on PL BW pin 3, is attenuated by R1420 and R1424, and applied to long-tailed pair U1408c and U1408d, whose outputs provide the trace separate current to the Y O/P module. The tail current of the long-tailed pair is controlled by emitter switch pair U1408a and U1408b, which are driven by the differential outputs of ECL AND gate U1203d. When pin 2 of U1408 is driven high, and pin 4 low, the differential trace separate current is switched off, and an equal current applied to the Y pre-amplifier via R1421 and R1424 to maintain the same common mode level. As shown in Figure 4, in A ALT B mode, Q3 of U1616 is high when A is displayed, and $\overline{Q3}$ when B is displayed. Thus the input to U1203d via D1408 switches the trace separate on during the B phase. In all other horizontal modes the A ALT B input to U1617c is low, so the D3 input of U1616 is high, and $\overline{Q3}$ low, disabling trace separate. The input to U1203d pin 13 disables trace separate during the alpha display phase.

4.9.20.4 'B' ONLY

U1405a is held in preset, displaying 'B' only. 'A' ramp still runs, to provide the starting conditions for 'B', but is not displayed. U1617c is disabled by A ALT B, driving J and K of U1405b high. Thus U1405b toggles on every clock pulse, allowing the cursor management to select cursors 1 and 3 alternately if required.

4.9.20.5 X-Y

U1616 outputs have no effect, as they are overriden by the SELECT EXTERNAL X input to U1409, as already described.

4.10 X–OUTPUT

4.10.1 BASIC FUNCTION

The X output circuit amplifies the ramp and alpha X inputs to a level sufficient to drive the CRT deflection plates, and provides for beam switching between alpha and real-time inputs. The real-time gain is switchable between x1 and x10, to give X expansion.

4.10.2 OPERATING MODES

The system has three operating modes, alpha, real-time x1 and real-time x10.

4.10.3 GENERAL SYSTEM

Fig. 4.10.1 shows a block diagram of the X output system. The CRT plates are driven by a pair of shunt feed-back amplifiers, whose inputs are switched between alpha and real-time tail circuits by a high speed diode switch, capable of operating at chop frequency. There are two real-time tails, which are selected by switching their emitter currents. This is a manual selection via the processor, so does not require fast response. The X shift is driven by an output from the voltage generator system via an op-amp, which provides scaling and level shifting.

4.10.4 CIRCUIT DETAILS

The CRT driving section consists of two identical, shunt feed-back amplifiers working independently. Only one side will be described. Emitter follower Q1909 drives cascode pair Q1910, Q1907 whose operating potential is set by zener diode D1920 form a constant current

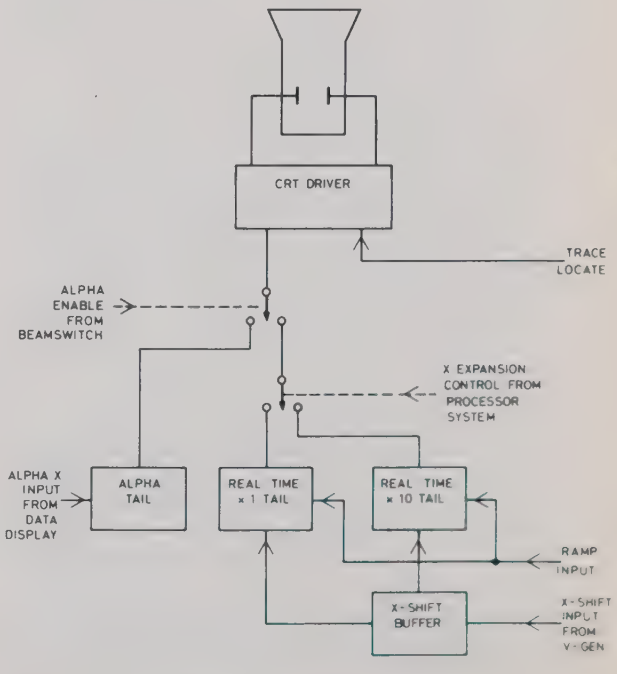


Fig. 4.10.1 X Output Block Diagram

circuit as the collector load of Q1907. At high frequencies Q1905 emitter is driven via C1909 and C1910, to improve the positive slew rate performance.

Overall gain of this section is controlled by shunt feedback resistor R1918, producing a virtual earth at the base of Q1909. C1936 provides local feedback at high frequencies, to improve loop stability.

R1919 and C1907 partially bypass the emitter follower at high frequencies, to further improve the gain and phase margins of the loop. A small fraction of the output is tapped off by capacitive potential divider C1904 and C1906, and fed back to the input via C1941 to adjust the overall pulse response.

Zener diode D1921, which is supplied from the -120V supply by R1927, is used to provide the correct mean-plate-potential of +30V, which is 33 volts below the working point of the amplifier.

The beam switch consists of a diode switch system driven by emitter switch pair Q1901 and Q1902, which provide a level translation from the ECL alpha enable line to approximately +7 volts at the virtual earths. Fig.4.10.2 shows part of the beam switch system extracted from the main circuit diagram for clarity. R1987 and R1988 are chosen so that IBIAS is equal to ITAIL plus the mean switching diode current, so that the total current in R1908 and R1909 is zero. Thus the collectors of Q1901 and Q1902 swing equally above and below the voltage Vz defined by zener diode D1909. Since the Vbe's of Q1909 and Q1910 are of opposite polarity, the virtual earth potential is also approximately Vz. In alpha mode, Q1902 conducts and Q1901 is cut off. Thus the anode of D1906 is below Vz allowing D1904 to conduct, connecting the alpha tail to the virtual earth. The anode of D1911 is above Vz, cutting off D1919 and disabling the real-time tails and diverting the real-time tail current via D1911 into R1987. In real-

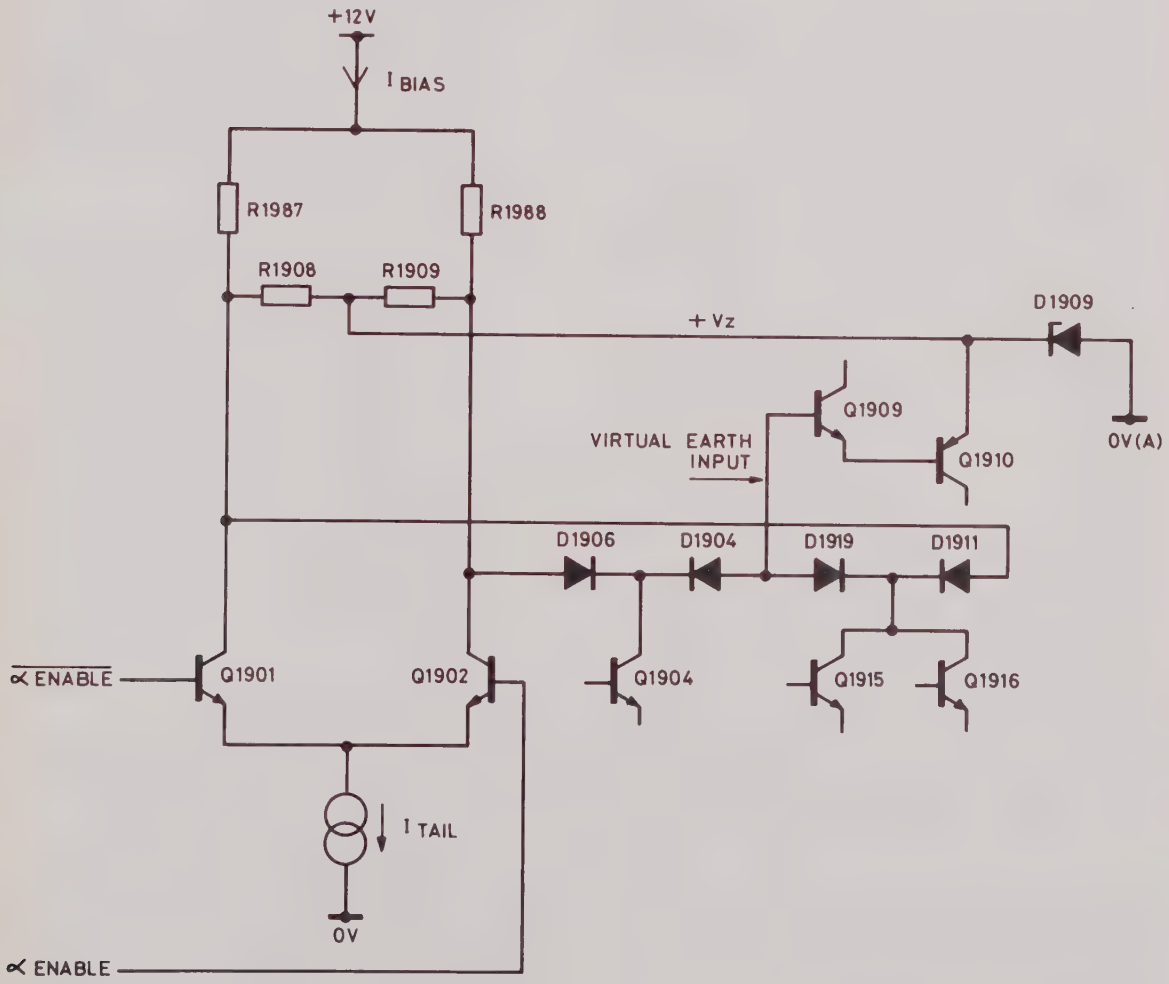


Fig. 4.10.2 X Beam Switch Driver and One Half of Beam Switch

time mode, Q1901 conducts, Q1902 is cut off and the above situation is reversed, enabling real-time signals via D1919 and diverting the alpha tail current via D1906. D1903, 5, 10, 12 perform a similar function for the other virtual earth (Q1912 base).
Note that all signals, being currents, pass undistorted through diodes into the virtual earth.

X expansion is controlled by emitter switch Q1920 and Q1921, which are driven by the processor system via R1968. If the $\overline{x10}$ control line to R1968 is high, Q1920 is cut off, and the current from R1965 passes via Q1921 to R1959. This produces a well defined potential across R1959, and turns on the constant current source consisting of Q1918 and its emitter components. D1922 compensates for the Vbe of Q1918, making the current source independent of temperature. Q1918 provides the tail current for long-tailed pair Q1913 and Q1916, which receive the ramp input via R1944 and shift input via R1952. The constant current from Q1918 (x1 tail), which is set by R1961, controls the common mode current into the output amplifier, and hence the mean X plate potential. Using a constant current source also provides the amplifier with a high degree of common mode rejection, which is necessary, as the ramp drive is single ended. R1946 controls the overall gain in x1 mode.

In x10 mode, the input via R1968 is low, Q1920 is switched on and Q1921 is off. Thus there is no current through R1959, Q1918 is cut off, disabling the x1 tail. The x10 pair, Q1914 and Q1915 are now enabled via constant (x10 tail) current source Q1919. The mean plate is set by R1963, and the gain by R1948.

R1939 and R1940 form common collector loads to both x1 and x10 tail sections. Since the tail transistors can be cut off during parts of the ramp which are shifted well off screen, schottky diodes D1915–1918 are used to clamp the collectors, avoiding a large voltage swing and excessive recovery time.

The alpha tail system, Q1903, Q1904 and associated components, which is permanently energised, is somewhat simpler than the real-time tails.

The drive is symmetrical, so no constant current circuit is required, also the input never overloads the amplifier, so there are no schottky clamps. Alpha gain and mean plate potential are set by R1915 and R1917.

The X shift output from the voltage generator is applied to the real-time tails via operational amplifier U1902. The shift system requires a swing of 0 to +4 volts, whereas the voltage generator provides ±4 volts approximately. Film network N1901, and +2V bias from the cursor system, provide the required scaling and level shifting.

4.10.5 TRACE LOCATE

When the trace locate button is operated, R1970 is connected to +12V, and the resulting current through D1913 and D1914 diverts part of the tail current, leaving insufficient current to allow the trace to be driven off screen.

4.11 DISPLAY MANAGEMENT

4.11.1 BASIC FUNCTION

The instrument uses a single beam CRT to display real-time traces, stored traces, and alpha–numeric information. These functions are time-multiplexed to the CRT deflection amplifiers by the display management system. This system also provides a signal to the CRT grid, via the blanking amplifier, to blank the beam switch transistions.

All non real-time functions will be referred to as the "alpha" mode (alpha-numeric and trace replay). This mode changes X, Y and blanking amplifier signal sources, whereas CH1, CH2 and Trig. View affect Y only

4.11.2 OPERATING MODES

In order to provide the alpha functions with a minimum of interference with real-time time traces, the display management operates in three modes, depending upon timebase speed and trigger frequency:-

1. At low sweep speeds (0.5ms and below) CHOP mode is selected. In this mode, the display cycles around all required functions in a total cycle time of 4μs. As may be seen in the timing diagram Fig. 4.11.2 the first 1μs of each cycle is permanently allocated to alpha mode, and the remaining 3μs. are divided between the required real-time channels.
2. At high sweep speeds CHOP mode would produce a discontinuous trace, so the instrument is normally switched to ALTERNATE mode, in which each required real-time channel is displayed for one timebase sweep. Every 15ms an "alpha request" is latched. At the end of the current cycle of real-time sweeps, the request is acknowledged, allowing one scan of the alpha functions.
3. In ALTERNATE mode, at low trigger rates, the real-time channels may not complete a sequence within 15ms. If another alpha request occurs before the previous one is acknowledge, the system goes into FORCED ALPHA mode, and an alpha scan occurs immediately, or at the end of the current timebase sweep if one is in progress.

4.11.3 BLOCK DIAGRAM GENERAL

Fig. 4.11.1 shows a block diagram of the display management system. The channel beam switches are controlled by a variable configuration shift register, each register stage corresponding to a particular display function; in order alpha, CH1, CH2, Trig. View. Analogue gates, which are set up by the processor during channel selection, route a logic '1' through each register stage, or bypass it as required.

The register clock signal, which produces the beam switch transitions, is preceeded by a blanking pulse, to

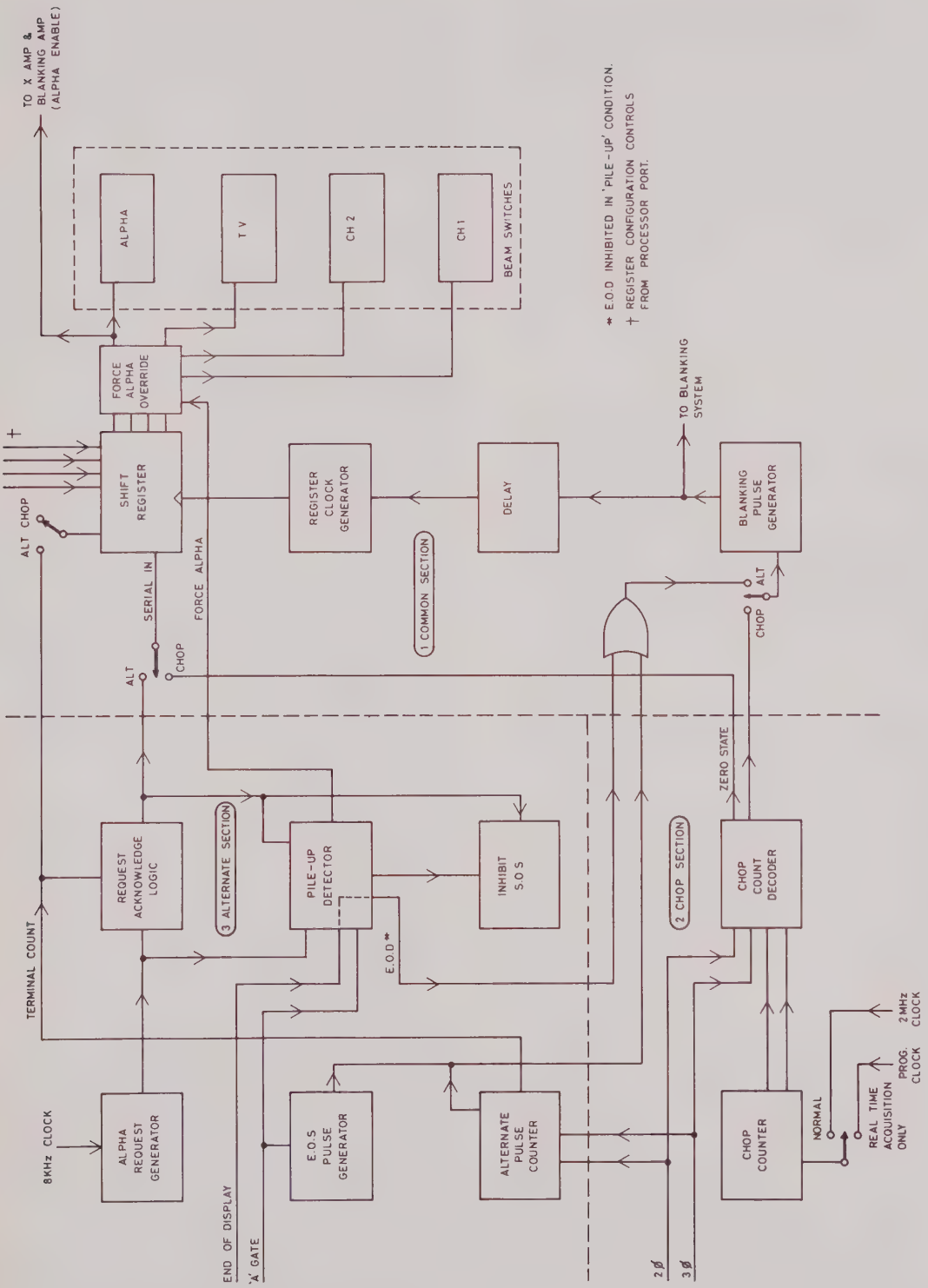


Fig. 4.11.1 Display Management Block Diagram

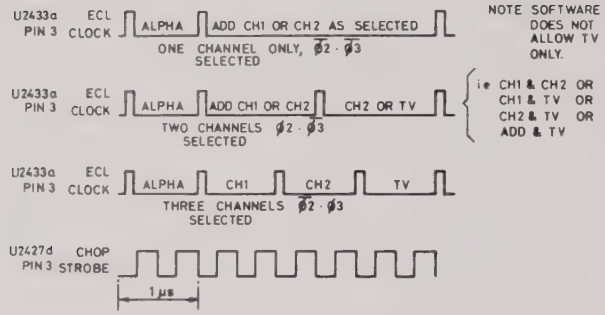

U2433a PIN 3 ECL CLOCK
ALPHA
ADD CH1 OR CH2 AS SELECTED
ONE CHANNEL ONLY, Φ2 · Φ3 SELECTED
NOTE SOFTWARE DOES NOT ALLOW TV ONLY.
U2433a PIN 3 ECL CLOCK
ALPHA
ADD CH1 OR CH2
CH2 OR TV
TWO CHANNELS Φ2 · Φ3 SELECTED
ie CH1 & CH2 OR CH1 & TV OR CH2 & TV OR ADD & TV
U2433a PIN 3 ECL CLOCK
ALPHA
CH1
CH2
TV
THREE CHANNELS Φ2 · Φ3 SELECTED
U2427d PIN 3 CHOP STROBE
1μs

Fig. 4.11.2 ECL Register Clock Patterns set by Φ2 & Φ3 Control

allow time for the blanking amplifier to cut off the beam. In CHOP mode, the blanking and register clock system is driven by the CHOP decoder (see Fig.4.11.2 for details of decoder pattern). The CHOP counter is driven by a 2MHz signal, which is thus the master clock signal in CHOP mode.

In ALTERNATE mode the system is clocked either by the END OF SWEEP (EOS) pulse, which is derived from 'A' timebase gate at the end of 'A' sweep, or by the END OF DISPLAY pulse produced by the data display circuit when all required alpha functions have been scanned.

FORCED ALPHA mode inhibits register clock pulses, and drives the alpha beam switch directly from the "pile-up" detector circuit, overriding the shift register.

The block diagram (Fig.4.11.1) has been divided into 3 sections:-

1. Units common to CHOP and ALTERNATE mode.
2. Units used in CHOP mode only.
3. Units used in ALTERNATE mode only.

These sections will now be described in details (see also Fig.4.11.1).

4.11.4 BEAMSWITCH CONTROL SECTION

The shift register which drives the beam switches consists of ECL Dual 'D' latches U532 and U534, linked together as required by analogue gates U531 and U533. Control lines L, M, N, CHOP/ALT, TV and their complements set up the register configuration according to the channel selections. Fig.4.11.3 shows the settings for all possible combinations of channels.

A logic '1' may be introduced into the first (alpha) register stage via ECL line receiver U536b and "serial input". This input is used in CHOP mode. In ALTERNATE mode, the logic '1' is introduced into the second stage via "I.ALT". U531a is off, isolating the first stage, which is only driven following an alpha request. The shift register outputs drive the beam switches via ECL gate U535. Note that the alpha beam switch is connected in the opposite sense from the other three, so that a high logic level on pin 12 forces alpha mode, and inhibits the other channels, regardless of the shift register state.

To assist rapid recovery from false operating conditions, e.g. at start-up and following a change of channel selection, the shift register does not form a closed loop. The logic '1' is discarded at the end of each real-time sequence and a new one introduced at a time controlled by counter U2446 (section a in chop, b in alternate). To maintain continuity, the number of register clock pulses between the introduction of successive logic '1's into the register must be equal to the number of active stages in the register. Port lines "DUAL CH", "2 Φ" and "3 Φ" from U2412 are used to simplify the decoding of the counter outputs for this purpose.

Fig. 4.11.3 shows the outputs from U2412 for all possible channel selections, from which the following points may be noted:-

a) 2Φ is set if any 2 (and 2 only) real-time channels are selected.

b) 3 Φ is set if all 3 real-time channels are selected.

c) DUAL is set if CH1 and CH2 are selected.

d) All lines are clear if one real-time channel is selected.

LINE	BIT	MODE								
		CH1	CH2	T.V.	ADD	CH1.TV	CH2.TV	ADD.TV	DUAL	DUAL.TV
DUAL	Do	0	0	0	0	0	0	0	1	1
2Φ	D1	0	0	0	0	1	1	1	1	0
3Φ	D2	0	0	0	0	0	0	0	0	1
CHOP	D3	HIGH IN CHOP, LOW ALTERNATE								
TV	D4	0	0	1	0	1	1	1	0	1
L	D5	0	1	0	1	0	1	1	1	1
M	D6	0	1	1	1	0	1	1	0	0
N	D7	1	0	0	1	1	0	1	1	1

Fig. 4.11.3 Control Lines from Port U2412 on Display Management PCB

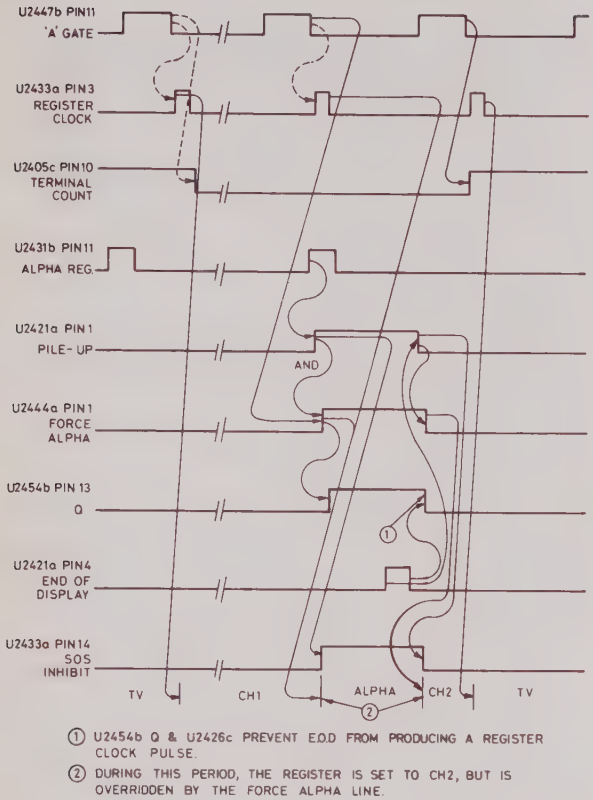


Fig. 4.11.4 Timing Diagram Three Channels alternate Mode with Forced Alpha.

CHOP/ALTERNATE CONTROL LINE. Certain sections of the circuit are specific to CHOP or ALTERNATE mode only. The CHOP/ALT signal from port U2412 is inverted by U2422b so that both polarities are available to qualify each section as required.

4.11.5 BLANKING AND REGISTER CLOCK GENERATOR

Depending upon operating modes, "END OF SWEEP", "END OF DISPLAY", or the output of the CHOP decoder circuit, are applied to the clock input of TTL 'D' type latch U2455b. Following each positive clock edge, a blanking pulse is produced by a monostable circuit as follows:-

As the 'D' input of U2455b is permanently high, Q is clocked high. This signal is inverted by U2445d, and, after a delay of ~150ns set by R2434 and C2404, and pulse shaping by Schmitt buffers U2445b and c, is applied to its own RESET input.

Following the leading edge of the blanking pulse, R2433 and C2405 provide a preset delay, to allow for the blanking amplifier response time, before the register clock pulse is produced by another monostable based on U2455a. ECL line driver U2433 is used to convert the TTL signal to differential ECL level for transmission to the Y pre-amp PCB, where it is received by ECL line receiver U536, to drive the register clock inputs.

4.11.6 COMPOSITE BLANKING - See also Section 4.8

The data display board produces a FLY-BETWEEN BLANKING signal as the beam moves between successive display points. This CMOS signal is converted to ECL compatible level by D2404, inverted by U2407b, and qualified for alpha mode only by U2407d before being ORed with the CHOP BLANKING signal from U2407a by U2407c, and transmitted as a differential ECL signal to the tubebase board.

The CHOP BLANKING signal is also produced in ALTERNATE mode, following, END OF SWEEP, but has no effect, since there is no BRIGHT-UP from the timebase during this time.

4.11.7 ALPHA ENABLE LINE

The drive to the alpha beam switch is also a major control signal to the rest of the instrument, driving the X amplifier and blanking/bright-up system into the alpha mode.

It is also returned to the display management board, where it qualifies the fly-between blanking from the data display board for alpha phase only, as part of the COMPOSITE BLANKING signal. An inverted, TTL version synchronises the ALPHA REQUEST generator, and is transmitted as the display board as the START $\overline{\text{ALPHA}}$ signal.

4.11.8 CHOP MODE

A chop strobe signal (which is normally a 2MHz clock signal) is used to clock counter U2446d. The fourth stage of the counter is not used, outputs 0–2 are decoded according to the signals on 2Φ and 3Φ control lines, to appear at U2437 pin 10. To eliminate glitches produced by the decoding process, the output is gated by the chop strobe signal via U2416b (which allows this clock source for CHOP mode only) and U2416a.

The decoded output is applied to the blanking and register clock generator via U2456c. Fig. 4.11.2 shows the clock patterns produced for all valid combinations of 2Φ and 3Φ.

Count state zero is decoded by U2525 and passes via U2416d and U2405a to provide the logic '1' at the shift register input. U2446 also provides a MEM CLOCK signal, at half the CHOP STROBE frequency, to control the acquisition system, see next section.

4.11.9 REAL-TIME ACQUISITION

Certain functions of the CHOP section of the display management are modified during real time acquisition. Note that all arrangements described under this heading exist only during the timebase sweep following an acquisition request. When acquisition is completed, the processor returns the system to normal mode operation. See also section 4.13.

A control signal from port U2411 to U2422c, U2427a and b changes the chop strobe frequency from 2MHz to "PROG CLOCK". The processor selects the frequency of "PROG CLOCK", using information about timebase speed and channel selection, to acquire the equivalent of 100 samples per cm of one or both realtime channels as required (TRIG VIEW is not sampled).

In dual real time acquisition TRIG VIEW and alpha functions are inhibited, and the number of CHOP STROBE pulses in the real-time cycle is halved in order to obtain maximum sampling speed. The processor selects 3Φ although only 2 channels are active (an exception to the normal rules, see Fig. 4.11.4). This produces a register clock pulse on alternate PROG CLOCK pulses in synchronism with MEM CLOCK to the acquisition system (see Fig. 4.11.2). Transmission gate U2444d is enabled in this mode, so that, on alternate register clock pulses, the Q1 output of the chop counter U2446a provides a logic '1' at the second stage of the shift register, bypassing the alpha section. Thus the logic '1' is propagated through only the middle two sections of the shift register, selecting channel 1 and channel 2 alternately. The normal decoding process still produces a logic '1' at the alpha input to the register, but this is disabled by holding the first stage in reset via D401. U2406d pin 13 is high in this mode, so COMP TRIG does not effect 2Φ and 3Φ control lines, but the processor disables Trig View.

In single channel real-time acquisition, the processor actually forces the system into ALTERNATE mode. In this case, the above modifications to the CHOP STROBE input are made simply to provide the correct MEM CLOCK frequency to the acquisition circuits.

4.11.10 ALTERNATE MODE

Since, in this mode, there is not normally an alpha scan for every real-time sequence, the first stage of the shift register is isolated by U531a and treated as a separate entity. The remaining three stages are configured in the normal way (Fig. 4.11.4) with a logic '1' introduced into the second stage via U2444c. Register clock pulses are produced by END OF SWEEP or END OF DISPLAY pulses as described below.

4.11.10.1 BASIC OPERATION WITHOUT ALPHA REQUESTS

At the end of 'A' timebase sweep, 'A' timebase gate closes, and END OF SWEEP pulse of ~300μs width is produced by a monostable consisting of CMOS 'D' type latch U2447b and feedback components R2408, C2402 and C2403 (operation as described for U255b).

The END OF SWEEP pulse is routed via U2456b (which ORs it with END OF DISPLAY) and U2426b (which allows this pair of clock sources for ALTERNATE mode only) to produce blanking/register clock.

U2446b, and the logic network feeding back to its MR input, form a programmable ÷ N counter controlled by 2Φ and 3Φ to make N equal to the number of real time channels. This counter is clocked by the END OF SWEEP pulse, as is the register in this mode. Thus the cycle time of the counter is equal to propagation time through the register. The terminal count output of the counter, at U2405c pin 10, is routed via U2414c, U2451a and U2444c to provide a logic '1' to the shift register input as the previous one is discarded at the end of the register. Thus TERMINAL COUNT marks the end of a complete sequence of real time events.

In the special case of only one real time channel being selected, 2Φ and 3Φ are low, thus isolating the counter outputs via U2435a and b, but U2425b is high, so the REGISTER CLOCK pulse to U2435c provides one TERMINAL COUNT pulse for every END OF SWEEP pulse. Figs. 4.11.5–7 show the timing diagrams for 1, 2 and 3 real-time channels.

4.11.10.2 ALPHA REQUEST GENERATOR

U2441 and feedback gates U2451c and d form a ÷ 90 counter, which is clocked by an 8kHz signal from the CPU board, and produces the ALPHA REQUEST signal at U2441b pin 14. One input of U2451d has the START ALPHA signal applied via U2424c, thus holding the counter reset during the alpha scan. This particularly synchronises the ALPHA REQUEST signal to real-time events, and reduces flicker at critical trigger rates.

4.11.10.3 NORMAL INSERTED ALPHA (HIGH TRIG RATE)

Dual D latch U2431, and S.R. Latch U2414a and b form a "request acknowledge" unit, to synchronise ALPHA REQUEST to the next TERMINAL COUNT.

In ALTERNATE mode, the D input of U2431b is held high by U2426d while the processor allows alpha via U2411 pin 12, so the ALPHA REQUEST signal from U2441b clocks the Q of U2431b high. The next TERMINAL COUNT sets U2431a, and this Q output, after a dekay set by R2481 and C2451, resets U2431b.

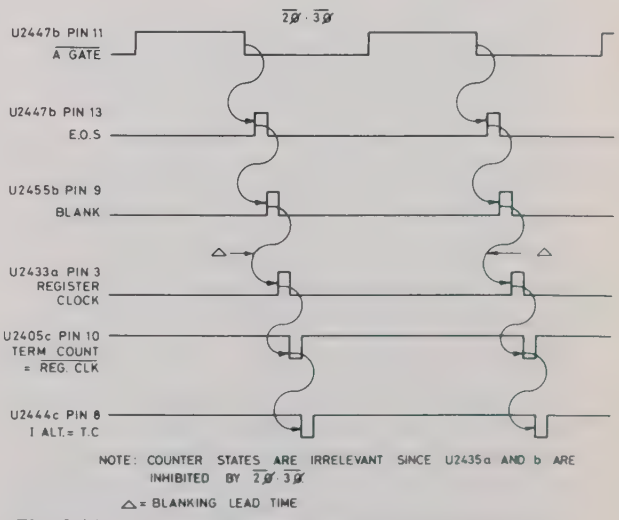


Fig. 4.11.5 Timing Diagram Single Channel alternate Mode without Alpha Request.

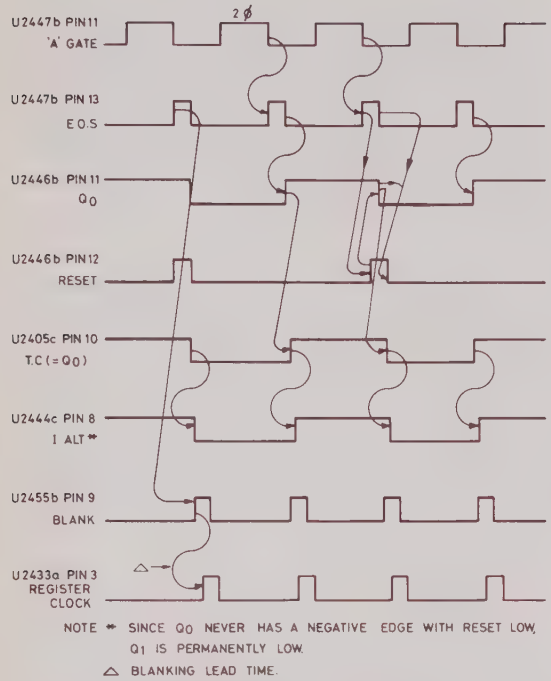

2ϕ
U2447b PIN 11 'A' GATE
U2447b PIN 13 E.O.S
U2446b PIN 11 Q0
U2446b PIN 12 RESET
U2405c PIN 10 T.C (=Q0)
U2444c PIN 8 I ALT *
U2455b PIN 9 BLANK
U2433a PIN 3 REGISTER CLOCK
NOTE * SINCE Q0 NEVER HAS A NEGATIVE EDGE WITH RESET LOW, Q1 IS PERMANENTLY LOW.
△ BLANKING LEAD TIME.

Fig.4.11.6 Timing Diagram Two Channels, Alternate Mode without Alpha Request.

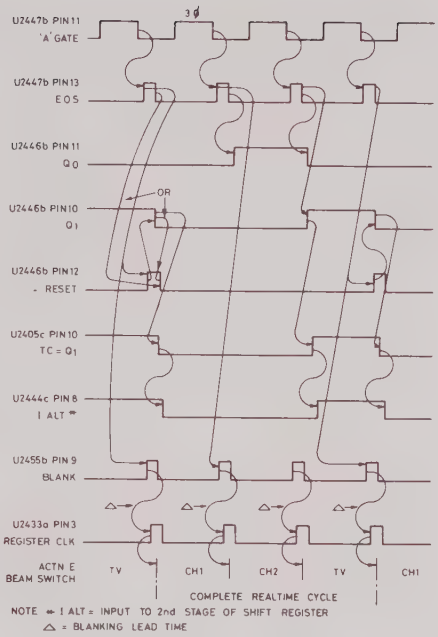

3ϕ
U2447b PIN 11 'A' GATE
U2447b PIN 13 E.O.S
U2446b PIN 11 Q0
U2446b PIN 10 Q1
OR
U2446b PIN 12 - RESET
U2405c PIN 10 TC = Q1
U2444c PIN 8 I ALT *
U2455b PIN 9 BLANK
U2433a PIN 3 REGISTER CLK
ACTN E BEAM SWITCH
TV CH1 CH2 TV CH1
COMPLETE REALTIME CYCLE
NOTE * I ALT = INPUT TO 2nd STAGE OF SHIFT REGISTER
△ = BLANKING LEAD TIME

Fig. 4.11.7 Timing Diagram Three Channels, Alternate Mode without Alpha Request

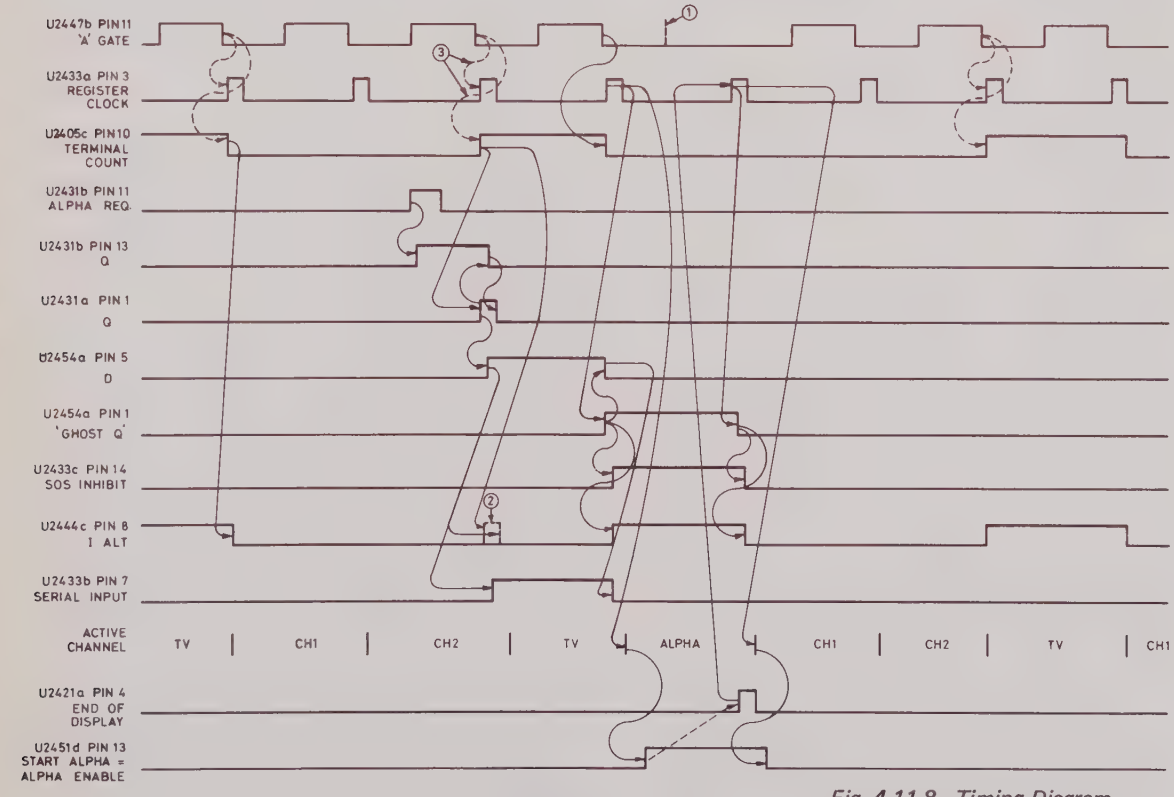

U2447b PIN 11 'A' GATE
U2433a PIN 3 REGISTER CLOCK
U2405c PIN 10 TERMINAL COUNT
U2431b PIN 11 ALPHA REQ.
U2431b PIN 13 Q
U2431a PIN 1 Q
U2454a PIN 5 D
U2454a PIN 1 'GHOST Q'
U2433c PIN 14 SOS INHIBIT
U2444c PIN 8 I ALT
U2433b PIN 7 SERIAL INPUT
ACTIVE CHANNEL
TV CH1 CH2 TV ALPHA CH1 CH2 TV CH1
U2421a PIN 4 END OF DISPLAY
U2451d PIN 13 START ALPHA = ALPHA ENABLE
① SWEEP WOULD NORMALLY START HERE BUT IS SUPPRESSED BY SOS INHIBIT.
② THIS PULSE MAY BE LOST DUE TO RACE CONDITIONS WITH NO EFFECT ON PERFORMANCE.
③ BLANK AND RESET AS IN FIG.

Fig. 4.11.8 Timing Diagram Three Channels, Alternate Mode with Alpha Request.

The Q output from U2431b then resets U2431d. Thus the TERMINAL COUNT produces a pulse at U2431a Q output, which passes through U2414d to set the S.R. latch formed by U2414d and b. See timing diagram Fig. 4.11.8. U2414 pin 9 is now held low, thus inhibiting the propagation of TERMINAL COUNT to the register. Instead, a logic '1' from U2414 pin 3 is passed to the alpha section of the register via U2416c, U2405a, D2403 and U2433b. Following the next END OF SWEEP pulse, the register is clocked into alpha mode. At the same time, the register clock pulse sets U2454a, thus clearing the S.R. latch and sending a logic '1' to the second stage of the register via U2451a. Thus U2454a delays the TERMINAL COUNT to the register by one clock pulse, and is set during the alpha phase, acting as a "ghost" of the first register stage. The "ghost Q" output is routed via U2456a to the "inhibit start of sweep" gate U2422a, preventing timebase sweep during the alpha phase. At the end of the alpha phase, the data display circuit sends an "END OF DISPLAY" pulse, which passes via U2426c, U2456b, U2426b and U2456c to produce a register clock pulse. Note that "END OF DISPLAY" does not clock U2446b, thus the counter effectively misses one register clock pulse, maintaining synchronism with the TERMINAL COUNT delayed by U2454a. Since the R.S. latch is cleared, the current clock pulse now clears U2454a, and the system resumes normal operation until the next alpha request. Fig. 4.11.8 shows the timing for 3 channels. Timings for 1 and 2 channels may be obtained by comparison with Figs. 4.11.5 and 4.11.6.

4.11.10.4 FORCED ALPHA MODE

In the previous section, it was assumed that high trigger rate allowed each ALPHA REQUEST to be followed by a TERMINAL COUNT. Since the actions following TERMINAL COUNT clear U2431b, the 'D' input of U2421a is always low when the next ALPHA REQUEST occurs.

At low trigger rates, an ALPHA REQUEST may occur before the previous one has been acknowledged by a TERMINAL COUNT. See Fig. 4.11.4.

Since the 'D' input of U2421a is now high, the Q goes high, defining the "PILE UP" condition. U2421b is directly set, and its Q output inhibits the action of the normal "request and acknowledge" system via U2414d. The PILE UP condition is also propagated via U2456a and U2426a to the "inhibit start of sweep" gate U2422a, preventing any further timebase sweeps.

The $\overline{\text{PILE UP}}$ $\overline{\text{Q}}$ output of U2421a passes via U2405b and U2434e to U2435d. At the end of the current timebase sweep, if any, this signal is gated through to the FORCE ALPHA line. U2444a converts the FORCE ALPHA signal to an ECL compatible level, which is transmitted to the Y preamp board and applied to U535 pin 12. This action overrides the shift register contents and forces the system into alpha mode. The FORCE ALPHA condition also sets U2454b, thus inhibiting U2426c, so that the END OF DISPLAY pulse does not produce a register clock, and the real-time sequence is not disturbed.

The END OF DISPLAY pulse clears down the PILE UP condition via the reset input of U2421a, allowing the timebase to resume on the next trigger pulse. The back edge of the END OF DISPLAY pulse clears U2454b via U2451b. Following the next TERMINAL COUNT pulse, the back edge of the pulse from U2431a clocks U2421b to clear, provided that there is no further PILE UP condition.

4.11.10.5 SOS INHIBIT

During the alpha phase in ALTERNATE mode, the timebase is inhibited, to prevent breakthrough effects and unwanted clock pulses from the timebase gate. Any input to U2422a activates the START OF SWEEP INHIBIT line, which is converted to an ECL differential signal by U2433c, and sent to the timebase board. The action of this control on the timebase circuit prevents any new sweep from starting, but does not reset the current sweep, if any. Inputs to the INHIBIT START OF SWEEP circuit may be:–

1. Software Force Alpha (see below)
2. Ghost Q (See NORMAL INSERTED ALPHA)
3. PILE UP (see FORCED ALPHA)

4.11.11 SOFTWARE FORCE ALPHA

The processor can select alpha mode, with absolute priority, by setting line O of U2411. This turns on U2444b, thus setting the FORCE ALPHA line. Timebase sweeps are inhibited by U2422a. This function is used mainly to display menus.

4.12 DATA DISPLAY SYSTEM

The Data Display System operates under control of the Display Management System, and is responsible for producing analogue X–Y signals and a digital blanking signal for alphanumerics and stored traces. A block diagram is shown in Fig. 4.12.1.

Data is displayed on an X–Y bases where each displayed dot has a unique X–Y co-ordinate generated from an address counter and ROM for alphanumerics, and an address counter for stored traces. These, in turn, are under the control of the Data Display Process Supervisor.

The function of this Supervisor is to sequentially allow display of alphanumerics pages 1 and 2, and stores 1 and 1, if so requested by the processor, and on command of the Display Management System, (see section 4.11).

In alternate mode, when the Display Management System requires data to be displayed it asserts $\overline{\text{Start}\propto}$. The Supervisor then steps through all dots of any display process selected (i.e. 1024 for a store and dots for all characters on the screen) using Memory Clock (1MHz for display modes), and returns the "End of Display" signal.

In chop mode $\overline{\text{Start}\propto}$ changes at chop rate and the Supervisor allows one dot to be displayed for each $\overline{\text{Start}\propto}$ pulse.

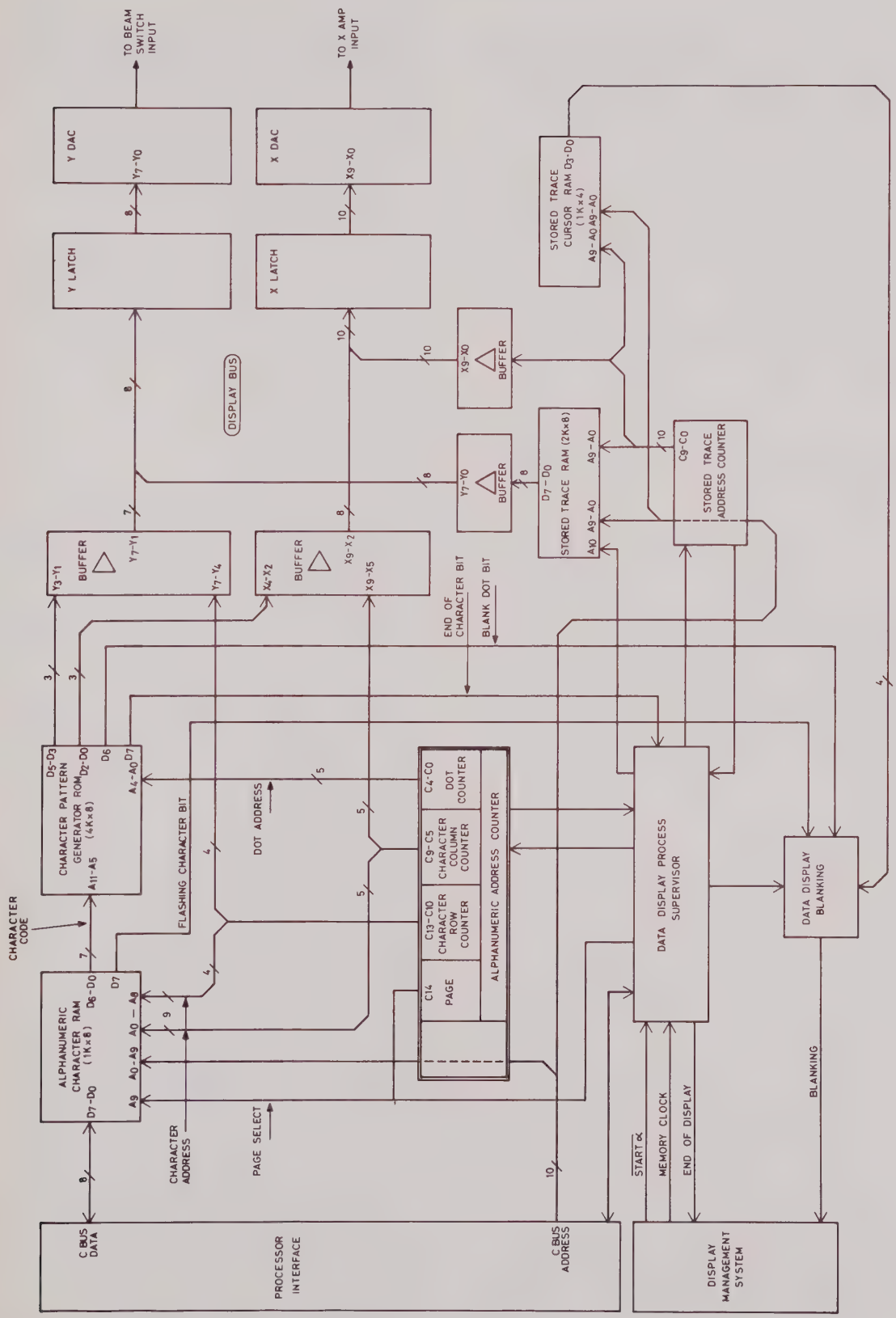


Fig. 4.12.1 Data Display System Block Diagram.

Alphanumerics are available as two independent pages each with 16 lines of 32 characters. Each character consists of a maximum of 31 dots within an 8 x 8 dot matrix. The Alphanumeric Character RAM, which is part of the processor memory map, contains 8 bit character codes which are formed from 7 bits ASCII and 1 bit for flashing character. During display time the Alphanumeric Address Counter steps through the RAM addresses. The RAM outputs (7 bit ASCII code) are presented to the Character Pattern Generator ROM along with the 5 least significant outputs from the counter. These 5 bits determine the ROM address of the dot currently being displayed within the current character.

Hence the counter steps through each character position and the dots of each character working line by line from the top left of the screen to the bottom right.

Each location in the ROM contains 3 bits for X, 3 bits for Y, 1 bit for blanking and 1 bit to mark the last dot of a character so that the Supervisor may move to the next character without having to waste time scanning blank "dots" of a character having fewer dots than the maximum possible.

When displaying alphanumerics the most significant 4 bits of the DAC define line position (1 of 16) and the remaining 3 define dot position (1 of 8). The least significant bit of the Y DAC is unused. Similarly the least significant 2 bits of the X DAC are unused. The most significant 5 bits define character column (1 of 32) and the remaining 3 define dot position (1 of 8).

Thus, each character is accommodated within a cell of 8 x 8 dots with a maximum of 31 dots per character (The hardware does not allow the expected 32 dots). Most characters however, exist within a 7 x 5 matrix, as shown for the letter 'A' in Fig. 4.12.2. The 3 columns and 1 row of blank "dots" serve to separate characters in normal text.

There are two independent 1K x 8 stored trace RAMS. For stored trace display, the 10 bit Stored Trace Address Counter steps through the 1K locations of each Stored Trace RAM. The 10 bit address and 8 bit data are applied directly to the DACs as X–Y dot co-ordinates. Each dot may be defined as blank, bright or flashing (for stored trace cursors) by the 1K x 4 Stored Trace Cursor RAM, addressed in parallel with the trace RAMs. Two bits are allocated to each store as shown below.

The blanking signals from both alphanumerics and stored trace display processes are combined with an inter-dot blanking signal for connection to the Display Management System where chop blanking is mixed in to produce a composite blanking signal.

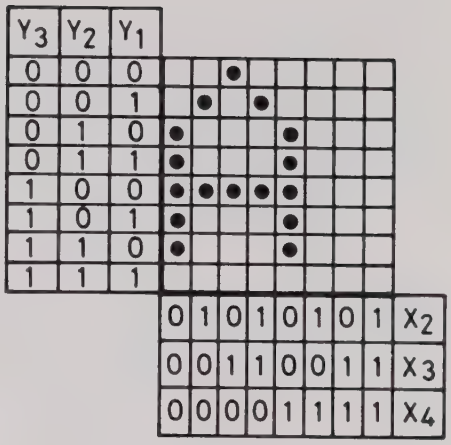


Fig. 12.2 Dot Pattern for Letter A.

4.12.1 DATA DISPLAY DIGITAL TO ANALOGUE CONVERTERS

The voltage regulator U2760 produces a 7V temperature-stable reference voltage for use by the various DACs on the Data Display PCB.

R2728 and R2729 produce a 3V reference at U2766 buffered by Q2701 to produce a constant 3V at R2725 wiper etc.

The Y DAC U2718 produces a differential output current (IOUT, $\overline{\text{IOUT}}$) which is proportional to its digital input value and its reference current. R2720 provides for gain calibration. The output currents are converted to voltages by R2725, 6, 7 and applied to emitter followers Q2702, 3 to produce a differential output voltage. R2725 provides offset adjustment.

The X DAC U2719 produces a single-ended output current proportional to its digital input. This current is converted to a voltage by R2745 for presentation to emitter follower Q2704. R2733, 4, 5 and R2789 produce a d.c. voltage having a nominal value equal to the half-scale voltage at Q2704. Emitter follower Q2705 passes this bias, producing a bipolar differential output for the following circuitry. R2735 provides for offset adjustment but X gain can only be adjusted at the X output amplifier.

4.12.2 DATA DISPLAY SUPERVISOR AND BLANKING

Initially, this description assumes the instrument to be in "alternate" mode. Thus Q4 of write only port U2706 will be low (CHOP/$\overline{\text{ALT}}$).

D3	D2	D1	DO
FLASH STORE 1	$\overline{\text{BLANK}}$ STORE 1	FLASH STORE 2	$\overline{\text{BLANK}}$ STORE 2

Fig. 4.12.3 Cursor RAM Bit Allocations

The incoming MEMORY CLOCK (1MHz in data display modes) is divided by 2 by U2753a, to produce the 0.5MHz DISPLAY CLOCK.

The Supervisor is formed around U2740 which is a 10 bit Johnson Counter. Only one output may be active (high) at a time and so there are 10 possible output states. The counter is reset and thus inactive until the $\overline{\text{START}\propto}$ line goes low.

4 bits of write only port U2706 are used by the processor to request data display with assignments as Table 4.12.4.

Write port U2706 output high	Data display requested
Qo	Alphanumerics page 1
Q1	Alphanumerics page 2
Q2	Store 1
Q3	Store 2

Table 4.12.4 Functional assignments for U2706 Qo–Q3

Assume first that U2706 Qo–Q3 are all low. $\overline{\text{START}\propto}$ goes low removing the reset on U2740. Since only U2740 Qo will be high at this time, U2742b and U2741a, b, c will be disabled, and thus U2743a output will be high. This allows the output from the "skip" oscillator formed around U2729a (running at about 100kHz), after re-timing with $\overline{\text{DISPLAY CLOCK}}$ in U2769b, to clock U2740 via U2746d and U2745b. Clocking continues and, as no display is requested when Q4, Q6, Q7, Q8 go high sequentially, the outputs of U2742b, U2741a, b, c remain low and eventually U2740 Q9 goes high producing END OF DISPLAY, which causes the Display Management System to send $\overline{\text{START}\propto}$ high again. (see section 4.11).

Assume now that the processor requires page 1 of alphanumerics to be displayed (i.e. has taken U2706 Qo high). This time when U2740 Q4 goes high, U2742b output goes high (assuming that $\propto$ RAM $\overline{\text{CS}}$ is high signifying no activity between the processor and the Alphanumeric Character RAM), U2743a output goes low disabling U2746d and preventing the skip oscillator from clocking U2740. DSP1 being low enables the alphanumeric display process to execute. (see section 4.12.3).

When alphanumeric display is complete, C14 (U2726 Q1), being terminal count, goes high; U2746a output goes high followed by U2745b output. This clocks U2740 into its next state and since display of alphanumerics page 2 is not requested $\overline{\text{DSP1}}$ goes high and the skip oscillator continues to clock U2740 until END OF DISPLAY is produced. A similar mechanism is provided to terminate stored trace display: TERMINAL COUNT P2 goes high and as DSP2 will be high. U2746c output will go high followed by U2745b output which clocks U2740.

It should thus be seen that the action of the Supervisor is to "hunt" for enabled display functions, with oscillator U2739a causing it to skip past those not required.

The outputs of skip counter U2740 are functionally assigned as shown in table 4.12.5.

U2740 Output	Function
Qo–Q2	Not Used
Q3	Alphanumeric RAM access prohibited
Q4	Display alphanumerics page 1
Q5	Not Used
Q6	Display alphanumerics page 2 Stored Trace RAM access prohibited
Q7	Display Store 1 Alphanumeric RAM access allowed
Q8	Display Store 2
Q9	End of Display Stored Trace RAM access allowed

Fig. 4.12.5 Functional Assignments of U2740 outputs

In "chop" mode, U2732c output is low, disabling U2770d allowing counter U2740 to run continuously

Inter-dot blanking is necessary to mask effects of DAC transitions. U2739b, R2710, C2710 and U2744c produce an I.D. BLANKING pulse on every positive edge of DISPLAY CLOCK as shown in the timing diagram of Fig. 4.12.6.

Every I.D. BLANKING pulse is passed to the BLANKING output via U2770b and U2828a.

4.12.3 ALPHANUMERIC DISPLAY

For this description the reader is referred to Fig. 4.12 (block diagram) and to the Data Display circuit diagram. U2722 is the Character Pattern Generator ROM; U2720 and U2721 the Alphanumeric Character RAM, and U2769a, U2723, 4, 5, 6 the Alphanumeric Address Counter.

Assuming that display of alphanumerics page 1 is just commencing, U2742b output goes high, U2744b output low and $\overline{\text{DSP1}}$ (Display Process 1) is asserted. This enables

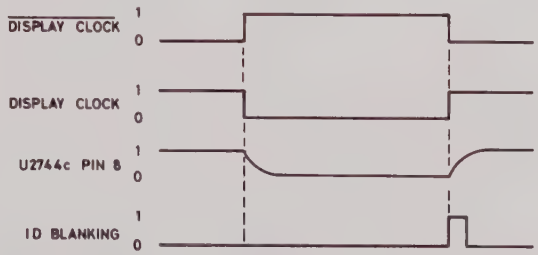


Fig. 4.12.6 Timing of Inter-Dot Blanking Circuit

buffers U2713, 4 and the ROM to drive the Display Bus to the DACs. The RAM is also enabled by $\overline{DSP1}$ forcing U2746b output low and thus U2720, 1 $\overline{CS}$ active. U2732b output (DSP1) being high, ensures that the RAM $\overline{WE}$ is inactive as it drives U2768a output high. Transmission gate U2733b is on, causing the page select line of the RAM (Aq of U2720, 1) to be driven by U2741b output. This output will be low at this time (since only one output of U2740 may be high), and thus page 1 is selected.

Before the display process started $\overline{DSP1}$ was high, U2729b pin 4, U2742d pin 10) setting all counter outputs C0–C14 low, and so the lowest RAM address is selected. This location contains the code of the character required in the top left hand corner of the CRT. The ASCII code for this character (appearing at the RAM output) forms part of the address of the ROM. The remaining 5 dot address bits come directly from U2769a and U2723. As these 5 bits are low the ROM produces the dot code/co-ordinate for the first dot of this character at its outputs. D0–D5 is the X–Y address of this dot within the character cell, and when combined with counter outputs C5–C13 the unique dot co-ordinate is formed for presentation to the output DAC latches.

When the next DISPLAY CLOCK (positive edge) occurs, (transmission gate U2733d is on), or the leading edge of $\overline{START}$ $\propto$ through U2733c in chop mode, the output latches U2715, 6, 7 are clocked and the X and Y DACs produce analogue voltages for the dot. Assuming that this dot is neither blank nor the last of the character, the same DISPLAY CLOCK edge clocks the dot counter U2769a, U2723 to address the next dot. Clocking continues until either U2723 reaches terminal count, when $\overline{TC}$ of U2723 goes low, or, more usually when D7 of the ROM goes high, indicating END OF CHARACTER. In the latter case U2727a D input becomes high and U2724 $\overline{CI}$ (Carry In) low i.e. forced carry. The next clock will advance the character count in U2724, 5, 6 by one and fire the monostable formed around U2727a to produce a brief (0.5μs) reset pulse for application to the dot counter U2769a, U2723 thus moving on to the next character.

The monostable operates as follows. When D is high and a clock occurs, Q goes high allowing R to rise towards +5V with a time constant determined by R2707 and C2708. When the voltage on R is sufficiently high, $\overline{Q}$ will start to rise and the positive feedback via C2707 assists, speeding up the reset pulse, which causes Q to change low.

When all characters have been displayed, C14 goes high to inform the supervisor of this fact.

Blanking circuitry is included to allow the blank character and the flashing character.

When no display process is enabled, U2727b is disabled (set) and $\propto$ BLANKING is high.

When a blank character is encountered, the BLANK DOT bit (D6) of the ROM will be high, U2729c output high and as DSP1 turns on transmission gate U2709a, the D input of U2727b will be high so that the next DISPLAY CLOCK takes U2727b Q output high asserting $\propto$ BLANKING.

When a flashing character is encountered the most significant bit of the character code, U2720 pin 14 will be high, enabling U2730d to pass the 2Hz clock to the blanking circuitry described above.

Since the display process is considerably faster than flash rate U2727b latches the current state of the flash (2Hz) signal.

4.12.4 STORED TRACE DISPLAY

In the following description DSP2A and DSP2B correspond to display of Store 1 and Store 2 respectively. Note that component references with prefixes of 2600 refer to Data Acquisition and Store circuit diagram and 2700 refer to Data Display board/circuit diagram.

The Data Acquisition and Store hardware is organised so that display of stored data represents one of its several modes of operation. These modes are detailed in Table of Fig. 4.13.5 which should be referred to for the following description to determine the static state of many acquisition/display signals. This description assumes that the processor has requested display of Store 1.

Referring to the Data Acquisition and Store circuit diagram, U2620, 1, 2, 3 form the Stored Trace RAM and U2624 the Stored Trace Cursor RAM. U2620, 1 contain Store 1 data, U2622, 3 contain Store 2 data whilst U2624 contains cursor/blanking information for both stores (see Table 4.12.3.) U2625, 6, 7 form the Stored Trace Address Counter which is under the control of the Data Display Process Supervisor.

For display of Store 1 the processor sets Q2 of U2706 (Data Display circuit diagram). When this display process is enabled the Supervisor takes U2741a output high asserting DSP2A and DSP2 via U2744d. U2745a output goes low enabling buffers U2710, 1, 2 to pass X and Y data from the Data Acquisition system via cable link PLCG/PLBV, to the X and Y output DACs.

Since DSP2A is high, U2602a output is high and holds the RAM $\overline{WE}$ inputs inactive (high). Also, $\overline{DSP2A}$ being low ensures that $\overline{CS}$#1 is low enabling U2620, 1 to drive 8 bit data to the Y DAC.

AS $\overline{DSP2}$ is low, U2625 is enabled for counting (μB3 is high turning on transmission gate U2639c and $\overline{DSP2}$ takes U2625 $\overline{CI}$ low via U2632b) and since DISPLAY CLOCK ENABLE is high (see Table 4.13), U2625, 6, 7 are clocked by DISPLAY CLOCK. As the count proceeds, 10 bit X information is obtained from the counter outputs for application to the X DAC. U2627 Q2 goes high when the contents of all Store 1 locations have been displayed as dots on the CRT, producing TERMINAL COUNT P2. This takes U2643c output high, U2644a output high resetting the counters. TERMINAL COUNT P2 also clocks U2740 out of the DSP2A state, informing the Supervisor

that Store 1 display is complete (U2746c, U2745b).

As previously stated, the cursor store contains two bits per stored trace dot to specify whether the dot is blank, steady or flashing.

If Store 1 display is in progress then $\overline{DSP2A}$ is low and U2628a output is high. Since $\overline{DSP2B}$ is high, CURSOR BLANKING is determined by U2628c input, pins 12 and 13. If the current dot is blank, $\overline{BLANK}$ STORE 1 is low forcing U2628c output high and CURSOR BLANKING high. If BLANK STORE 1 is high and FLASH STORE 1 low, U2629a output is high allowing CURSOR BLANKING to be low.

If $\overline{BLANK}$ STORE 1 is high and FLASH STORE 1 high, U2629a output becomes $\overline{2Hz}$ which allows the CURSOR BLANKING output to switch at 2Hz.

CURSOR BLANKING is taken to the Data Display system where it passes through the enabled transmission gate U2709b to reach the D input of U2727b when the next DISPLAY CLOCK updates ∝ BLANKING accordingly.

4.12.5 PROCESSOR INTERFACE TO DATA DISPLAY SYSTEM

When the processor requires access to the Alphanumeric Character RAM the ten least significant CBUS address lines are routed through the counters U2724, 5, 6 which are in parallel load mode during the transaction. Data is routed through bi-directional buffers U2701, 2 between the CBUS data lines and the RAM U2720, 1.

The particular counters used have a significant propogation delay time in parallel load mode and in order to prevent data being written to an incorrect address, the first half of a CBUS cycle is used to parallel load the address through the counters, and the second half to perform the actual read/write transaction with RAMs. Fig. 4.15.3 showing the CBUS (extended) cycle timing should be referred to here.

Before description of the CBUS/RAM transaction it must be noted that the processor may not access the RAM during display time. If it were to do so, a random (as far as the display process is concerned) address would be left in address counters U2724, 5, 6 and multiple access activity would result in a badly flickering display. Set- Reset bistable U2730a/U2743c provides alphanumeric display status for the processor to read via D7 of read only port U2714. Alphanumeric RAM access is allowed only when U2743c output is low. If neither page display is requested by the processor Q0 and Q1 of write only port U2706 will be low, U2730c output high forcing U2743c output low allowing permanent access. If at least one page is to be displayed then outputs from the counter U2740 determine status. U2740 Q3 goes high one skip oscillator period (about 100μs) before alphanumeric display commences. This sends U2730a output low and U2743c output high giving the processor enough time to finish any current transaction with the RAM. (Allowing a delay of some 30μs between the processor reading status and the RAM transaction). When display is complete U2740 Q7 goes high sending U2743c output low again.

At the start of a CBUS cycle involving the alphanumeric RAM, ∝ RAM $\overline{CS}$ goes low and U2732d output goes high to put the counters into parallel load mode. U2742d output goes low to prevent reset from overriding parallel load. Also the RAM U2720, 1 $\overline{CS}$ is active as U2746b output goes low. When CBUS $\overline{E}$ goes low U2768a is enabled so that if the cycle is a write cycle the $\overline{WE}$ of the RAM may go low. $\overline{QCS}$ will also be low allowing either U2728 c or d outputs to be low dependent upon R/$\overline{W}$ (If R/$\overline{W}$ is low, U2728c output will be low enabling data transfer from CBUS to the RAM).

The mechanism for processor access to the Stored Trace RAM is similar to that for alphanumerics. However, reference should be made to Table 4.13.5 to determine the static state of many signals.

Stored trace display status is generated by set-reset bistable U2703a, b. If the processor requires neither store display then Q2 and Q3 of write only port U2706 will be low giving U2703c output high and U2703a output low which allows the processor access.

When a store display is enabled, U2740 Q6 goes high (one state before that for display of Store 1) U2703a output goes high to prevent processor access, and when U2740 Q9 goes high (display of stores complete) U2703a output goes low again to allow access.

If the processor attempts to access Store 1, Store 2 or the cursor RAM, U2601c output goes low and U2635a output high to parallel load the address counters U2625, 6, 7 with the processor address. U2643 output goes low to disable the counter reset.

If the processor is attempting to access Store 1, $\overline{CS\#1}$ goes low to chip-select the Store 1 RAMs U2620, 1. μB3 is high and so the processor R/$\overline{W}$ line drives the RAMs via U2602a and tri-state buffer U2668b. Tri-state buffers U2603, 4, 5 handle CBUS data to or from the store RAMs. $\overline{P2\ ADD}$ will go low during the transaction allowing U2603, 4 $\overline{1G}$ to go low for a read cycle and U2603, 4 $\overline{2G}$ low for a write cycle.

When the processor needs to access the Cursor Store, CSR BLK $\overline{ADD}$ goes low and U2605 $\overline{1G}$ will go low for a write cycle, and U2605 $\overline{2G}$ low for a read cycle.

Although the two access status bits normally control processor access it is still possible for the processor to disregard this status and execute a memory transaction anyway. If alphanumeric display is in progress when access is demanded, DSP1 being high would disable the RAM $\overline{WE}$ via U2768a. However ∝ RAM $\overline{CS}$ will take U2742b and U2741b outputs low, temporarily preventing display. For stored trace RAM access, U2742a output ($\overline{STORE\ ADDRESS}$) goes low, taking U2741a, c outputs low to ensure DSP2 low and no store display activity for the duration of the transaction.

4.13 ACQUISITION AND STORE SYSTEM

4.13.1 BLOCK DIAGRAM AND GENERAL OVERVIEW

Fig. 4.13.1 shows the block diagram for the complete Acquisition System.

The sampling head, required to hold analogue data stable for A/D conversion, is normally in 'follow' mode but holds the instantaneous 'Y' signal voltage upon receipt of the hold command from the Acquisition Controller. START CONVERSION instructs the ADC to convert this static voltage into an 8 bit value for the processor to read, or for storing in the Trace Stores, depending upon the acquisition mode chosen.

In single shot modes (e.g. current cursor or real-time trace) the controller allows the processor to read the ADC value directly, but in trace capture modes (e.g. real-time capture) the controller writes the ADC value directly into the trace store, incrementing the Acquisition Counter after every ADC conversion and so builds up a complete stored trace.

Acquisition is subject to certain Global Acquisition Qualifiers; for instance, those that define 'Y' channel beam-switch state. Acquisition is also at the request of the processor, which configures the controller for the particular acquisition mode.

Under processor control, the contents of either store may drive plot outputs for pen recorder use.

In single shot modes, the processor may optionally request acquisition from the Data Word Input. This 8 bit value may be read directly by the processor.

4.13.2 SAMPLING AMPLIFIER, BRIDGE & BUFFER (See Y Output & Sampling Circuit)

The instrument Y channel (i.e. after the beam-switch stage) drives the Sampling Amplifier input via emitter followers Q3005,6. This amplifier receives a differential wide-band input at Q3153,4 bases but in order to achieve high d.c. stability the low frequency route to Q3153 base is via the L.F. amplifier formed around U3170a whose gain may be adjusted for calibration purposes by R3174. This is shown in schematic form in Fig. 4.13.2.

The output from the first differential amplifier, Q3153,4 is taken to a second amplifier formed by Q3151,2. The single-ended output at Q3152 collector feeds emitter follower Q3150.

Overall negative feedback is from Q3150 emitter via R3155 to Q3153 base but R3151 provides L.F. negative feedback for U3170a and associated components.

The Sampling Bridge (see later for details), consisting of Schottky diodes D3120,1,2,3 normally conducts, and so the sampling capacitors C3183,4 form the (capacitive) load of the Sampling Amplifier. When the bridge opens to hold the sampling capacitor voltage, this capacitive load is suddenly removed and hence the Sampling Amplifier is considerably compensated to prevent instability.

The Sampling Capacitor Buffer, formed by Q3190,91,93,94 has a much lower band-width since it has a considerable time to settle to the signal held on the sampling capacitor for the ADC conversion to take place. Q3190 – a totem-pole source follower biased by Q3191 (on the same sub-

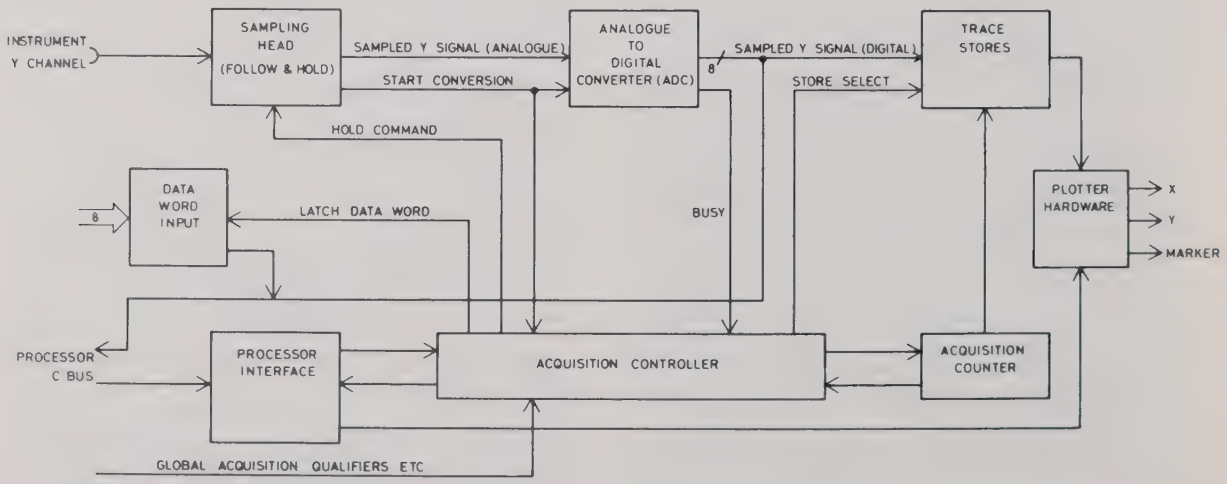


Fig. 4.13.1 Acquisition System Block Diagram

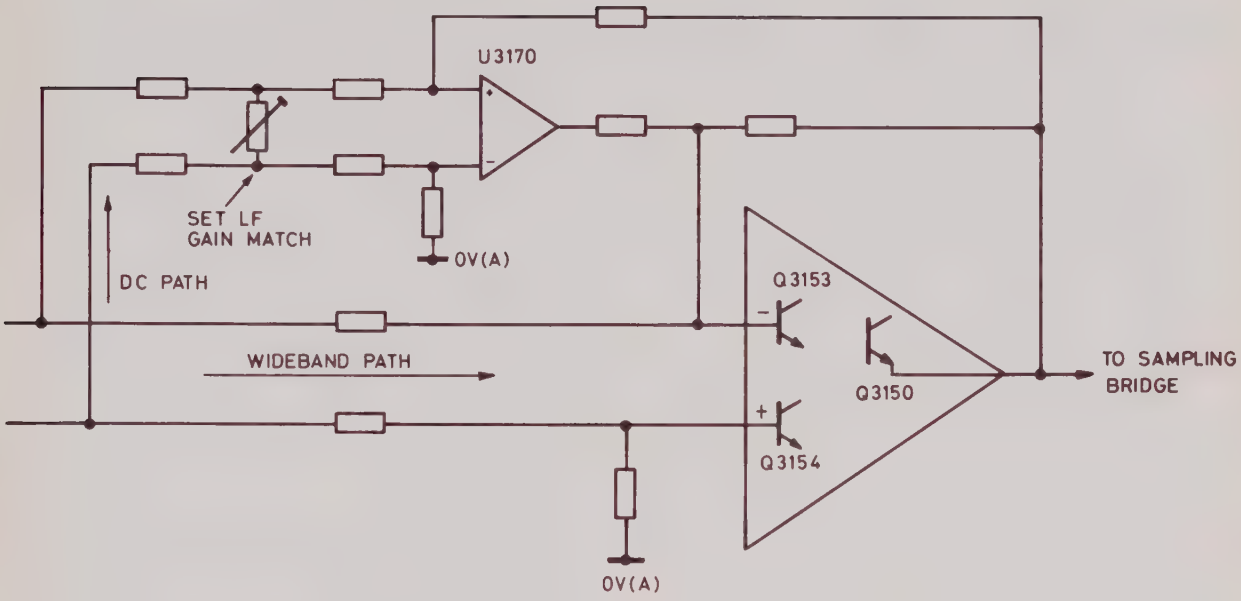


Fig. 4.13.2 Sampling Amplifier Schematic

strate as Q3190) and diode-connected Q3193 – has an adjustable gate current bleed in the form of R3184,5,6. (This is used to set capacitor voltage droop during ADC conversion time). Emitter follower Q3194 passes the buffer output to the ADC.

The Sampling Bridge (D3120,1,2,3) normally conducts so that the sampling capacitor voltage follows the output of the Sampling Amplifier. A schematic of the sampling bridge and control is shown in Fig. 4.13.3. When in 'follow' mode, "switches" Q3115,6 are open and the current I+, accurately matching I-, is allowed to flow through the bridge causing all four diodes to conduct. There is thus a very low impedance path from Vin to Vout. When in 'hold' mode switches Q3115,6 close and divert current I+ and I- from the bridge. Thus all four diodes are cut off leaving the sampling capacitor to hold its charge.

In the 'follow' state HOLD 1 and HOLD 2 are low: Q3110 is on, Q3111 off and thus Q3115 off; Q3112 is on, Q3113 off and thus Q3116 off. Consequently the current in Q3120 is identical to that of Q3123 holding all four diodes conducting.

The divider chain R3140,1,4 holds U3104b non-inverting input at 4V. The feedback action of this Op-amp holds Q3120 emitter at the same voltage with Q3120 boosting the Op-amp output current to that defined by R3145 (30mA). The current through the bridge from this source is sunk by a similar circuit consisting of U3104a and Q3123. These two currents are accurately complementary since R3140 matches R3144 and R3145 matches R3148.

When the sample head is in the "hold" state HOLD 1 and HOLD 2 are high: Q3110 is off, Q3111 on and thus Q3115 on; Q3112 is off, Q3113 on and thus Q3116 on. In this state Q3116 sinks the current from Q3120 and Q3115 that of Q3123. The potential divider R3142,3 holds U3104c non-inverting input at +3V and the feedback action of U3104c holds the emitter of current booster Q3121 at +3V. A similar circuit using U3104d and Q3122 holds Q3122 emitter at -3V.

The anodes of D3120,1 are thus driven to -3V and those of D3122,3 to +3V. Hence the Sampling Bridge is cut off leaving the sampling capacitor charged to the voltage on it at the instant of changeover.

Schottky diodes D3115,6 prevent Q3115,6 from saturating so that the bridge may be turned back on in a fast, controlled way.

T3101,2 are provided to prevent one half of the bridge drive electronics changing state significantly before the other, which would disturb the sampling capacitor voltage and drastically alter the load at the Sampling Amplifier with consequent instability.

As Q3111 turns on, its collector voltage falls. This change is coupled via T3101 to assist Q3116 turning on.

As Q3115 collector voltage rises, coupling via T3102 assists in taking D3120,1 anodes negative. When the bridge turns back on the skew between each half of the bridge drive electronics is additionally controlled by the SET SKEW 2 control R3207.

U3102a,c are configured as Schmitt triggers and when HEAD RESET is asserted the actual time skew between

U3103a and U3103b changing state may be set by R3207, which in conjunction with C3110,1 provides the necessary variable delays.

4.13.3 ANALOGUE TO DIGITAL CONVERTER (ADC) (See Data Acquisition & Store Circuit)

The output from the Sampling Capacitor Buffer (ref section 4.13.2) is fed via co-axial cable to SKSS, terminated by R2061 and applied as the analogue signal input to the ADC U2660. DC input bias is obtained by R2669, R2638 & R2663 to give a full scale signal swing of 0.5V centred at -0.25V. The actual bias point is therefore set by ADC offset preset R2669.

The voltage at the ADC reference input VREF is nominally -0.5V and is generated by R2659, R2661, & R2660 which is used to set the precise reference voltage.

The ADC which is of the successive approximation type, has two digital inputs; Clock and Start Convert, and one additional logic output; Busy. Full timing information is given in Fig. 4.13.4.

4.13.4 ACQUISITION LOGIC

4.13.4.1 GENERAL

The Acquisition System hardware has several operating modes which are detailed in the table of Fig. 4.13.5. Reference should be made to this table to determine the static state of many lines for the particular mode under discussion.

Firstly, however, that part of the Acquisition logic common to all modes will be described. This is the logic for controlling the Sample Head, the ADC and for generating RAM write enable pulses and Acquisition counter clocks. Frequent reference will be made to the Data Acquisition and Store and Y Output and Sampling circuit diagrams.

The following description assumes that HOLD ENABLE has just gone high and a SAMPLE CLOCK (used to clock the Sample Head into 'HOLD' state) has occurred, as the exact condition required for this to happen depends upon capture mode. The timing diagram Fig. 4.13.6 should also be referred to for this discussion.

Following HOLD ENABLE high and a SAMPLE CLOCK, U3103a Q and U3103b Q will be high asserting HOLD 1 and HOLD 2. These signals control each half of the sampling bridge; when HOLD 1 and HOLD 2 are high the sampling head is in the 'hold' state. The output from U3103a forms the START CONVERSION signal for the ADC.

The 20MHz ADC clock is only started when acquisition is required and the oscillator is formed by Schmitt NAND gate U2663c, emitter follower Q2610, R2632, C2602, R2634, R2635. With U2664a output low, U2663c output is high and the clock disabled. When START CONVERSION goes high, U2664c output goes high and Q2610 base goes low allowing U2663c pin 9 to fall, with a time constant determined by R2632 and

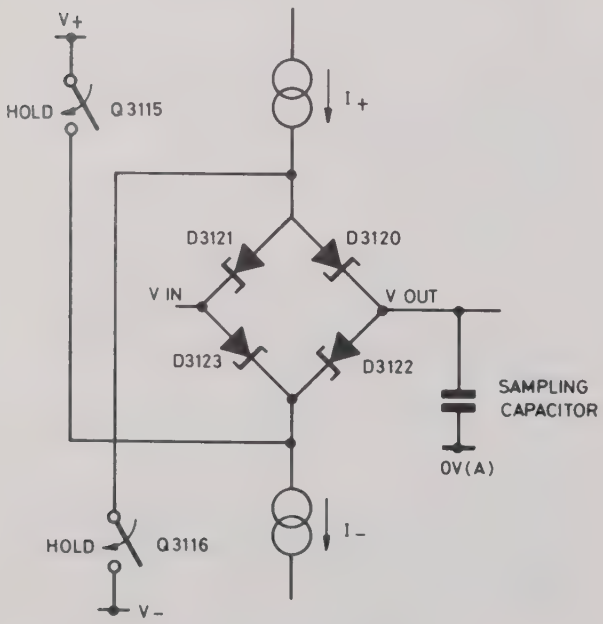


Fig. 4.13.3 Sampling Bridge Schematic

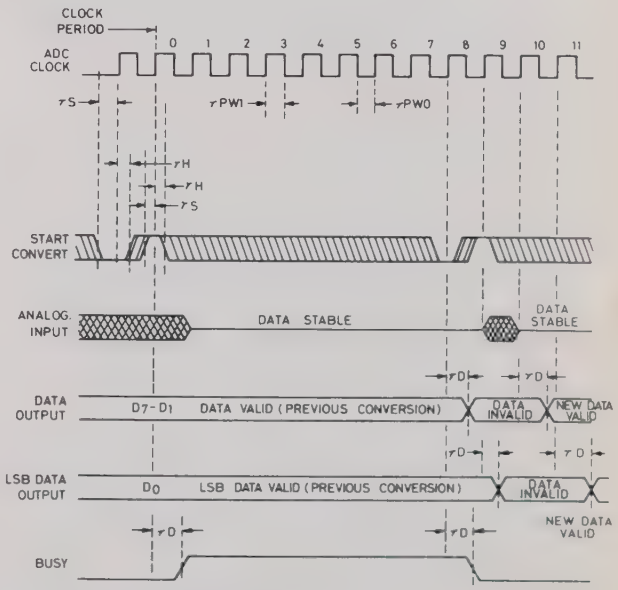


Fig. 4.13.4 ADC Timing Diagram

PARAMETER	MIN	NOM	MAX
τD		35ns	50ns
τS	7ns		
τH	7ns		
τPW0	20ns		
τPW1	20ns		

Signal Name	1 Display/ Processor Access S.S. ADC	2 Single Shot Word	3 Single Channel Post-Trig.	4 Dual Channel Post-Trig.	5 Single Channel Pre-Trig.	6 Dual Channel Pre-Trig.	7 Plot Mode
μB0	1	1	1	1	0	0	1
μB1	1	1	1	⊓	1	1	1
μB2	1	1	1	1	1	1	1
μB3	1	0	0	0	0	0	1
μB4	1	1	1	1	1	1	1
μB5	1	1	0	0	0	0	1
μB6	0	1	0	0	0	0	1
μB7	0	0	1	0	1	0	0
μB8	0	0	0	1	0	1	0
μB9	0	0	0	0	0	0	0
μB10	1	0	0	0	0	0	1
μB11	1	1	1	1	0	0	1
μB12	1	1	CD/$\overline{RT}$	CD/$\overline{RT}$	CD/$\overline{RT}$	CD/$\overline{RT}$	1
μB13	0	0	0	0	*	*	0
μB14	0	0	0	0	1	1	0
μB15	0	0	High to store CH1 data in Store 1				0
μB16	0	0	High to store CH2 data in Store 2				0
μB17	0	0	High to store CH1 data in Store 2				0
μB18	0	0	High to store CH2 data in Store 1				0
μB19	1	1	CD/$\overline{RT}$	CD/$\overline{RT}$	0	0	X
$\overline{PRE\text{-}TRIG.}$	1	1	1	1	0	0	1
START P.T. ACQUISITION	X	X	X	X	⌐	⌐	X
CLOCK DISPLAY ENABLE	1	0	0	0	0	0	1
ENABLE DUAL R-TIME ACQ.	0	0	0	$\overline{CD}$/RT	0	$\overline{CD}$/RT	0
CHOP STROBE SELECT	1	1	CD/$\overline{RT}$	CD/$\overline{RT}$	CD/$\overline{RT}$	CD/$\overline{RT}$	1

KEY TO DATA ACQUISITION AND DISPLAY TRUTH TABLE

CD = Countdown i.e. repetitive capture mode
RT = Real-time capture mode
* = Held low by processor until half store of pre-trigger information guaranteed.
X = Irrelevant
⊓ = Negative-going pulse
⌐ = Positive edge active

Fig. 4.13.5 Data Acquisition and Display Truth Table

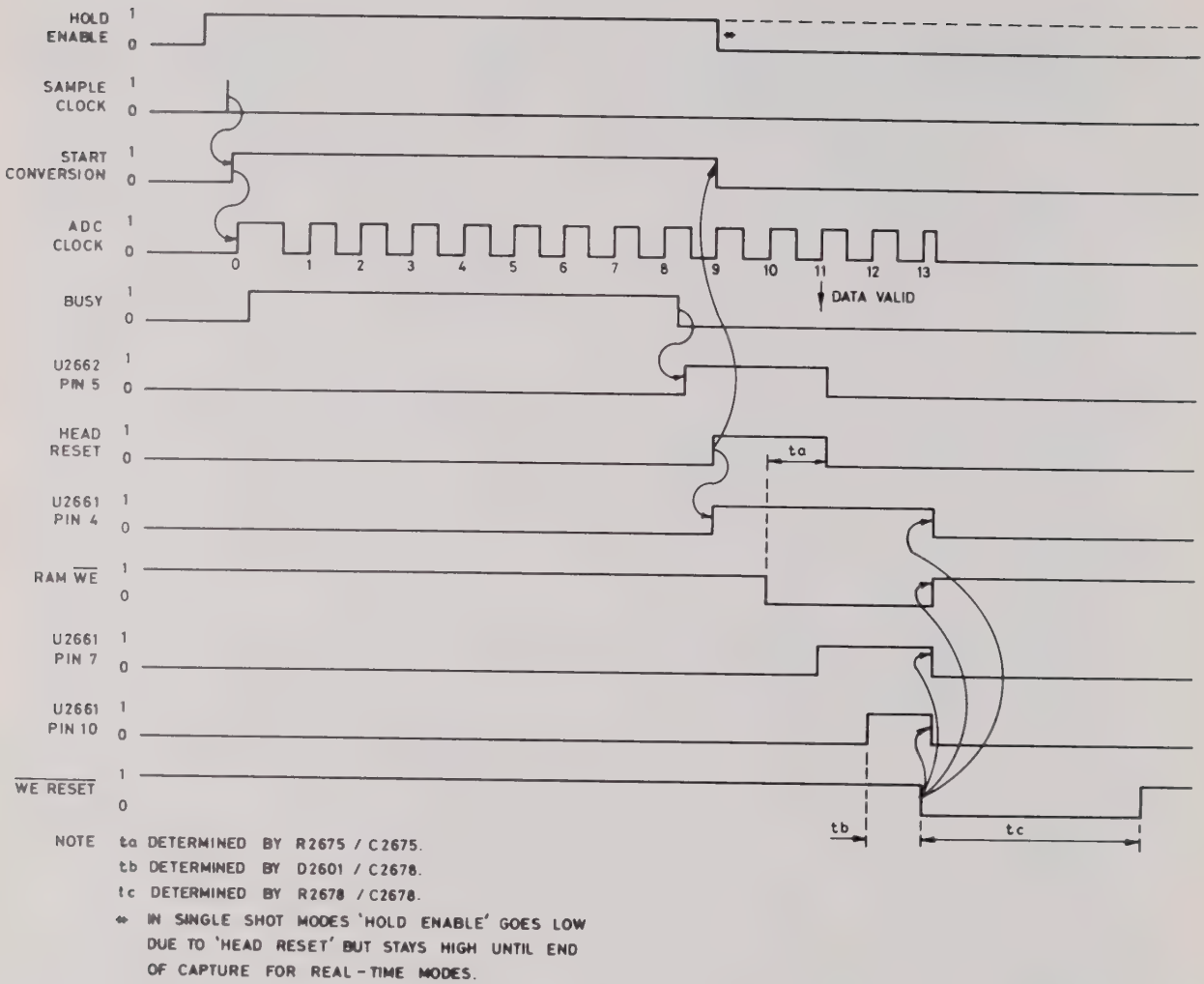

HOLD ENABLE
SAMPLE CLOCK
START CONVERSION
ADC CLOCK
BUSY
U2662 PIN 5
HEAD RESET
U2661 PIN 4
RAM WE
U2661 PIN 7
U2661 PIN 10
WE RESET
0 1 2 3 4 5 6 7 8 9 10 11 12 13
DATA VALID
ta
tb
tc
NOTE ta DETERMINED BY R2675 / C2675.
tb DETERMINED BY D2601 / C2678.
tc DETERMINED BY R2678 / C2678.
⇔ IN SINGLE SHOT MODES 'HOLD ENABLE' GOES LOW DUE TO 'HEAD RESET' BUT STAYS HIGH UNTIL END OF CAPTURE FOR REAL-TIME MODES.

Fig. 4.13.6 Basic Acquisition Timing

C2602, until the negative-going threshold (VT-) of U2663 pin 9 is reached. U2663c output then goes low and allows U2663c pin 9 to rise towards the positive-going threshold (VT+) with a time constant determined by R2632, R2634, C2602 and R2635 the latter being used to set up the 20MHz oscillator. The timing diagram shows that the first half cycle of the ADC CLOCK takes longer than any other. This is because the normal voltage excursion on C2602 is (VT+) – (VT-) but at start-up the voltage on C2602 is considerably greater.

Having received START CONVERSION and ADC CLOCK the ADC soon produces the BUSY signal which takes U2666c output low. When BUSY goes low the ADC still requires the clock to continue for several cycles (see section 4.13.3). When the trailing edge of BUSY clocks U2662a, U2662a Q keeps the 20MHz clock running via U2664b and U2664a. This anticipates START CONVERSION going low at the start of the next clock cycle.

U2629d ensures that whenever BUSY occurs U2662a Q will go high to keep the clock running. Assume, temporarily that HOLD ENABLE is low but BUSY goes high, U2629d output will go high and when the trailing edge of BUSY clocks U2662a, U2629d output will still be high utilising the difference in propagation delay time between U2629 which is a CMOS device and U2662 which is TTL.

Returning to the timing diagram, ADC CLOCK 9 takes HEAD RESET high and this resets U3103a,b via line-receiver U3101 and skew control circuitry U3102a,c (see section 4.13.2).

To cover the possibility that START CONVERSION produces no HEAD RESET, the time-out circuit around

U3105b,d is employed. U3105d is a Schmitt trigger so that after START CONVERSION has gone high C3108 charges until U3105d pin 15 goes high (about 7μs) and resets U3103a and U3103b via U3105b.

Now that the ADC conversion is complete, U2661 can produce RAM write enable and counter clock signals for modes requiring these.

U2662b Q (HEAD RESET) was left high after clock 9, this takes U2661a D input high via U2664d so that clock 10 takes U2661a Q low asserting RAM $\overline{WE}$. Since U2661a Q is high U2661a D input will remain high (independent of HEAD RESET) so that, after a delay tA, U2662 is reset and HEAD RESET goes low again. U2662a Q being low cannot now keep the ADC clock running (required only to clock U2661), but this function is taken over by U2661a Q which holds U2664b output high. U2661a Q can now only go low when reset, since it supplies its own D input.

Clocks 11 and 12 take U2661b Q and U2661c Q high respectively, and are used purely for time delay to produce a RAM $\overline{WE}$ pulse sufficiently long for the MOS RAMs.

When U2661c Q goes high, however, U2663a output goes low after time tB, and $\overline{WE}$ RESET goes low resetting U2661a, b,c, and taking RAM $\overline{WE}$ high again. (The ADC CLOCK also stops at this point). When U2661c Q goes low, D2601 is cut off and C2678 discharges via R2678. Hence a time tC elapses before $\overline{WE}$ RESET goes high again. This positive going edge is used to clock the Acquisition counter (U2625,6,7). The delay tC assures the minimum low time requirement of these devices.

For acquisition modes requiring the ADC output to be stored in RAM (Real-time), the Store 1 (U2620,1) and Store 2 (U2622,3) $\overline{CS}$ inputs are enabled according to:

a) which channel acquisition was made on, and

b) the capture destination selected by the user.

The beam switch state is determined by a combination of the inputs CH1 + CH2 and CHANNEL Φ. When CH1 + CH2 is high the beam switch circuitry is not set for CH1 or for CH2 and so CHANNEL Φ is meaningless. When CH1 + CH2 is low, CHANNEL Φ low indicates that the beam switch is in the CH1 state, and when high, the CH2 state. Acquisition start is qualified by CH1 + CH2 and so CHANNEL Φ is valid when sampled during the acquisition.

When the first START CONVERSION occurs, U2640b Q will thus become high for CH2, low for CH1, and when U2662a pin 5 goes high during cycle 8 (see Fig. 4.13.6), U2640a Q and $\overline{Q}$ are updated.

Transmission gates U2672a,b,c,d route Q and $\overline{Q}$ to the Store 1 and Store 2 $\overline{CS}$ inputs as set by μB16, μB17, μB18 (see Fig. 4.13.5). For example if μB17 only is high, U2640a Q ($\overline{\Phi 1}$) will drive the Store 2 $\overline{CS}$ low (U2662,3) via U2643a.

In single channel capture modes the processor temporarily forces the beam switch state for the single channel required (no alphanumerics i.e. Alternate mode) and so the above sequence merely clocks the static state of CHANNEL Φ through to the RAM $\overline{CS}$ inputs and this situation prevails until capture is complete.

Dual channel operation is described in section 4.14.4.3.

4.13.4.2 CURRENT CURSOR VOLTAGE AND REPETITIVE ACQUISITION (See Fig. 4.13.7)

For Current Cursor Acquisition the processor configures the acquisition hardware to convert the voltage at the current cursor instant into an 8 bit digital word for subsequent numerical converstion and display. In this mode the current cursor clocks the sample head into the 'hold' state. (Reference should be made to Fig. 4.13.7 and to column 1 of Fig. 4.13.5). Most bits in this table appear on write only ports U2606,7,8 with the remainder on write only port U2706 (Data Display PCB).

To initiate acquisition the processor takes ACQUISITION REQUEST high, which clocks U2671a Q high. This request is acknowledged when U2671b is clocked and the condition required for this to happen is "'A' ramp not running".

In this mode, Q0 of U2606, $\overline{PRE\text{-}TRIG}$ is high so that tri-state buffer U2668d is disabled and U2668c enabled. Hence U2601b output is effectively connected to U2671b clock input. This equivalent circuit is shown in Fig. 4.13.8.

If acquisition is requested when 'A' ramp is not running, (for example during the timebase 'hold-off' period) then $\overline{AQ}$ will be high. Thus U2671a Q going high clocks U2671b Q (HOLD ENABLE) high.

If acquisition is requested whilst 'A' ramp is running, then $\overline{AQ}$ will be low and U2671b clock input held low. When U2671a Q goes high, U2671b D input is set up but cannot be clocked until $\overline{AQ}$ goes high, i.e. end of 'A' sweep. Once U2671b Q goes high U2671a is reset in readiness for a future acquisition and HOLD ENABLE is asserted. HOLD ENABLE causes SAMPLE CLOCK as described at the end of this section. This then initiates the 'hold and convert' sequence described in section 4.13.4.1.

When head reset goes high, μB10 is high and so, via U2662d and transmission gate U2639d it passes to U2671b reset input. This takes HOLD ENABLE low again in readiness for the next acquisition.

To inform the processor that acquisition is complete, when $\overline{HOLD\ ENABLE}$ goes high, U2609a is clocked and its Q output goes high to generate the ACQUISITION INTERRUPT. This bistable is cleared down when the processor accesses any store or the ADC or Data Input Word latch, via U2642b and U2635c.

To read the ADC output the processor reads address $C81 which takes READ ONLY ADDRESS $C81 low to enable tri-state buffer U2667 via U2665a and U2612a. At the same time U2642b output goes low and as R/W is low (read cycle) U2633c output goes low enabling buffers U2603,4 to pass the ADC data from U2667 through to CBUS.

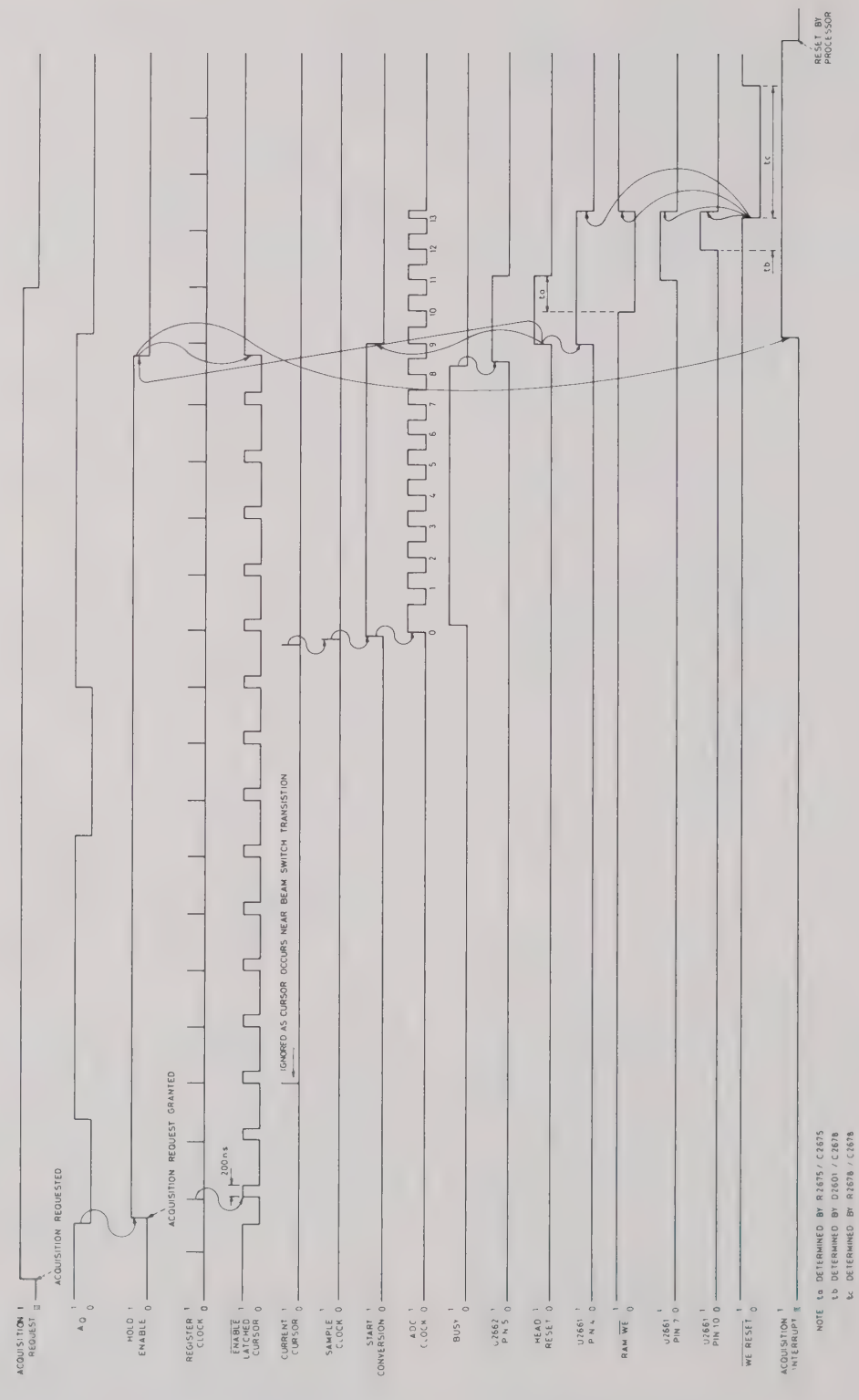


Fig. 4.13.7 Current Cursor Voltage and Repetitive Acquisition Timing

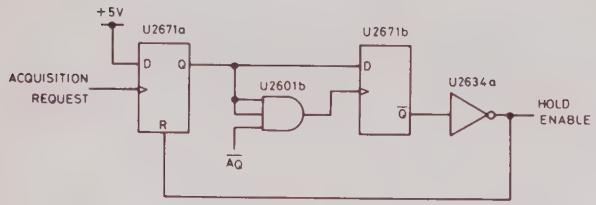


Fig. 4.13.8 Acquisition Request/Grant Logic

In Repetitive capture mode, the above sequence is executed 1024 times, with the processor reading the ADC output value, storing the result in the required trace store and moving the cursor to the next required position. In this way a complete trace is built up at the full instrument bandwidth at the expense of at least 1024 sweeps. (In practice the capture rate is limited by processor execution time and not sweep rate).

HOLD ENABLE is used to enable a latch (U1610b, Cursor Management System) which is clocked by the current cursor to produce LATCHED CURSOR and hence SAMPLE CLOCK. However, due to beam switch settling times (particularly in 'Chop' mode) this latch may not be enabled unless 200ns have elapsed since the last Register Clock. (i.e. not within the 200ns after the Beam Switch register has been clocked.) Monostable U2673a provides this additional qualification. When HOLD ENABLE is high, D2603 conducts and sets U2673a, holding ENABLE LATCHED CURSOR high (inactive). (In this mode μB12 is high and so U2632e output is low and D2605 cut off).

If a REGISTER CLOCK now occurs then U2673a Q will go high (its D input is HOLD ENABLE which is high) and allow pin 4 (Reset) to rise at a time constant of R2687, C2686 (200ns). When pin 4 begins to take $\overline{Q}$ high, positive feedback via C1685 provides 'snap action' on the reset, and Q quickly falls low again.

When $\overline{\text{ENABLE}}$ LATCHED CURSOR is low, U1610b (Cursor Management circuit) D input is low and the next current cursor clocks U1610b Q low and Q high i.e. LATCHED CURSOR is high. In turn this takes U2637d output high and since μB11 is high holding U2637b pin 6 at Vbb, U2637b output goes low. Q2607 turns on, Q2606 off and SAMPLE CLOCK is produced.

4.13.4.3 REAL-TIME ACQUISITION

In real-time capture modes (post- and pre-trigger) the instrument Y channel is sampled once for every cycle of a programmable frequency clock. The ADC system converts each sample to a digital value which is stored in one of the two trace stores. After each conversion the store address is incremented. Capture ceases when all store locations have been filled.

Unlike repetitive capture mode, real-time capture is executed wholly by hardware (except for software initiation and data sorting), since the programmable clock rate may be as high as 1MHz.

When capture is armed the current instrument state is saved by software so that data display can be disabled, normal trigger selected and the beam switch set for the appropriate channel(s). When capture is complete the instrument state is restored.

In real-time capture modes CHOP STROBE SELECT (See Display Management circuit diagram) is set low. This allows tristate buffer U2427b to pass PROG CLOCK to counter U2446a whose Q0 output divides this frequency by 2 to give MEMORY CLOCK. The actual MEMORY CLOCK rate selected depends on Timebase range and specific values will be found in Table 4.13.9.

In the following description, reference will be made to Fig. 4.13.5.

μB3 is low so that $\overline{\text{WE}}$ of the store RAMs is controlled by RAM $\overline{\text{WE}}$ via U2664c and tri-state buffer U2668a.

μB5 low allows RAM $\overline{\text{WE}}$ to pass via U2650d, U2665a and U2612a to enable tri-state buffer U2667 to write ADC data to stores.

μB6 low enables U266c to pass BUSY to U2662a.

μB7 high enables tri-state buffer U2647b to allow the positive edge of $\overline{\text{WE}}$ $\overline{\text{RESET}}$ to clock the Acquisition Counter U2625,6,7.

μB8, μB9, and DISPLAY CLOCK ENABLE are low disabling U2647a,c,d.

Post-trigger and pre-trigger capture in single channel will be described, followed by operation in dual channel.

POST TRIGGER OPERATION

Refer to column 3 of Fig. 4.13.5 and Fig. 4.13.10. $\overline{\text{PRE}}$ $\overline{\text{TRIG}}$ is high and so U2666d output is high enabling tri-state buffer U2668c and disabling U2668d.

Acquisition is not requested by software until A ramp is not running and thus when ACQUISITION REQUEST clocks U2671a Q high, $\overline{\text{AQ}}$ is high and U2601b output goes high clocking U2671b via U2668c. HOLD ENABLE is thus asserted and will remain so until acquisition is complete.

μB19 holds transmission gate U2639d off and U2639a on so that U2671b Reset input is driven from TERMINAL COUNT P2, (terminal count from acquisition counters U2625,6,7).

The Sample Head/ADC system will now hold and convert one sample for every SAMPLE CLK.

A cursor (Cursor 1 for A sweep, Cursor 2 for B sweeps) is positioned close to the start of the sweep selected so that when the instrument is triggered, AQ goes high followed shortly by LATCHED CURSOR going high.

μB11 (high) enables U2637b via Q2608 so that when LATCHED CURSOR is high, SAMPLE CLOCK is controlled by monostable U2673b.

When the beam switch is in either the CH1 or CH2

Timebase Range	MEMORY CLOCK frequency Single Channel	Dual Channel	Proportion of store filled	
.5s/cm	200Hz	400Hz	100%	
.2s/cm	500Hz	1KHz	100%	
.1s/cm	1KHz	2KHz	100%	
50ms/cm	5KHz	10KHz	100%	
10ms/cm	10KHz	20KHz	100%	
5ms/cm	20KHz	40KHz	100%	
2ms/cm	50KHz	100KHz	100%	
1ms/cm	100KHz	200KHz	100%	
.5ms/cm	200KHz	400KHz	100%	
.2ms/cm	500KHz	1MHz	100%	
.1ms/cm	1MHz	1MHz	100%(Sgl.)	50% (Dual)
50μs/cm	1MHz	1MHz	50%	25%
20μs/cm	1MHz	1MHz	20%	10%
10μs/cm	1MHz	1MHz	10%	5%
5μs/cm	1MHz	1MHz	5%	2.5%
2μs/cm	1MHz	1MHz	2%	1%

Fig. 4.13.9 MEMORY CLOCK Frequencies for Timebase Speeds

state U2637c output will be low enabling U2673b D input for clocking. μB12 is low, so MEMORY CLOCK passes through U2634d to clock U2673b, and U2673b R input is low (via D2606). Monostable operation is as described for U2673a (section 4.13.4.2) but with 100ns period.

The monostable produces a negative going pulse of width of 100ns at Q2607 base which produces SAMPLE CLOCK at the collectors of U2606,7.

Acquisition now occurs once for every SAMPLE CLK i.e. once for every MEMORY CLOCK. The circuitry associated with this acquisition process is described in section 4.13.4.1.

μB0 is high so that during acquisition the output of U2642a is high (the other inputs to U2642a are: $\overline{DSP2}$, high, as the software disables data display during acquisition, and CSR $\overline{BLK}$ $\overline{ADD}$ also high). Hence the cursor RAM U2624 has $\overline{CS}$ high and will not be corrupted.

μB14 is low and so transmission gate U2630a is on, U2630b off. This allows U2627 Q, to drive A9 of the RAMs via buffer U2631c. (straight binary count). Also U2630d is off and U2630c on, allowing U2627 Q2 to drive TERMINAL COUNT P2.

For timebase speeds less than 50μs/cm and when 1024 samples have been stored U2627 Q2 goes high producing TERMINAL COUNT P2. μB19 is low and so U2639d is off, U2639a on and thus terminal count resets U2671b to terminate acquisition and generate ACQUISITION INTERRUPT by clocking U2609a.

At higher speeds where less than 1024 samples can be captured within one timebase sweep, the acquisition is aborted by the processor after one full timebase sweep. The captured samples are then redistributed by the processor with non-relevant positions blanked by the cursor RAM U2624 (see section 4.12). Table 4.13.9 shows the proportion of a store filled for a given timebase range.

PRE-TRIGGER OPERATION

Pre-trigger acquisition may be thought of as having three distinct phases:-

1. Flushing phase, where all locations in the pre-trigger store are written to – with trigger disabled – so that all old data is removed (this fills the pre-trigger store with pre-trigger data);
2. Pre-trigger phase, where trigger is re-enabled but writing continues to the pre-trigger store until trigger actually occurs;
3. Post-trigger phase, where data is captured after the trigger event.

In the 5110, pre-trigger data is stored in the lower 512 locations of the particular store, with post-trigger data in the upper 512 locations. (50% pre-trigger). Pre-trigger capture timing is shown in Fig. 4.3.11.

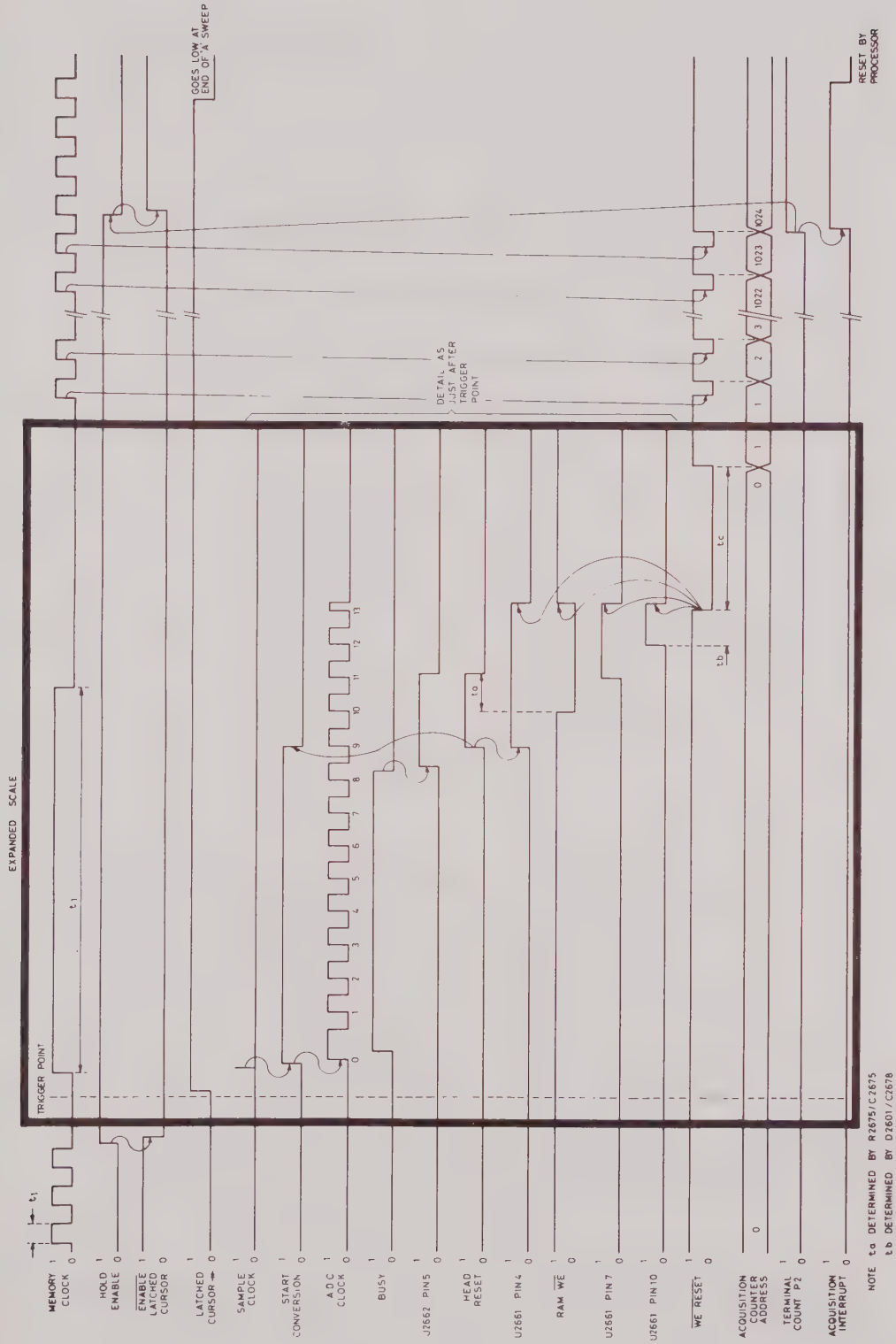


FIG 4.13.10. TIMING FOR REAL TIME POST-TRIGGER CAPTURE

Fig. 4.13.10 Timing for Real-Time Post-Trigger Capture

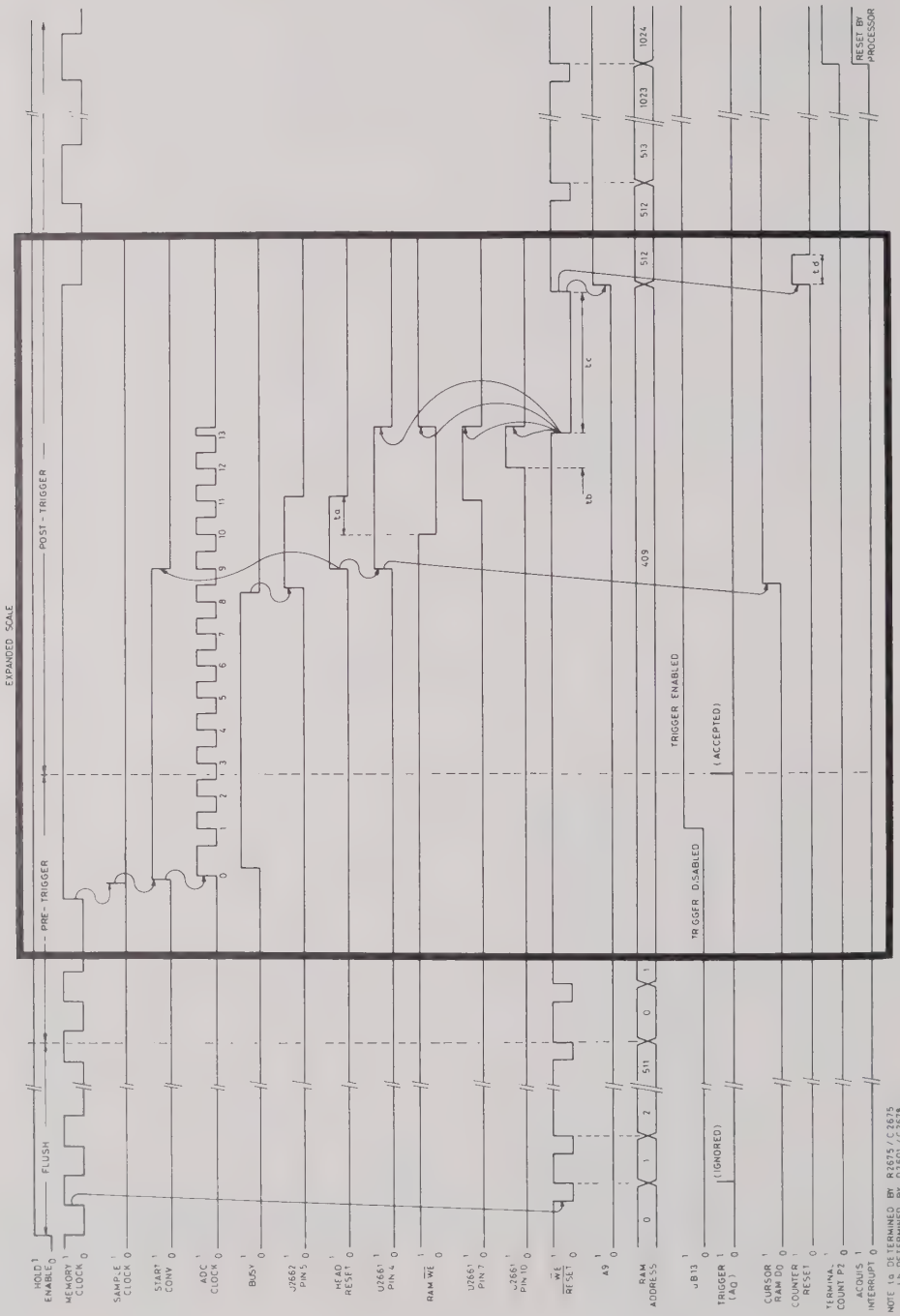


Fig. 4.13.11 Pre-Trigger Capture Timing

The acquisition hardware, once initiated holds store address line A9 low and starts acquiring data to all locations in this half of the store. The software allows a delay for this to happen (e.g. 25ms for timebase range 5ms/cm) and then enables trigger. Pretrigger data is written to the store until trigger occurs. During the pre-trigger phase the counter is allowed to 'overflow' from Ao–A8 all high to all low, thereby 'joining' the pre-trigger store end to end. As trigger is an asynchronous event the writing point in the store is arbitrary, and so the trigger point is marked with a change in one bit of the cursor RAM. A9 then goes high and writing proceeds linearly from the lowest of the upper 512 locations where post trigger data is stored.

Software is later used to move data in the pre-trigger store so that it aligns correctly with the post-trigger store. This mechanism is illustrated in Fig. 4.13.12.

$\overline{\text{PRE TRIG}}$ will be low, holding U2666a output high, U2666d output low. Tri-state buffer U2668d is thus enabled and U2668c disabled. ACQUISITION REQUEST goes high clocking U2671a Q high. UNCON. ACQ. EN. then goes high and clocks U2671b $\overline{Q}$ low and asserts HOLD ENABLE thus forcing the start of acquisition. μB11 is low, so Q2608 is conducting holding U2637b pin 6 low. U2637a is thus free to drive Q2607 base. A SAMPLE CLK pulse is produced for every MEMORY CLOCK by U2673b (for description see Post-trigger section).

Samples are taken and converted for every MEMORY CLOCK and since μB14 is high, store address line A9 is controlled by U2649a Q via U2630b. The three pre-trigger control bistables U2648a,b and U2649a were reset by $\overline{\text{AQRQ}}$ in the period between U2671a and U2671b being clocked. Hence A9 will be low initially and the lower 512 bits of the selected store are written to, flushing the pre-trigger store.

μBO is low and this holds U2642a output low and also the $\overline{\text{CS}}$ of cursor RAM U2624 so that the state of U2648bQ (initially low) is written to Do of U2624 via tri-state buffer U2612d, thus marking locations as pre-trigger.

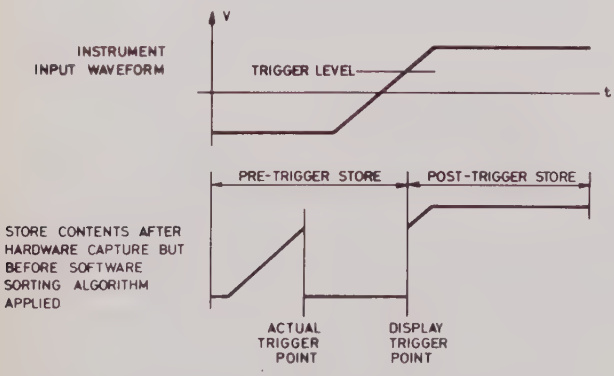


Fig. 4.13.12 Example Waveforms During Pre-trigger Acquisition

Once sufficient time has elapsed for the pre-trigger store to be cleared, the processor takes μB13 high. This enables U2648a Q to be clocked high by the next AQ (signifying trigger).

μB8 being low enables U2665d via U2635d and U2644d. Thus when U2662a Q goes high (see Fig. 4.13.5) it clocks U2648b Q high causing a 1 to be written into the cursor store to mark the trigger event.

U2649a Q must now drive A9 high but must not change until sufficient time has been allowed for this bit change to be written to U2624. Hence U2649a is only clocked when $\overline{\text{WE RESET}}$ goes high at the end of the same conversion.

Monostable U2609b now produces a pulse of duration 330ns to reset U2625,6,7 via U2644a. Further store writing thus takes place from the first post-trigger location.

When U2627 Q1 goes high, signifying all 512 locations of the post-trigger store updated, U2631a output goes high and produces TERMINAL COUNT P2 to terminate acquisition.

DUAL TRACE OPERATION – Reference columns 4 and 6 of Fig. 4.13.5 see also Fig. 4.13.13

In this section components with prefix 2400 refer to the Display Management circuit diagram.

In Dual Real-Time Acquisition the instrument is temporarily forced into 'chop' mode but with the Beam Switch switching between CH1 phase and CH2 phase only. (See section 4.11 for full description).

As will be seen from Table 4.13.9, MEMORY CLOCK runs at twice the frequency required for single channel (for a given timebase speed) – but subject to the same maximum of 1MHz. Note that two conversions are required for every counter address, one for CH1 (to Store 1) and one for CH2 (to Store 2). As before, every SAMPLE CLOCK, occurring with MEMORY CLOCK, initiates a sample/convert sequence as described in section 4.13.4.1 but the Acquisition Counter U2625,6,7 is clocked on every other acquisition by QUAL. Φ2 via U2647c, (as μB8 is high); see Fig. 4.13.13 QUALL Φ2 is generated by U2649b where Φ2 is clocked through on WE going high. See section 4.13.4.1 for details of Φ2.

In Post-trigger mode U2649b is initialised into the Φ2 state (QUAL Φ2 high) by a brief negative going pulse issued by the processor on μB1. This is to ensure correct phasing of the counter clock relative to beam switch changes and thus routes each channel to its correct store. This pulse is not required in pre-trigger mode since the flushing process ensures correct initialisation of U2649b.

4.13.5 DATA WORD ACQUISITION

Outputs from the Data Word Pod are fed to the Acquisition PCB via the Pod Interface PCB; (prefix for component references is 3300). This unit may be configured to pass the data word directly through or to introduce a 120ns delay to compensate for that of the Y channel delay line.

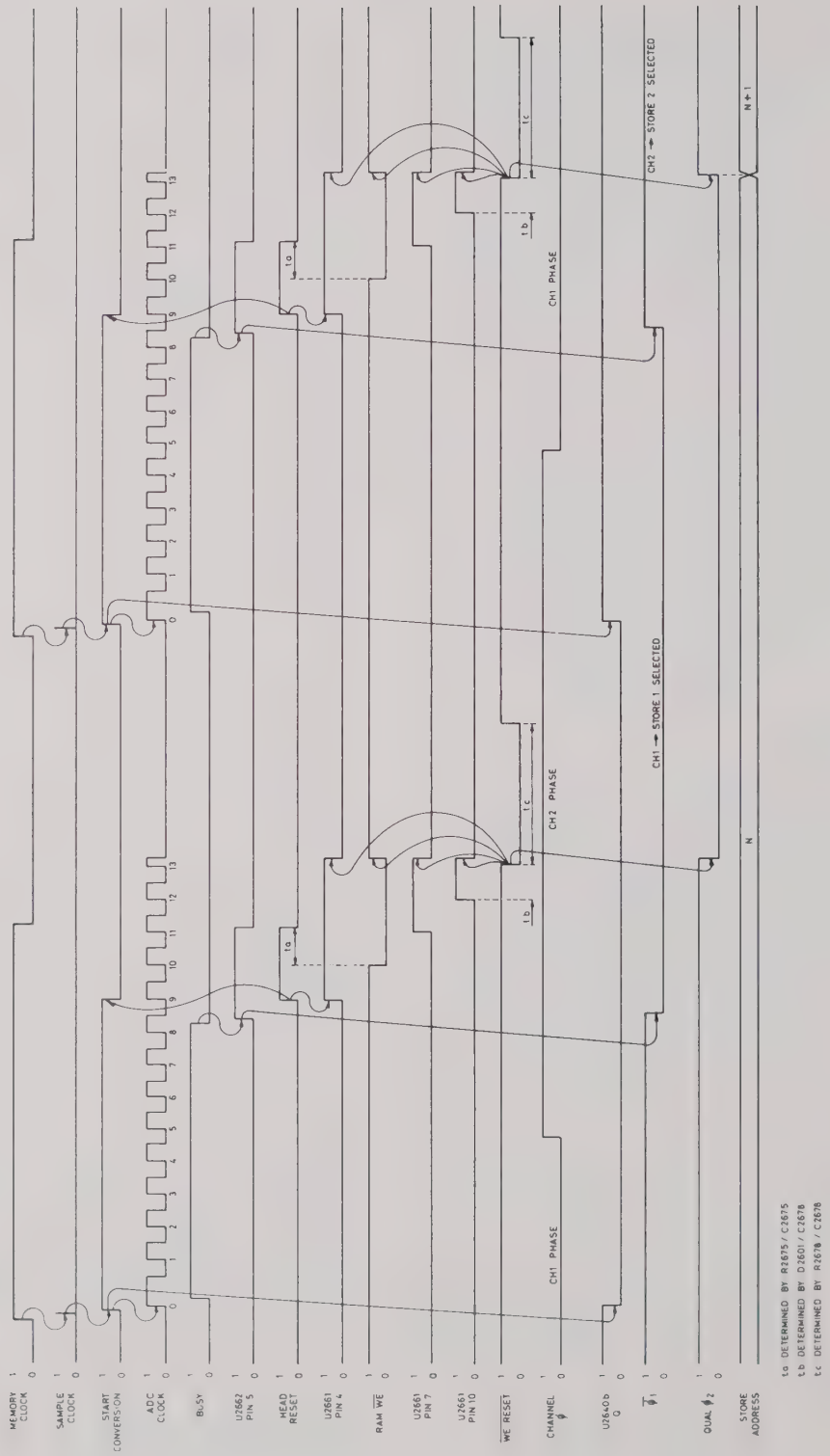


Fig. 4.13.13 Dual Realtime Capture

To capture the trigger word the delay is not required and so the processor sends POD DELAY $\overline{IN}$/OUT (U2606 Q7) high. This disables tri-state buffer U3305, turns on Q3301 and enables U3306 to pass data directly through.

In current cursor mode POD DELAY $\overline{IN}$/OUT is low, disabling U3306 and enabling U3305 to the data word from the digital delay comprising U3301, 2,3,4 and associated R–C time constants.

The data word from the Pod Interface PCB is taken via conditioning comparators U2617,8 to the Data Word Latch U2616. The processor may read this latch by reading address $C07 which takes U2665b output low to take U2616 $\overline{OE}$ low; and U2642b output low to enable buffers U2603,4 for reading.

The logic to drive LATCH DATA WORD and thus latch pod data via ECL/TTL converter U2638c, is physically part of the Delay System. (Component prefix 1500).

In trigger word mode, the processor takes Q2 of U1566 TRIG WORD SAMPLING low. Hence when $\overline{A\ TRIG}$ and $\overline{B\ TRIG}$ are both true (it is assumed they are connected to Trigger and Clock outputs respectively from the pod). U1568c output goes high and asserts LATCH DATA WORD via ECL line driver U1569e.

In current cursor mode Q1 of U1566 ($\overline{ENABLE}$ CURRENT CURSOR ASYNC) is taken low by the processor. Hence when the selected cursor clocks U1567a Q low, after a delay set by R1596 and C1575, U1569a output goes high and causes the data word to be latched. U1567a S input goes high at this time and returns U1567a Q high.

4.13.6 PLOTTER SYSTEM (See DATA DISPLAY circuit diagram)

The Plotter system actively employs both hardware and software. PROG. CLOCK is set for the required plot rate and generates a processor $\overline{FIRQ}$ (Fast Interrupt Request) once per cycle. The processor then initiates transfer of data from the required store to the plotter X and Y DACs.

When plotting commences the PLOT MARKER output from U2767 Q4 goes high along with Q5 to enable $\overline{FIRQ}$ generator U2753b.

When PROG. CLOCK goes high U2753b $\overline{Q}$ goes low and generates $\overline{FIRQ}$. The processor responds by taking U2767 Q6 high to enable transmission gate U2709c. The processor then executes a dummy read of the next store location to be plotted, and this takes U2742a output low and U2753b is reset via U2744a. During this instruction the address and contents of the required location are placed on the Display BUS and when TRANSFER CLOCK goes high (See Fig. 4.15.3 – Extended Cycle Timing) this data is clocked into the plotter latches U2750,1,2. U2767 Q6 is then returned low so that Display Bus activity may continue without corrupting plotter output waveforms.

The plotter Y DAC, U2763 produces an output current (IOUT, $\overline{IOUT}$) proportional to its digital input value and reference current, (set by R2761,3,7). The following amplifier U2764 produces a bipolar output voltage whose centre-zero may be set with R2764. Overall amplitude may be set by R2763 which adjusts the DAC reference current.

The plotter X DAC, U2761 again produces an output current (IOUT1) proportional to its digital input value and reference input. The DAC with internal resistive feedback works in conjunction with U2762 to produce a negative voltage at U2762 output. The following stage, U2765 corrects this for sign and amplitude.

Zero adjustment is by means of R2762 and amplitude by R2771.

4.14 VOLTAGE GENERATION SYSTEM

4.14.1 BLOCK DIAGRAM & GENERAL DESCRIPTION

The voltage generator of the 5110 has the function of supplying the instrument with eight accurate voltages (four cursor shift voltages, two vertical shift voltages, a horizontal shift voltage, and one for future expansion). These voltages are required to be programmable by the microprocessor software and be accurate enough for use in horizontal and vertical measurements.

The action of the circuit is to convert 8 independent 16 bit numbers into 8 independent analogue voltages. To this end, each number in turn is read from the scratch-pad ram and presented to the 14 bit DAC. The resultant analogue voltage is stored on a sample & hold capacitor and buffered to produce a low-impedance output. Unless the processor stops the system to update one of the numbers the system will cycle continuously, topping up the charge in each capacitor before the droop reaches a significant fraction of one bit resolution.

The processor may only access the scratch-pad at a specific point in the cycle when all sample capacitors are fully isolated to avoid disturbing the outputs. For a similar reason the cycle stops until the processor relinquishes access. The processor access time is therefore kept to a minimum to avoid excessive droop.

The voltages are supplied by a compound 14 bit digital to analogue converter (DAC), comprising a 10 bit DAC and an overlapping 8 bit DAC.

The output of the 14 bit DAC is multiplexed to produce the 8 separate outputs using a one-line to eight line multiplexer with 8 sample and hold circuits. Feedback is applied via an 8 line to 1 line multiplexer to ensure all the 8 outputs correctly follow the DAC output. (see Fig. 4.14.2).

Of the eight outputs, V_{00}, V_{01}, V_{02}, V_{03} go to the timebase board to supply the cursor shift movement, and V_{06} supplies the X shift movement. V_{04} and V_{05} go through the shift scaling circuit before going to the Y-preamplifier board to supply the vertical shift movement. The shift scaling circuit modifies the shift voltage according to the attenuator setting of the channel, so that the voltage always represents a constant number of centimeters on the screen.

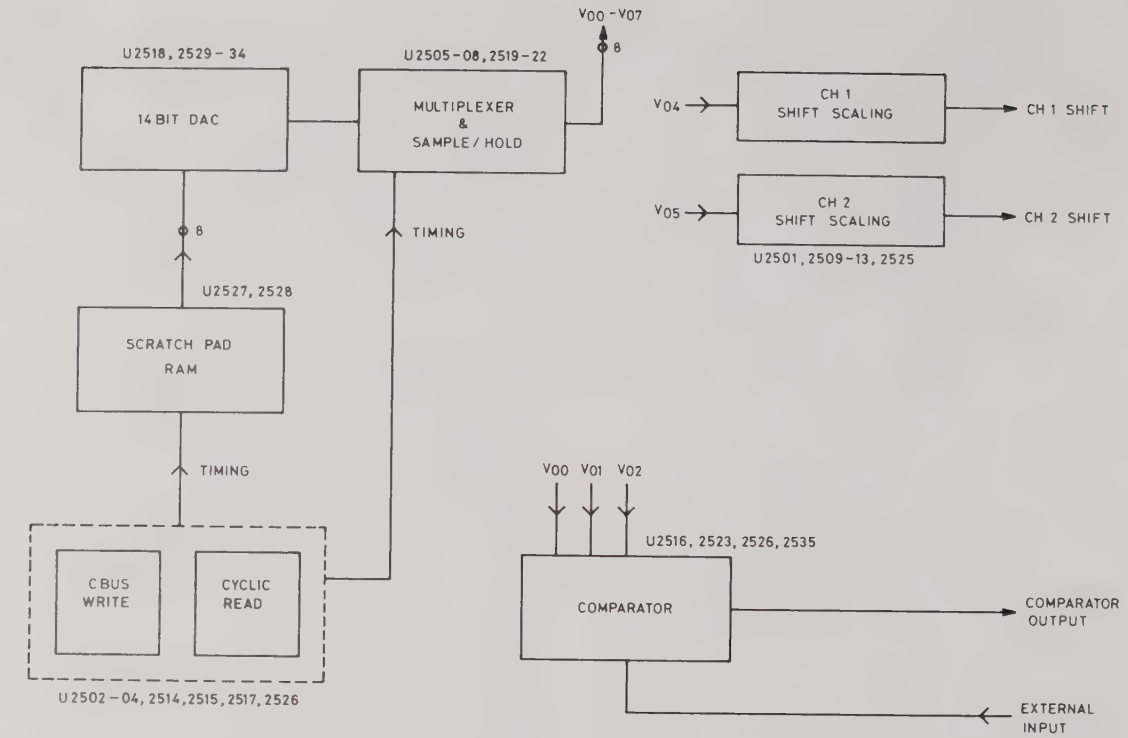


Fig. 4.14.1 Voltage Generator Assembly Block Diagram

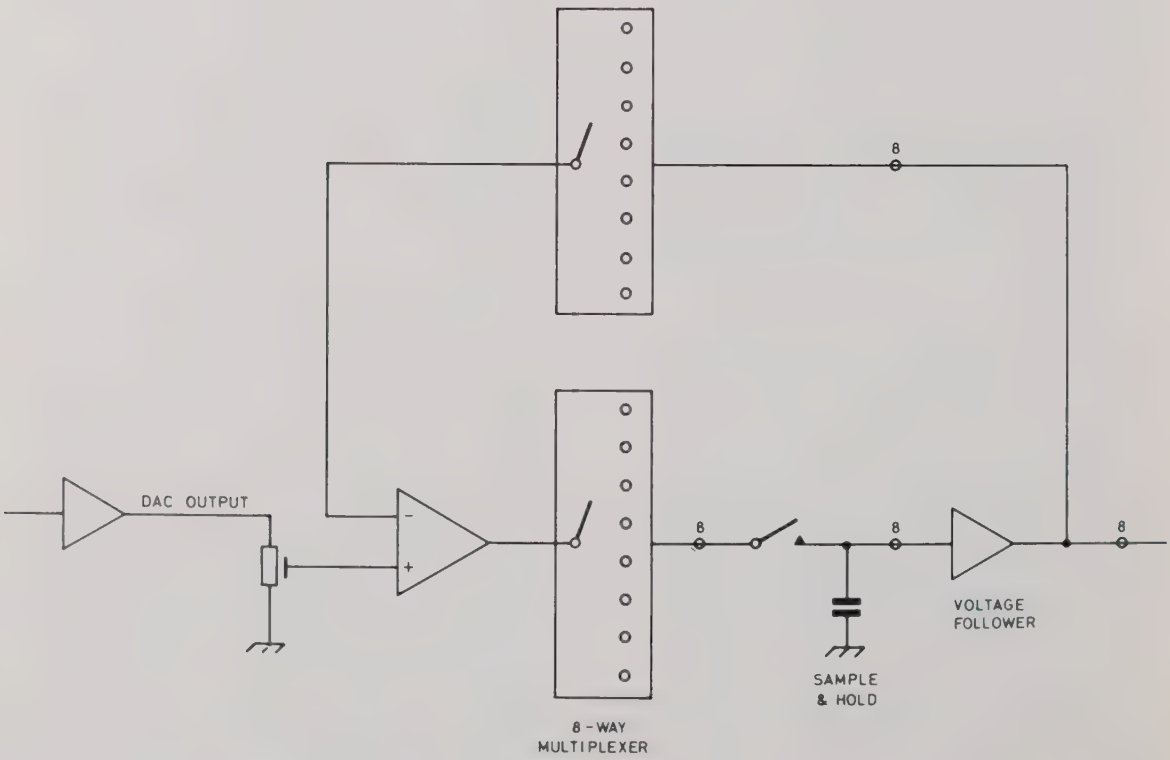


Fig. 4.14.2 Analogue Multiplexer & Sample Hold Block Diagram.

The scratch-pad RAM is a random access memory in which are stored eight 16 bit values corresponding to the eight voltage outputs from the DAC. Each value can be updated independently by the microprocessor in order to change that particular output. The microprocessor has write-access only to the scratch pad RAM via the C-Bus. The eight values contained in the RAM are sent in sequence to the DAC, to be sampled by the sample and hold circuit. This sequence is performed by the scratch-pad read circuit.

Finally, in order to calibrate the 14 bit DAC, and correctly adjust the matching between the 10 bit DAC and the 8 bit DAC that comprise the DAC circuit, a precision comparator is available. This can be configured to make a comparison between two V-gen outputs, or between one V-gen output and an external reference. By adjusting the voltage generator outputs, and reading the comparator output, the microprocessor can calculate appropriate corrections (ref. section 4.17.3).

4.14.2 14 BIT DIGITAL TO ANALOG CONVERTER

The DAC consists of two smaller DAC's combined together to give extra resolution. U2530 is a 10 bit DAC, of which the top 8 bits are used to give the most significant bits of the combined circuit. U2531 is an 8 bit DAC, which overlaps the bottom 4 bits of U2530 to give the least significant bits of the combined circuit. In other words, 2 bits overlap the least significant used bit of U2530. For an overall swing of 8 volts, the most significant bit of U2530 will contribute 4 volts, the most significant bit of U2531 will contribute 1/16 volts and the least significant bit of U2531 will contribute $\frac{1}{2048}$ volts thus the resolution of the DAC is roughly 0.5mvolts.

U2529 supplies the reference voltage to the DAC's U2530 and U2531. Its value is about 7 volts and is extremely stable. The digital signals to U2531 are supplied direct from the Q outputs of the scratch-pad RAM, while those to U2531 are supplied via the octal latch U2518. Because the digital input to U2531 is not latched, its output will vary at twice the rate of U2530 see Fig. 4.14.3. It is left to the sample and hold circuitry to sample the voltage at the right time.

The output from U2530 consists of two push-pull current sources I01 and I02, on pins 1 and 2. These drive operational amplifiers U2532 and U2533 as a current to voltage

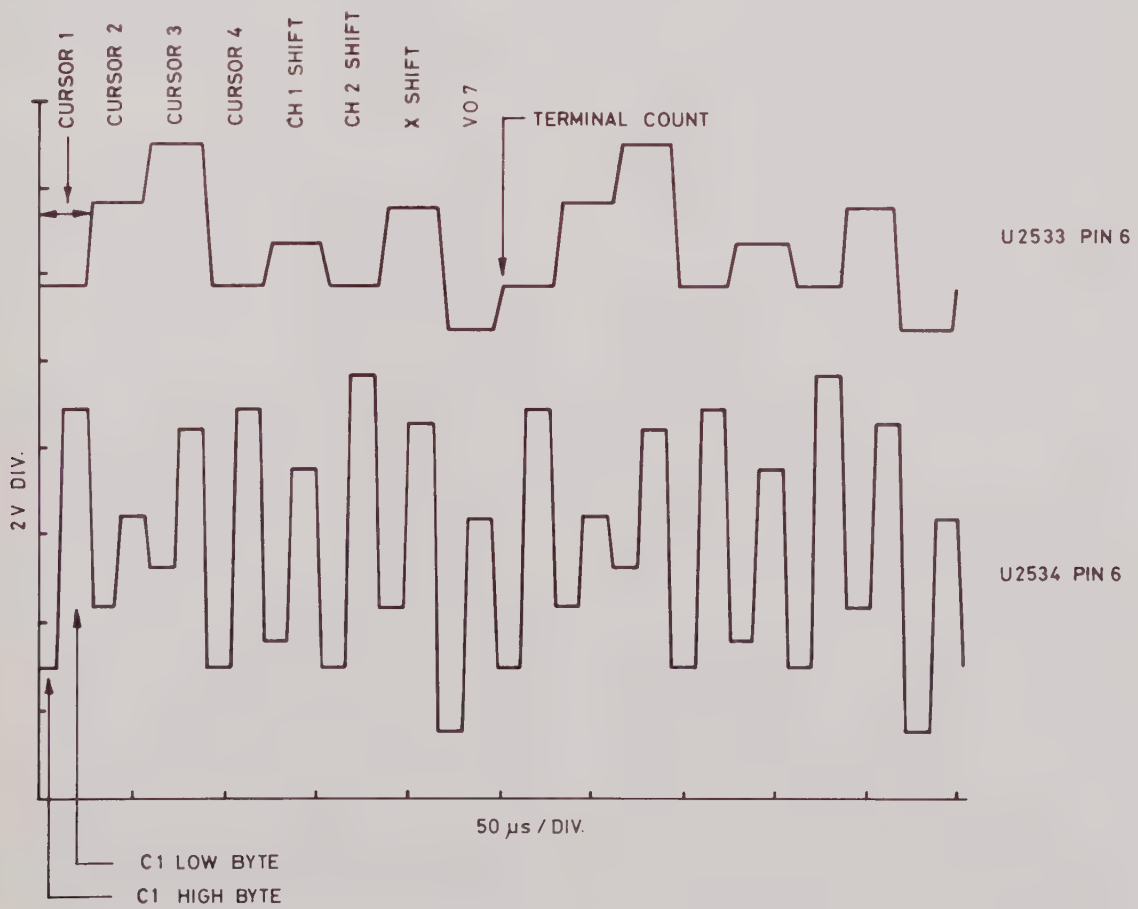


Fig. 4.14.3 Major and Minor DAC Typical Outputs

converter, while C2557 and C2558 optimise the pulse response of the circuit.

Similarly, the output from U2531 is two currents, I01 and I02, on pins 2 and 4, proportional to the product of the reference input and the digital input. They drive a simpler current to voltage converter U2534, with pulse response correction from C2527 and C2528. The outputs from the two DAC's are combined by resistors R2519 and R2514 in the ratio roughly 1:64, and the overall range of the DAC pair can be adjusted for calibration by R2505. Preset potentiometer R2507 is used to make slight changes to the relative gains of the two DAC's by altering U2531's reference voltage.

See section 4.17.3 for a description of how the two DAC's are combined to give a linear montonic output.

4.14.3 EIGHT WAY MULTIPLEXER AND SAMPLE/HOLD CIRCUIT

A simplified block diagram of the multiplexer and sample and hold circuit is shown in Fig. 4.14.2.

The output from the DAC passes through a voltage follower, U2520, where it is multiplexed 8 ways by U2507. C2580–2587 are sampling capacitors that store the voltage until it can be resampled. A set of eight voltage followers, U2522 and U2519 buffer the voltages before they are sent to the rest of the instrument. To complete the circuit, the eight voltages are multiplexed back to one line and fed back to U2520 as negative feedback.

U2520 is fed with the signal from the 14 bit DAC. It is configured as a voltage follower, when the analog switches are closed. When the switches are open, it runs at open loop gain and requires D2501 and D2502 to limit its output excursions and prevent saturation.

R2506 is preset to adjust its DC offset. Capacitors C2570–2577 smooth the output slightly before they go to the analog switches U2508 and U2506 used for further isolation. The networks of capacitors and resistors following these analog switches have two purposes. The main purpose is to store the sampled voltage until the next sample can be taken. This function is performed by C2580–2587. Resistors R2530–2537 correct an unwanted absorbtion characteristic of the capacitors. The other function of the network is to cancel out the digital feed-through from the multiplexers. This feed-through which takes the form of a pulse is cancelled by an equal and opposite pulse produced by resistor pairs R2520–2527 and R2530–2537.

U2522 and U2519 are quad operational amplifiers wired as voltage followers. They buffer the eight voltage outputs from the voltage generator board. From here, the voltages are sent to the rest of the instrument. Voo to V03 go directly to drive the 4 cursor positions, V04 and V05 go to the CH1 and CH2 shift scaling circuitry, and V06 goes directly to drive the X-shift. Simultaneously, Voo, V01 and V02 go to the comparator circuit.

The eight buffered voltages are sampled by multiplexer U2521, to produce one line, to act as the negative feedback for voltage follower U2520.

Multiplexers U2502 and U2521 are driven by 3 lines, from the scratch-pad read/write circuitry, so as to remain in synchronism with the DAC and RAM. The inhibit line (pin 6) is pulsed so that they only sample the voltage when the DAC has a valid voltage output (see fig. 4.14.4 for timing diagram).

Analog switches U2508 and U2506 are driven by the 8 lines produced by U2505 and RN2501 from the same 3 lines (plus inhibit) as U2506 and U2508. They therefore switch at nominally the same times.

4.14.4 SCRATCH-PAD RAM AND READ/WRITE CIRCUITRY

The scratch-pad random access memory consists of two 16 x 4 bit memory devices used to store the eight 16 bit words corresponding to the eight output voltages.

The processor can have access to write to any locations in the RAM, via the CBUS data and address bus. When not being written to the RAM sends its contents in sequence to the DAC. To control the timing of this read sequence and to drive the multiplexer and sample and hold circuits in phase, a circuit based around an oscillator and a ÷ 16 counter drives the RAM and the multiplexer and sample and hold. When the processor wishes to gain write access to the scratch-pad RAM, it makes a request and waits for an interrupt to signify access permission is granted. The oscillator stops, and the processor can write to the RAM. The processor then releases the access request line, and the oscillator starts again.

NORMAL READ CYCLE

In the normal cycle, the oscillator, U2503 a and b supplies the timing pulses. It is enabled by a high on U2503a pin 2, and runs at about 12KHz. This line, GX, is high for normal read cycling and low for processor write access.

From this basic clock, U2504b and U2504a produce two out-of-phase squarewaves, see Fig. 4.14.4. U2504b clocks the address counter, via U2503c, U2524d, and U2504a allows the multiplexers to sample the generated voltage, via U2524c, U2514c, U2524b. U2524d clocks the ÷ 16 counter U2517, and the same timing signal goes through the two-way selector U2514a, U2514b, U2515b to the ME inputs to diable the RAM until the counter has settled. The 4 outputs from U2517 are address lines to the RAM. Q0 selects the upper or lower byte, while Q1 to Q3 select one of the eight 16 bit locations. Q1 to Q3 also go to the multiplexer and sample and hold circuits to sample the correct voltage output from the DAC. Because the 16 bit value in the RAM is read out in two steps of eight bits (top 8 first, stored in octal latch U2518, then bottom 8) the multiplexers are disabled until the full 16 bits are applied to the inhibit lines on the multiplexers U2521, U2507 and U2505 for this purpose. A similar signal is used to latch the top eight bits into U2518 at the correct time. This signal is produced by U2514d.

Because U2502b pin 12 ($\overline{GX}$) is high, U2515b is disabled (disabling access from CBus) as is U2515d, holding the write enable lines on the scratchpad RAM (U2527

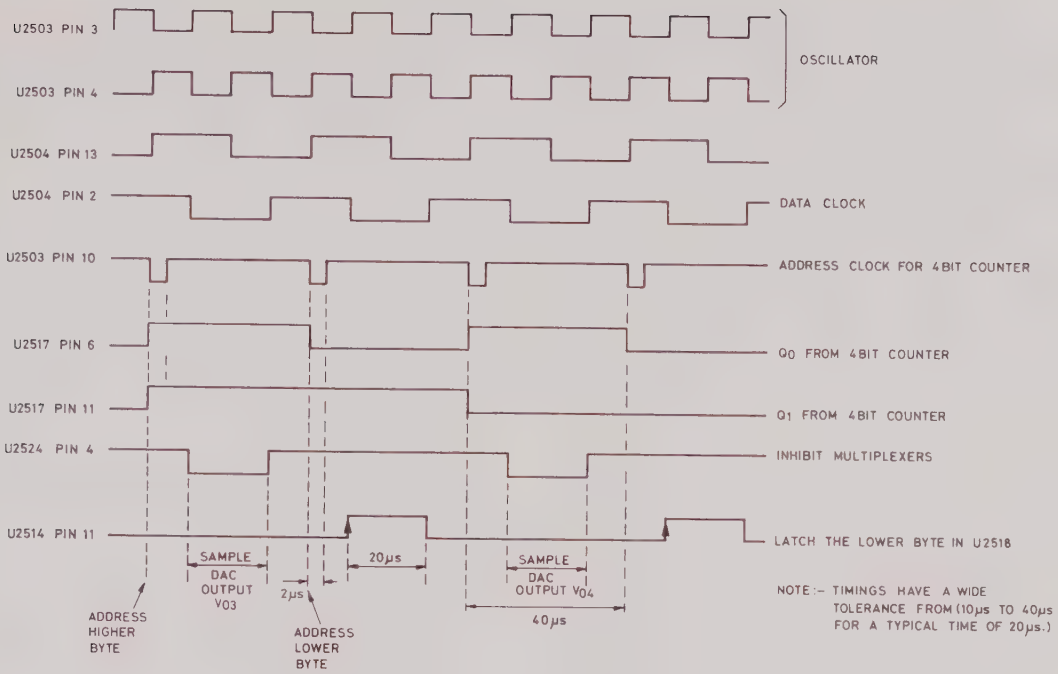


Fig. 4.14.4 Scratchpad Read Timing Diagram

and U2528 pin 3) high, keeping the RAM in read mode.

C-BUS WRITE SEQUENCE

U2502b controls access to the RAM. Normally its Q output is held low because port U2526, QO is driven low by the microprocessor. This enables the read cycle and inhibits any access to the scratchpad RAM from the C-Bus. When the processor wishes to write to the RAM, it sets U2526 pin 8 high as an access request and waits for access permission, in the form of an interrupt.

By writing a high to DO of port address $OD72, the high on U2526 pin 8 is clocked through to pin 9, and to the D input of U2502b. The oscillator will continue running and the 4 bit counter U2517 will continue counting until a full cycle is reached when the terminal count line U2517 pin 7 will pulse low. At this point the high on U2502b will be clocked through to the Q and $\overline{Q}$ outputs pins 13 and 12, signifying the start of external access.

The Q and $\overline{Q}$ outputs from U2502b control the whole switch over from reading to writing. The Q on U2502b pin 13 generates an interrupt notifying the processor of access permission. It also resets U2504a, so that the multiplexers U2521, U2507 and U2505 are turned off (Because of this the sample and hold capacitors are not refreshed and will gradually drift to Ov. So the minimum time is spent in this inhibited state). Furthermore, the preset enable pin on the 4 bit counter, U2517 pin 1 goes high, and U2517 goes transparent allowing C-Bus address to pass through to its outputs, Q0 to Q3 pins 6, 11, 14, and 2. U2514a is disabled and control of the scratchpad $\overline{MC}$ lines switches from U2514a to U2515d.

The $\overline{Q}$ output of U2502b, pin 12 has at the same time gone low. This turns off the oscillator, U2503a and b and enables U2515b.

The circuit has now switched over and is ready to accept data from the C-Bus. The processor puts address and data onto the C-Bus, corresponding to the information it wishes to update in the scratchpad RAM. The C-Bus data lines go directly to the data input (DO–D3) lines of the RAM, U2527 and U2528 pins 6, 4, 10, 12. Lines A0–A3 of the C-Bus address are coupled, via the 4 bit counter U2517 to address lines A0 to A3 of the RAM, pins 1, 15, 14, 13. When the processor writes to an address in the range $OF80 to $OFFF, U2515b pin 6 is pulsed low. This signal is coupled via U2514b to the memory enable pins 2 of the RAM U2527 and U2528. The RAM has thus been given address and data information, which will be clocked in when the write enable line goes low (pin 3). Pin 3 goes low when the C-Bus $\overline{E}$ line (U2515d pin 13) goes low to say that address and data are valid.

By this process, an 8 bit location is updated (4 bits each in U2527 and U2528). To update all 16 bits two such eight bit accesses are required.

Having written to the required locations, the microprocessor releases the circuit by writing a low to U2526 pin 8, (port $OD72). This low is clocked through to U2526 pin 9, Q0 output, and the circuit U2503d and

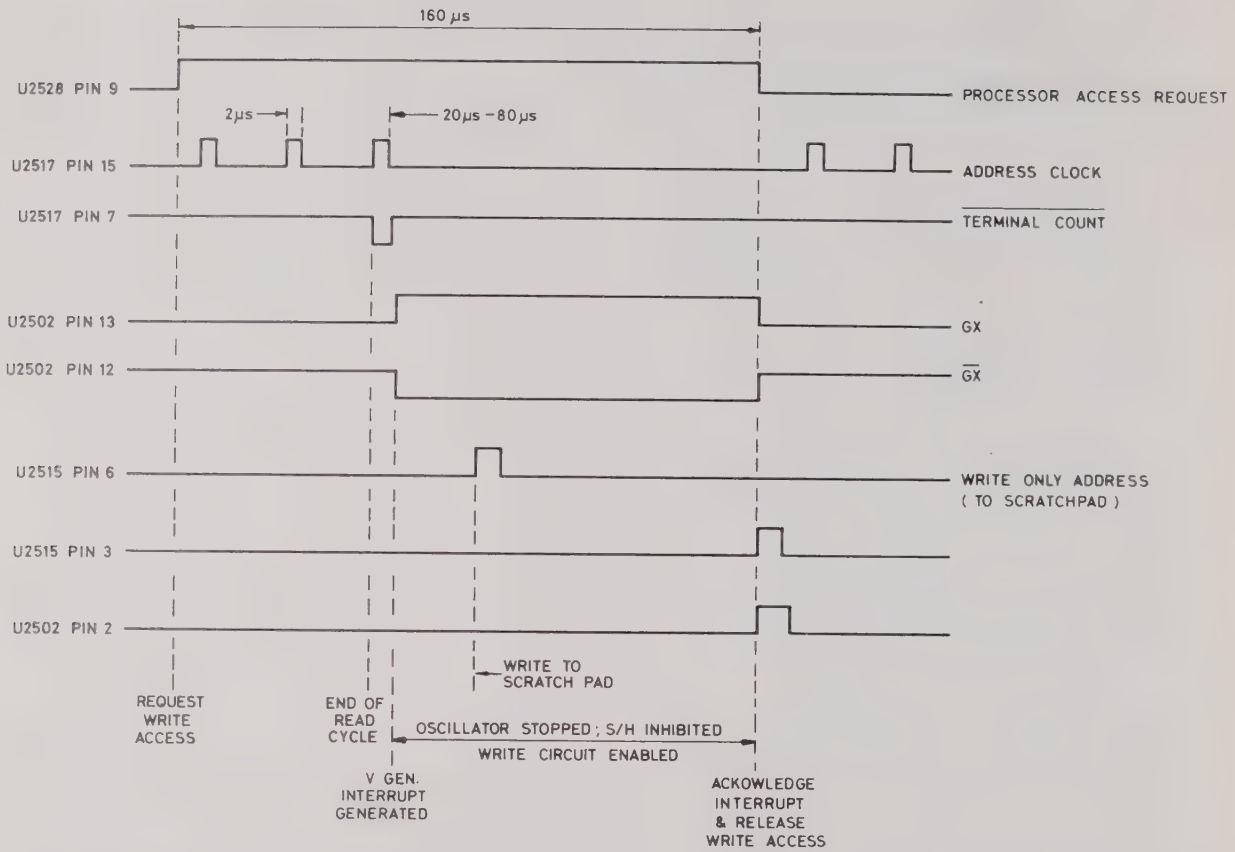


Fig. 4.14.5 Scratchpad Write Access Sequence

U2515a produces a positive going pulse which resets U2502a and U2502b. The Q and $\overline{Q}$ outputs of U2502b now revert to their normal state (Q is low, $\overline{Q}$ is high). This releases the interrupt (GX) from the processor; enables the oscillator, U2503a and b again; switches over the memory enable selector U2514b, U2515b, U2514a to disable C-Bus access and enable access from the read-access circuit; via U2524e, U2515d, U2515c and U2515b switches the RAM to read mode; and allows the multiplexers to sample again when required (i.e. releases the reset on U2504a). The final thing to happen before the circuit is functioning as normal is that the 4 bit ÷ 16 counter is reset. This is done by U2502a. The pulse from U2515a resets U2502 pin 2 low, thus resetting the counter U2517. This is necessary so that the counter starts from where it stopped at the end of the last read cycle. The low on pin 2 is not released until the trailing edge of the first clock pulse from U2503c pin 10. After that, U2502a pin 2 remains high until another write access sequence

The circuit is now functioning, as described before, sequencially reading values from the scratchpad RAM into the DAC.

4.14.5 CH1 AND CH2 SHIFT SCALING CIRCUITS

The function of the shift scaling circuits is to modify the range of the two shift voltages (V04 and V05 corresponding to CH1 and CH2 shift) according to the current attenuator setting of that channel. This is so that after going through the switched gain stages of the preamplifier (section 4.4.1) the shift voltage will always represent the same deflection on the screen(See Fig. 4.14.6 for block diagram).

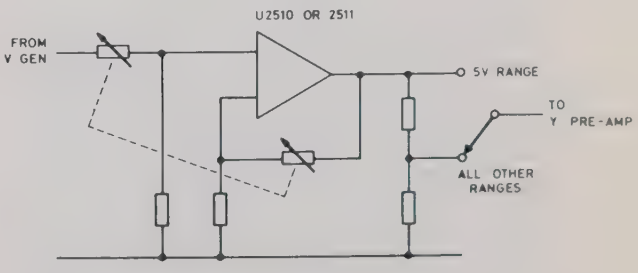


Fig. 4.14.6 Shift Scaling Block Diagram

The circuits for both channels are identical. They consist of operational amplifiers U2511 and U2510 with switchable gains and a further attenuation selection following them. The switching is controlled by the microprocessor via the port U2525 (port $OD74).

The dual 1 line to 4 line multiplexers U2509 and U2512 select the gain of the op-amp U2511 and U2510 by chosing a voltage tap-off from resistor networks N2502 and N2503. These operational amplifiers are configured as pseudo-differential amplifiers, with balanced impedance to eliminate common-mode noise and thermal drift problems. C2593 and C2594 improve the high frequency common mode rejection of the amplifiers. Preset potentiometers R2584 and R2583 adjust the dc offsets of the amplifiers.

The overall gain of the shift voltages can be adjusted for calibration by preset potentiometers R2581 and R2582. A final stage of gain selection is used only on the 5V/DIV setting of the attenuators. On all other ranges, the analog switches U2513a and U2513c are off, while U2513b and U2513d are on, routing the signals from the wipers through potential divider R2585, R2586 to drive the preamplifiers. In the 5V/DIV position, U2513a and c are turned on while U2513b and d are turned off so that an increased voltage is used to drive the preamplifier. The Table Fig. 4.14.7 shows the correct full scale outputs from the shift scaling circuits for the various preamplifier attenuator settings.

As mentioned above, the processor controls the gain switching by writing to port address $OD74, that is U2525. Outputs QO to Q3 go directly to the select lines of the multiplexers U2509 and U2512, while outputs Q4 to Q7 go through the level translater U2501. This changes the voltage levels from CMOS levels of 0/5V to the -5V/+5V required for U2513. Its reference voltage is supplied by R2589/R2590.

Attenuator Position	Peak to Peak Output (for ±32.7 Divs)
5V/Div	±4V
2V/Div	±1.6V
1V/Div	±0.8V
0.5V/Div	±0.4V
0.2V/Div	±1.6V
0.1V/Div	±0.8V
50mV/Div	±0.4V
20mV/Div	±1.6V
10mV/Div	±0.8V
5mV/Div	±0.4V
2mV/Div	±0.16V

Fig. 4.14.7 CH1 & CH2 Full Scale Shift Outputs

4.14.6 V-GEN COMPARATOR

This circuit describes the prevision comparator used to calibrate and adjust the voltage generator system.

Its function is to compare one of the voltage outputs (V00) with either another voltage output (VO1) with analogue OV or with an external voltage. This latter function is an option with components not normally fitted.

Comparison of two voltage outputs from the voltage generator system gives the microprocessor the facility to measure and adjust the linearity or monotonicity of the system (described in detail in section 4.17.4).

The various inputs to the comparator are selected by multiplexer U2523a and b. Selecting:-

XO compares V00 against V01, unfiltered

X1 compares V00 against V01, filtered

X2 compares V00, filtered, against analogue ground

X3 compares V00, filtered, against external input also filtered (this option not usually fitted)

The two inputs to the comparator are filtered by resistors R2554, 2555, 2556, 2557, and capacitors C2555 and C2556. Operational amplifier U2535a, b, d form a compound amplifier with very high common mode rejection and a differential gain of 1000.

As the resolution of the 14 bit DAC is roughly 0.5mV, this is amplified to a resolution of 500mV at U2535 pin 14. However, this resolution is only visible if VOO and V01 are almost identical, otherwise the amplifier will saturate. The output goes to a comparator U2535c, with hysterysis of roughly 50mV to improve noise rejection. Zener Diodes D2503 and D2504 limit the output swing of the comparator to CMOS logic levels and the output goes to the read only port $OC83, U2516. The microprocessor can read the comparator output by addressing this buffer, (via inverter U2524a), when its output will appear on the C-Bus data highway.

Offsets in the combined comparator circuit can be adjusted by preset potentiometer R2518 and by V02. Thus both manual and processor controlled offset is possible. VO2 is attenuated by R2568, R2564, R2518 so that 64 steps of VO2 only alter U2535d pin 14 by 100mV. It is thus a very fine adjustment. Coarse adjustment by R2518 is explained in section 4.17.3.

The processor controls the selection of inputs to the comparator by writing to port address $OD72. This latches the data on the C-Bus into octal latch U2526. Outputs Q1 and Q2 drive the dual multiplexer U2523, while outputs Q3, Q4, Q5 drive the 8 way multiplexer U2536 (if fitted), to select one of 8 external inputs (XO to X7.)

4.15 MICROPROCESSOR SYSTEM

4.15.1 GENERAL

The M.P.U. Board is housed in the card frame, being located in one of the three long-edge connector positions.

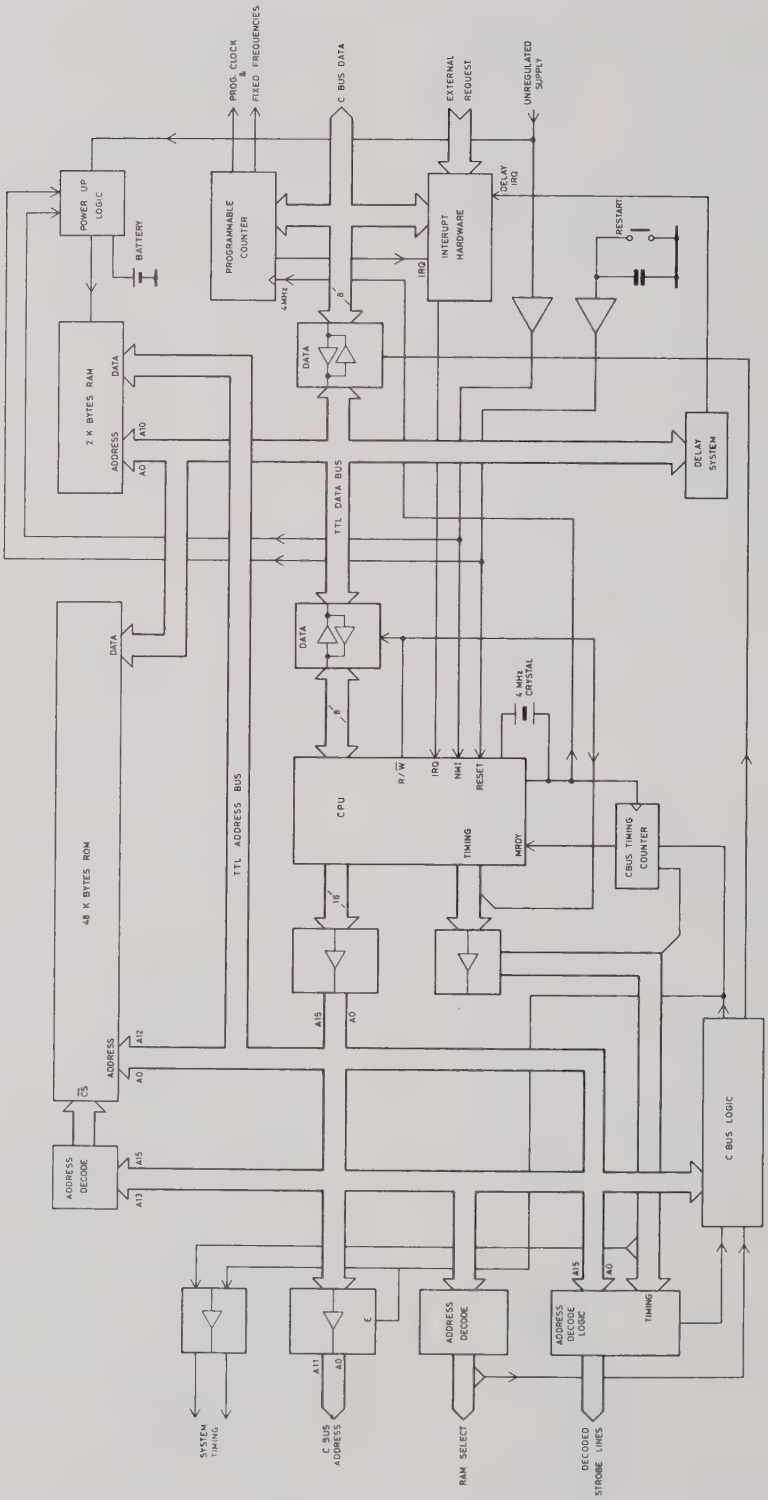


Fig. 4.15. Processor Block Schematic

On this board are the microprocessor, programmed ROM, address decoding, some non-volatile RAM, interrupt and slow peripheral interface hardware, A clock divider chain, and part of the delay system are also resident on this P.C.B.

4.15.1.1 MICROPROCESSOR

The device used is a 6809; an NMOS, 8 bit data, 16 bit address processor with a cycle time of 1μs. Only a brief description of relevant controls is contained below, for full information readers are directed to manufacturers data (Motorola, Hitachi).

4.15.1.2 MAJOR CONTROLS LISTED IN ORDER OF PRIORITY

RESET – highest priority, overrides all other controls. This line is active low and forces the microprocessor into the idle state. When RESET goes high, the program execution sequence is started, a two byte address held in rom at $FFFE, $FFFF is loaded into the program counter; this will be referred to as a vector fetch, and is signified by status lines BS (high) and BA (low). At power up, comparator U2012a and U2012c holds the microprocessor in reset until capacitor C2070 is charged, via R70. This ensures a delay of some 500ms whilst the crystal clock oscillator stabilises. Pushing switch S2001 forces a machine reset: releasing the push button causes a restart some 300ms later.

$\overline{\text{HALT}}$, $\overline{\text{DMA}}$ – next highest priority. These are reserved for use with options and are tied high, inactive by resistor network N2037.

$\overline{\text{NMI}}$ – non maskable interrupt. a negative going edge on this input is internally latched by the processor and causes suspension of normal operation. Subsequently a vector fetch from $FFFC, $FFFD causes execution of a service routine.

NMI is generated by U2012 which compares the unregulated power supply, via potentiometer R2072, R2082 with a preset voltage on the wiper of R2080. This pot is adjusted so that when the instrument is switched off an NMI is generated some milliseconds before the +5 volt supply becomes unuseable. This enables the program to end in a well defined way.

$\overline{\text{MRDY}}$ when a memory location is being addressed a low level on this input causes the cycle of operation to be stretched. In this system it is used to implement a slow, low activity data and address bus described fully in section 4.15.1.3.

$\overline{\text{FIRQ}}$ (Fast Interrupt Request). The action of this control can be masked (suppressed) by the processor. When enabled, and taken low, a vector fetch occurs from $FFF6, $FFF7, causing a service routine to be invoked. In the 5110 the use of this input is restricted to the data display system; (from U2753).

FIRQ is automatically cleared (set high) by addressing the trace stores.

$\overline{\text{IRQ}}$ (Interrupt Request). When granted, a low level on this input causes a vector fetch from $FFF8, $FFF9. An active low signal can be caused by any input to 'OR' gate U2051 going high. Several inputs can be simultaneously high, all have equal *hardware* priority. Part of the service routine examines the data read only port U2050 to determine the interrupt source, or sources.

Fig. 4.15.1, lists the cause of interrupts, and also the mechanizm used to return the particular line low. Of the two interrupts requests generated on board, REGULAR INTERRUPT occurs every 25ms and has a variable length service routine. Part of the service routine reads the setting of the front panel control switches, and in addressing this data latch automatically cancels the interrupt by the SET (Pin 8) of U2011. Software timers are also maintained by this routine.

TITLE	CAUSE	CLEAR BY	HARDWARE ENABLE
VOLTAGE GENERATOR	U2502	DATA TO PORT $OD72	✓
SHIFT	U1861	READ $OC86	
KEYPAD	U1860	READ $OC87	✓
END OF CAPTURE	U2690	ANY TRACE STORE ADC LATCH WORD LATCH	
END OF PLOT	RESERVED FOR OPTION		
IEEE	U2943	INTERNAL REGISTER U2552	✓
REGULAR	U2011	READ $OC04	
DELAY SYSTEM	U2062	DATA TO U2049	✓

Fig. 4.15.1 Interrupt Sources

XTAL, & EXTAL PINS 39 & 38. These form an oscillator circuit with crystal XL 2001, running at 4MHz.

This frequency is internally divided by the processor to form quadrature outputs Eout and Qout. These, normally at 1μs period, provide both internal and external timing signals.

The relationship between these signals is shown in Fig. 4.15.2, normal cycle timing. Eout is used by the microprocessor to latch data into the internal registers at the end of the cycle.

R/$\overline{\text{W}}$ (Read High; Write Low) is an output to signify the direction of data transfer. The state of the data buffers is dependant on this signal, when high, these are configured as inputs, when low as output.

Referring to Fig. 4.15.2. the start of a cycle occurs as Eout goes low. Internally generated address, data and R/$\overline{\text{W}}$

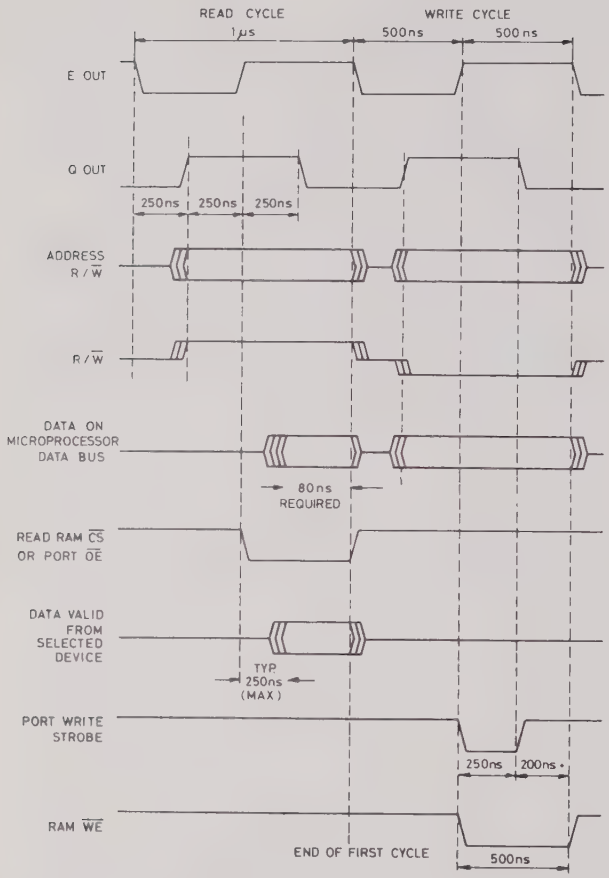


Fig. 4.15.2 Normal Cycle Timing

become valid at the processor pins on the rising edge of Qout, approximately 250ns later. At the half cycle point, Eout goes high, by which time address decoding has settled. In general chip selects ($\overline{CS}$) are produced by a suitable combination of uniquely decoded address; with Eout included as the timing signal. For RAM U2070, and read only ports U2067, U2068 ($\overline{CS}$ and $\overline{OE}$ are active low) data returned to the processor is required to be valid some 80ns before Eout returns Low.

This gives an access time of more than 400ns, worst case, from CS. Typically data is valid from RAM $\overline{CS}$ some 250ns after Eout low to high transition.

In the write cycle, access time for the write only ports U2049, U2060, U2061 need only be short and data is latched on the next defined transition, Qout going low. A write to RAM U2070 requires a longer access and a buffered Eout, from U2022 pin 5 is used to latch data into U2070 by taking write enable ($\overline{WE}$) high at the end of cycle.

ADDRESS OUTPUTS A0 – A15 are buffered by U2023 and U2024 which are normally permanently enabled. These introduce a delay of typically 12ns but provide a low impedance drive to the address lines which are taken to the backplane via the edge connector.

DATA INPUT/OUTPUTS D0–D7 (Pins 31 to 24) are buffered by a bi-directional device U2021, again normally permanently enabled by a low level on its Pin 19.

The direction of data flow is determinted by the control bit DR, Pin 1. This is driven from the microprocessor R/$\overline{W}$ inverted by U2022. When high, data is output to the TTL bus.

4.15.1.3 SLOW (C-BUS) INTERFACE – SEE FIG. 4.15 BLOCK SCHEMATIC AND FIG. 4.15.3. EXTENDED CYCLE TIMING

An extended cycle will occur for an address in the range $OC00 to $IFFF. CMOS buffers U2027 and U2028 for data, and resistor coupled buffers U2025 and U2026 for address, are enabled only when an extended cycle occurs.

The data and address bus so formed is called "C BUS", being CMOS compatible in terms of logic swing and speed. It is low activity in that only when data transfers occur on CBUS (A very small proportion of the total time) do the data and address buses become active.

The address range is decoded by U2030 and U2041, causing an OPEN CBUS on U2041 PIN 8. This signal inverted by U2018d, enables the address buffers; and via U2016 enables data buffers U2027 (D0 to D3) and U2028 (D4 to D7 dependant upon R/W.

Read gives U2016 pin 11 low, or write U2016 pin 8 low.

U2029 is a synchronous binary counter which is used to hold $\overline{MRDY}$ low for 6 crystal clock cycles (1.5µs) when an extended cycle is required. The counter is parallel loaded with a start value by taking $\overline{PE}$, Pin 9 low, coincident with a positive transition of clock; this occurs every microprocessor cycle. In a normal cycle this occurs every 4 clock periods and Q3 of the counter remains high, the count proceeds from $A counts $B, $C, $D then loads $A again.

When $\overline{OPEN\ CBUS}$ from U2018 d modifies the start count (Via D3 pin 6) to $2, Q3 of the counter is forced low on parallel load, synchronous with the clock to pin 2. MRDY connected to Q3 is held low causing the microprocessor to maintain Eout high, with data and address etc. valid. Six clocks later, on the count of $8, Q3 goes high and the microprocessor recognising $\overline{MRDY}$ on PIN 36, now high resynchronises the Eout high to low transition to the next quarter cycle, ending the extended cycle.

Note that as the data buffers are CMOS, typical enable times of 80ns can be expected. This data path is used extensively throughout the instrument to transfer data to write only control ports. The timing developed to latch data into these devices eg: U2052 is in the form of a unique address strobed by TRANSFER CLOCK U2017 PIN 6. This signal has a high ongoing edge some

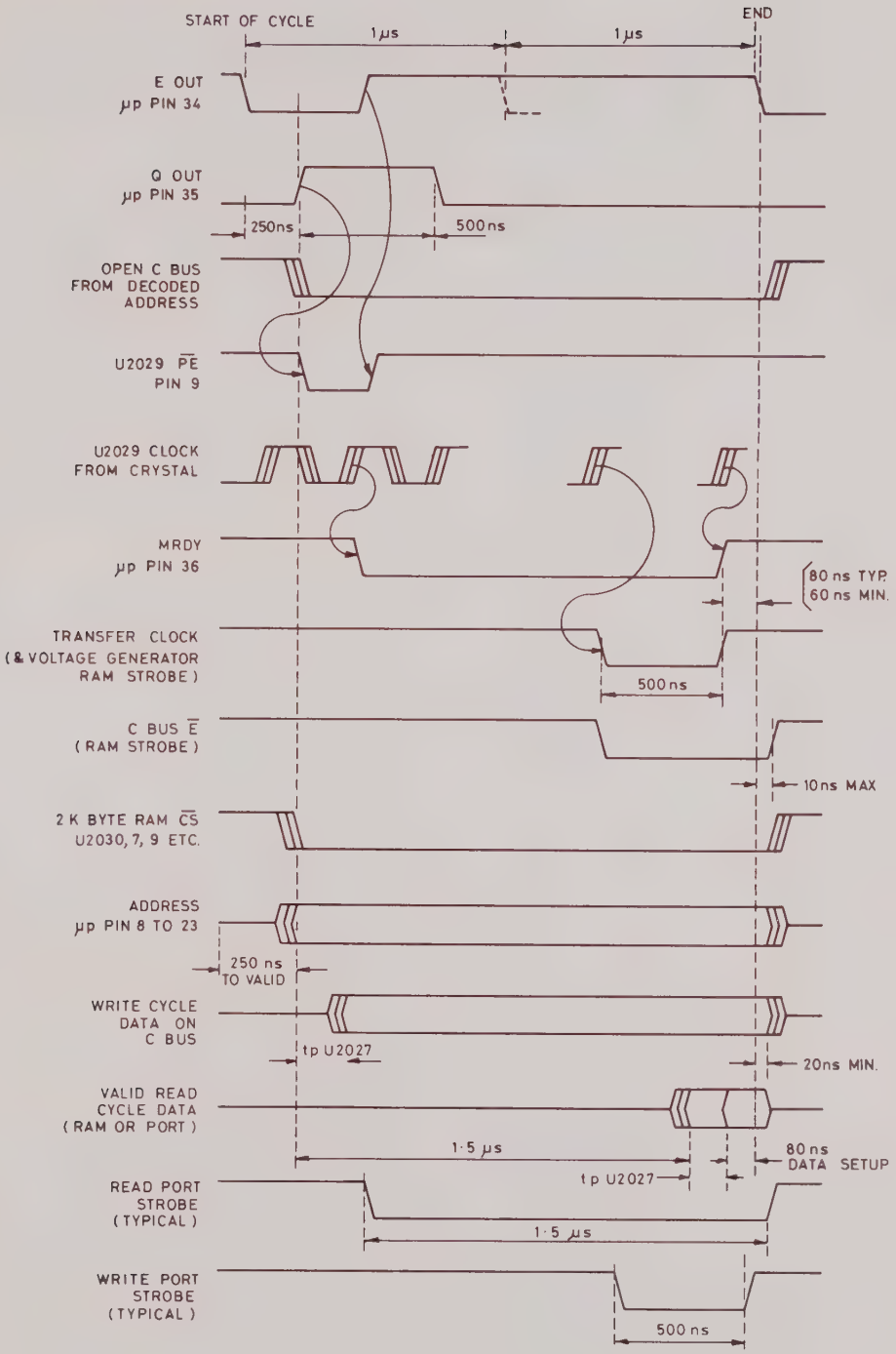


Fig. 4.15.3 Extended Cycle Timing Diagram

Hexadecimal Address	Device Location & Use		Primary Decode	
$FFFF				
$FFF2				Vectors
$E000	C.P.U.	U2001	U10 Pin 7	48k bytes FIRMWARE IN EPROM.
		U2002	U10 Pin 9	
$A000		U2003	U10 Pin 10	
		U2004	U10 Pin 11	
$8000		U2005	U10 Pin 12	
$6000		U2006	U10 Pin 13	
$4000	OPTION SPACE			
$2000	DATA DISPLAY	NUMERIC STORE	U30 Pin 7	C BUS ADDRESS RANGE
$1C00	ACQUISI-TION.	TRACE STORE 2	U30 Pin 9	
$1800	ACQUISI-TION.	TRACE STORE 1	U30 Pin 10	
$1400	ACQUISI-TION.	CURSOR STORE	U30 Pin 11	
$1000				
$0F8F	VOLT. GEN.	SCRATCH PAD		
$0F80				
$0F00		CONTROL PORTS READ PORTS		
$0C00				
		IEEE REGISTERS		
$0A00				
	C.P.U.	TTL DATA PORTS		
$0800	C.P.U.	NON VOLATILE RAM	U30 Pin 14 & Pin 15	
$0000				

Fig. 4.15.4 Address Map

60ns before the end of an extended cycle, and guarantees latching valid data before the end of the cycle, as address states remain stable for an unspecified time. Read only ports eg: U2050, are enabled whilst address decoding persists some 30ns after the end of the cycle.

Four, 1 kilobyte RAM blocks, on the data acquisition and display pcb's, use C BUS for data transfer to and from the microprocessor. Unqualified CS is provided to select these individual devices from U2030 pins 7,9,10 and 11.

In the "write to memory" mode, a long address and data propagation time is allowed, C BUS E being used to latch data into the addressed location. In "read", the RAM $\overline{CS}$ is used, giving an effective access time of 1.5μs before valid data is required on the bus.

The voltage generator scratchpad write only RAM uses transfer clock via U2031 pin 31, to latch data into local memory.

4.15.1.4 ADDRESS MAP

The 64 K bytes of directly addressable memory map is divided as shown in Fig. 4.15.4. All primary address decoding is performed on the CPU board. Further on decoding provides unique lines to read-only and write-only ports.

U2010 divides the map into 8 x 8 K byte segments, each equivalent to one EPROM U2001, 2002 etc: U2030 sub-divides the lowest 8 K bytes into 1 K byte sections. Four of these are taken to the edge connector for use by off-board RAM. The outputs for the bottom 2 K bytes, U2030 pins 14 and 15 are summed by U2015 b, and strobed by Eout providing a $\overline{CS}$, $\overline{OE}$ for the on board workspace RAM U2070. U2030 pin 12 enables another rank of decoders for the ports on CBUS.

Details of these port addresses are tabulated in the master index Fig. 5.6.2.

U2031 Pin 7 backplane 65 is used to address the voltage generator scratchpad which is a write only memory of 16 bytes.

Some ports on the microprocessor board use the T.T.L. data bus. The decoded address for these is provided by U2040. In read mode the address strobe to the ouput enable of buffers U2067 and U2068 (pins 1 & 19) is unconditional. In the write mode Pin 6 of U2040 is gated with Qout, causing data to be latched into U2049 etc. before the end of the cycle.

4.15.1.5 NON VOLATILE RAM (NVRAM)

U2070 provides 2 K bytes of RAM which retains data when the instrument is switched off. An on-board battery B2001, nominally 3.6 Volts supplies the very small current required (<10μA).

The chip select to the RAM must be high in the standby condition, and so that data integrity is maintained during power down/up an analogue gate U2072 is used to control the chip select (U2070 pin 18). The gate is enabled by U2011, which, during power on is clocked by system reset (Pin 11). Provided an $\overline{NMI}$ (ie: a low power condition) is not present, this D type latch will cause the output Q, Pin 1 to go high, enabling NVRAM. Power down causes an $\overline{NMI}$. Part of the service routine addresses $OC85 causing U2036 pin 10 to go low and the set of U2011 to go low, Q is reset disabling the analogue gate. This condition is irreversable without a power-on-reset or restart.

4.15.1.6 PROGRAMMABLE CLOCK DIVIDER CHAIN

The programmable clock utility is provided to enable the acquisition system sampling rate to be matched to time-base sweep speed.

Plot output rate is also set by using this facility. Various fixed frequency taps are used by the display hardware.

4MHz is derived from the crystal via transistor Q2020; U2018 e, a schmitt input device and U2018 b, converts this to TTL/CMOS Levels. This output then drives U2055 pin 1, the first in a chain of dual decade devices. U2055 pin 6 gives an output at 400KHz, pin 14 at 40KHz. Similarly U2056 divides U2055 output to provide 4KHz and 400Hz: U2057, 40Hz and 4Hz. These outputs are taken to individual inputs of an 8 way multiplexer U2053, which is controlled by U2052, a write only port at $OCF0. The output of U2053 on pin 14 is selectable as tabulated below.

INHIBIT	A	B	C	OUTPUT
1	X	X	X	TRI STATE
0	0	0	0	4Hz
0	1	0	0	40Hz
0	0	1	0	400Hz
0	1	1	0	4kHz
0	0	0	1	40kHz
0	1	0	1	400kHz
0	0	1	1	4MHz
0	1	1	1	Ext. Clock

X = Don't care.

Fig. 4.15.5 U2053 Output Programming

The output of U2053 is taken to the clock input of synchronous down counter U2054, the data inputs of which are taken to U2052, and hence the data presented to the preset inputs is under software control. An internally generated terminal count (at Zero) is available on pin 15 and goes low when enabled by CET low.

This $\overline{TC}$ output is connected to the parallel load ($\overline{PE}$) input (Pin 9). On the positive going transition of clock, data at the preset inputs is transferred to the counter outputs, if $\overline{PE}$ is low. The next clock will decrement the counter, provided terminal count is not loaded as the preset data. The counter will then take 'N' clock pulses where N = 2 to 15 to reach terminal count, giving an output and starting the

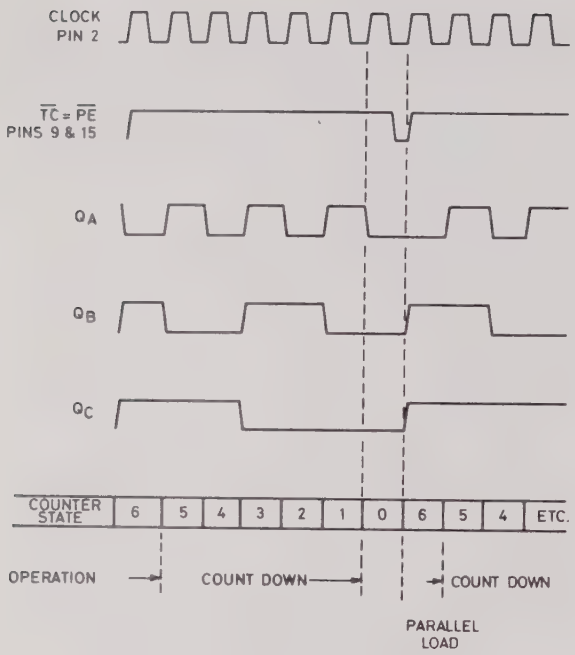


Fig. 4.15.6 U2054 Typical Waveforms

sequence again. In the special case where 0 (terminal count) is loaded as preset data the counter ÷ 1. This is because the clock applied to the CET input pin 7 causes $\overline{TC}$ to only go low.

4.16 CONTROL INTERFACE

4.16.1 CONTROL DATA BUS

Reference should be made to Fig. 6.13 (keypad circuit diag.) The Control Data Bus is used to enable the processor to read front panel control settings, and is controlled via circuitry situated on the keypad assembly.

The controls on this bus are: range and cal/uncal for CH1, CH2, TB A and TB B; data on/off and trace locate.

The Control Data Bus connects to the CH1 and CH2 switches via PLJK, to TB A and TB B switches via PLJJ and to data on/off and trace locate switches via PLJL.

Special monitor contacts form part of each switch assembly and may be 'addressed' individually by the processor via U1855 which is a 6 bit latch. At any instant only one output of Qo, Q1, Q3, Q4, Q5 may be high enabling one particular switch to drive the Control Data Bus, which may be read by the processor when U1854 is enabled.

For instance if CH1 attenuator range and uncal/status is to be determined, the processor will set U1855 pin 5 (Q1) high, allow a brief settling time of approx. 60μs and read the switch state via U1854 and CBUS (See Fig. 4.16.9). Assignments for Qo, Q1, Q3, Q4, Q5, of U1855 are shown in Fig. 4.16.1.

For each range switch diodes are included to ensure that changing one switch does not affect the code produced by another, see Fig. 4.16.2.

For the uncal bits however since the switches are single pole and must produce steady output to drive warning LEDs, U1862 (a transmission gate with active high control inputs) is employed to enable only one selected switch to affect the state of D7.

The codes produced by the various switches are shown in Fig. 4.16.3.

The processor examines all switch settings once every "regular" interrupt, i.e. every 25ms in the following order: Timebase A, Timebase B, Channel 1 attenuator, Channel 2 attenuator, Data on/off and trace Locate.

4.16.2 KEYPAD CIRCUITS

The keypad system consists of: a static (i.e. not scanned) key matrix; buffers to place matrix state on CBUS; interrupt control circuitry; software to debounce and validate keypad activities.

Qo	Timebase A range and uncal
Q5	Timebase B range and uncal
Q1	CH1 attenuator range and uncal
Q4	CH2 attenuator range and uncal
Q3	Data on/off and trace locate

Fig. 4.16.1: Switch Assignments for U1855 Outputs.

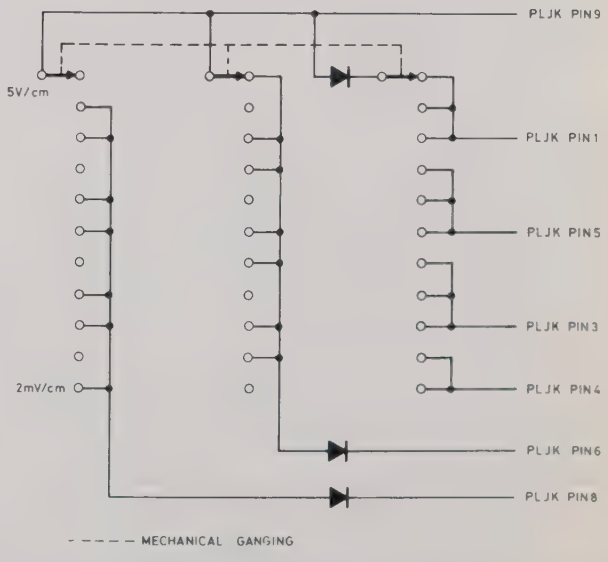


Fig. 4.16.2 Circuit schematic for CH1 attenuator range switch, with switch positioned at 5V/cm.

CONTROL	CONTROL POSITION	CONTROL DATA BUS LINES							
		D7	D6	D5	D4	D3	D2	D1	Do
Timebase 'A' range and uncal when U1855 pin 2 is high,	0.5 s/cm	1 = UNCAL	0	1	0	0	0	1	1
	0.2 "		1	0	0	0	0	1	1
	0.1 "		1	1	0	0	0	1	1
	50 ms/cm		0	1	0	0	1	0	1
Timebase 'B' range and uncal when U1855 pin 15 is high	20 "		1	0	0	0	1	0	1
	10 "		1	1	0	0	1	0	1
	5 "		0	1	0	1	0	0	1
	2 "		1	0	0	1	0	0	1
	1 "		1	1	0	1	0	0	1
	0.5 "		0	1	1	0	0	0	1
	0.2 "		1	0	1	0	0	0	0
	0.1 "		1	1	1	0	0	0	0
	50 μs/cm	0 = CAL	0	1	0	0	0	1	0
	20 "		1	0	0	0	0	1	0
	10 "		1	1	0	0	0	1	0
	5 "		0	1	0	0	1	0	0
	2 "		1	0	0	0	1	0	0
	1 "		1	1	0	0	1	0	0
	500ns/cm		0	1	0	1	0	0	0
	200 "		1	0	0	1	0	0	0
	100 "		1	1	0	1	0	0	0
	50 "		0	1	1	0	0	0	0
Channel 1 attenuator range and uncal when U1855 pin 5 is high	5 V/cm	1 = UNCAL	0	1	0	0	0	1	0
	2 "		1	0	0	0	0	1	0
	1 "		1	1	0	0	0	1	0
	0.5 "		0	1	0	0	1	0	0
	0.2 "		1	0	0	0	1	0	0
Channel 2 attenuator range and uncal when U1855 pin 12 is high	0.1 "		1	1	0	0	1	0	0
	50 mV/cm		0	1	0	1	0	0	0
	20 "		1	0	0	1	0	0	0
	10 "	0 = CAL	1	1	0	1	0	0	0
	5 "		0	1	1	0	0	0	0
	2 "		1	0	1	0	0	0	0
Trace locate and Data on/off when U1855 pin 10 is high.			0	0	0	0	0	1 = DATA OFF	1 = TRACE LOCATE

The processor examines all switch settings once every "regular" interrupt.

Fig. 4.16.3 Control Data Bus Truth Table

The controls included in the keypad matrix are the sixteen general purpose (soft) keys, the four cursor shift control keys, the two Y channel, and X shift control keys. Each pushbutton occupies a node in the keypad matrix, and when pressed applies +5V to the anodes of two diodes which in turn activate one of seven possible column bits and one of five possible row bits. The column and row words will appear on CBUS via read ports U1851 and U1852.

The keypad interrupt flip-flop, U1856b is clocked whenever a row line changes from low to high. The state of this flip-flop may be read by the processor via U1851, but whether an interrupt will actually be generated depends on the state of the keypad interrupt mask, formed by U1858b U1860b and under processor control via one line of write port U1855. If U1855 pin 7 is low the keypad may not interrupt the processor since U1858b is disabled forcing the keypad interrupt line (active high for interrupt) low. This is used to assist software in debouncing the keypad.

The keypad interrupt is cleared whenever U1851 is enabled i.e. whenever the column word is read by the processor. However, to allow the processor to read the state of the flip-flop directly (via U1851) the flip-flop is reset at the end of the read cycle, U1859c, C1855, R1855 and U1858c perform this function and timing is shown in Fig. 4.16.4.

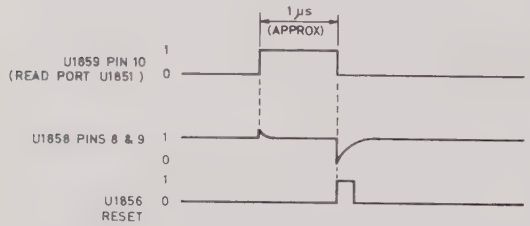


Fig. 4.16.4 Keypad Interrupt Reset Timing

Keypad validation is achieved with software which examines the state of the key matrix after a keypad interrupt.

As soon as the processor "sees" one column and one row bit high the key pressed is known and accepted.

It is necessary to debounce the keypad to distinguish between a bouncing key and multiple keypad entries on the same key. A bouncing key cannot produce an incorrect row/column code as if it were at a different matrix node, since both row and column words will have one bit set or a null on either row or column, or both. Thus the code is either illegal, or legal and correct for that key.

The processor examines the keypad every 25ms after a key has been pressed and will declare the key released when the row and column have been null for 50ms.

As the keypad lines are available to the processor unlatched, the latter may ascertain when a key held depressed for one of the keypad repeat functions.

4.16.3 SPINWHEEL CONTROL AND INTERFACE

The Spinwheel is a high resolution digital rotary control which may be used to vary one of the outputs of the Voltage General System (so that X or Y shift or cursor position may be changed) and to vary Delay System parameters.

The teeth of the spinwheel disc pass through the beams of two LED – phototransistor pairs as shown in Fig. 4.16.5 (Q1841, Q1842).

The optical paths are such that as one tooth edge just cuts one beam, the other beam is either in the middle of a tooth of middle of a gap.

Logic levels are obtained from the phototransistor outputs sharpened by U1858 a,d for presentation to the validation circuitry, which is shown in Fig. 4.16.6 with timing diagram in Fig. 4.16.7.

The function of the validation circuit is to interrupt the processor when the spinwheel has been moved and to give the state of the two beams at this time. Circuitry is required to generate this interrupt only when the spinwheel is seen to move two or more states in the same direction. This is to ensure that the processor is not continuously interrupted in the event of a tooth edge just cutting a beam with the spinwheel nominally stationary, but vibrated. (i.e. by fan, mains transformer etc.)

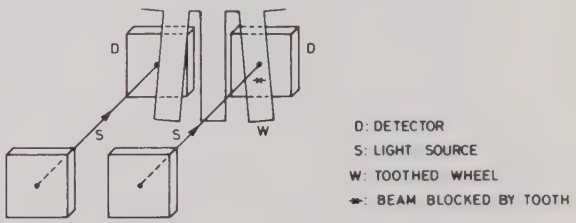


Fig. 4.16.5 Spinwheel Mechanics

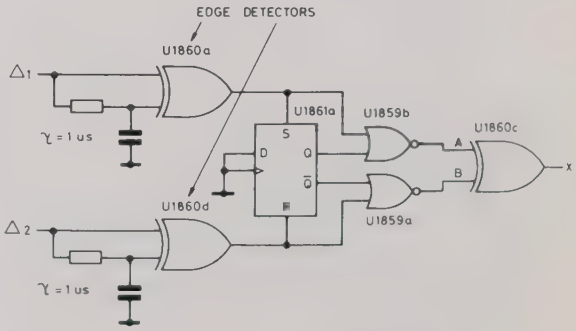


Fig. 4.16.6 Spinwheel Validator Credit

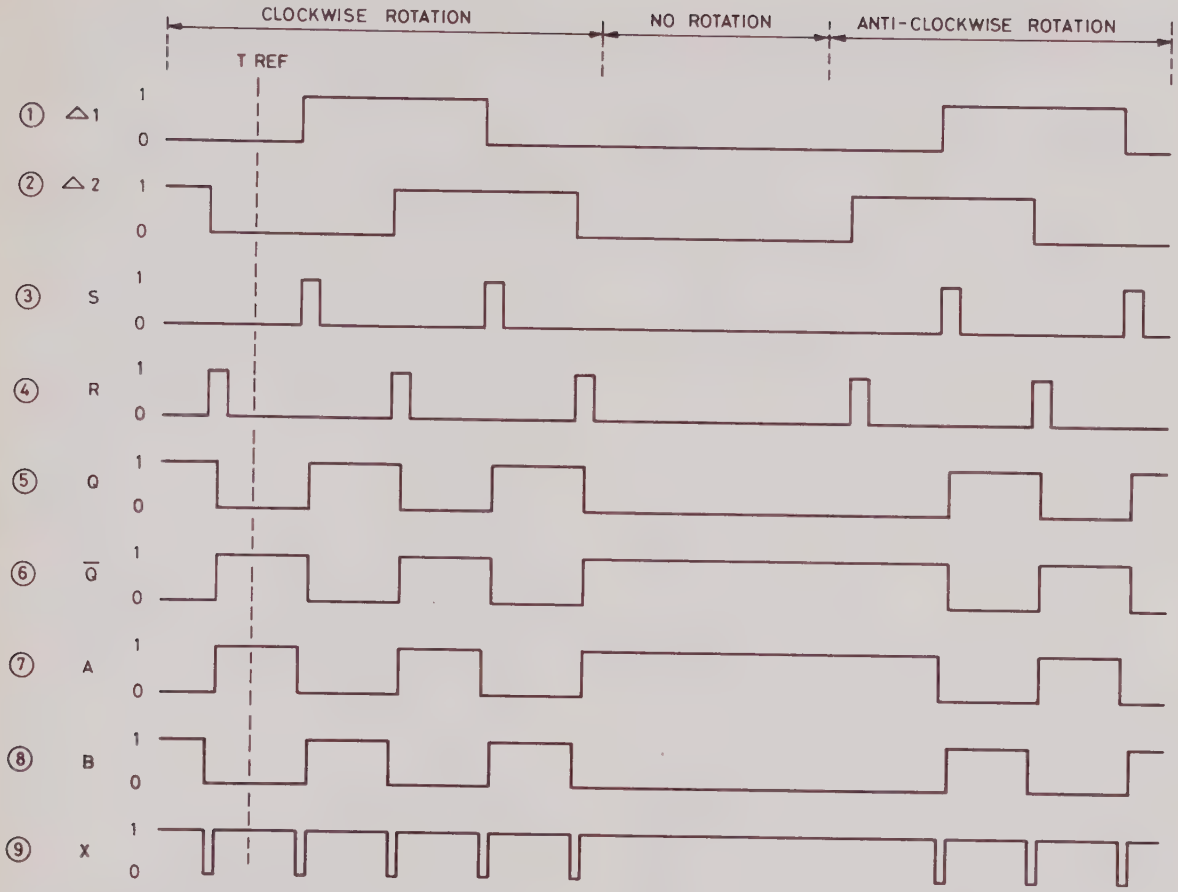


Fig. 4.16.7 Timing Diagram Spinwheel System

U1860a and U1860d produce a complete positive going pulse whenever Δ1 of Δ2 changes state, as shown in plots (3) and (4) of Fig. 4.16.7.

The timing diagram shows how the various logic levels change as the spinwheel is rotated clockwise, left stationary and then rotated anti-clockwise.

The flip-flop "remembers" whether Δ1 orΔ2 changed last. Starting at T ref. on Fig. 4.16.7, first Δ1 changes, Q becomes high which leaves A low. $\overline{Q}$ becomes low enabling the NOR gate U1859a. Δ2 then changes state causing B to go low and since A and B are both low at this instant X will go low. However A will change back high in response to Δ2 changing and a positive going edge is produced at X.

If the next phase to change is Δ2 again (for instance, as shown in Fig. 4.16.7 when anti-clockwise rotation first commences), no pulse appears at X since the flip-flop is waiting for a change on Δ1 and $\overline{Q}$ is high, disabling U1859a and enabling U1859b. Thus two edges are required.

The +ve edge at X (U1860 pin 10) is used to latch the spinwheel phase signals in U1857a,b following a change, and to generate the spinwheel interrupt via U1861b.

The processor may read the latched spinwheel phase by enabling read port U1852. This action automatically acknowledges the spinwheel interrupt by resetting U1861b via U1859d.

There follows a brief description of the software used to detect spinwheel direction.

As will be seen from Fig. 4.16.7 the spinwheel phase bits will change as shown in Fig. 4.16.8.

	Δ2	Δ1	
	0	0	↑
Sequence for clock-	0	1	Sequence for anti-
wise rotation	1	1	clockwise rotation
↓	1	0	

Fig. 4.16.8: Sequence of Spinwheel Bit Codes.

The software reads the spinwheel bit code on two successive interrupts. The entry in a table corresponding to Fig. 4.16.8 for the first code is found. If the next table entry matches the second code the spinwheel is declared to be rotating

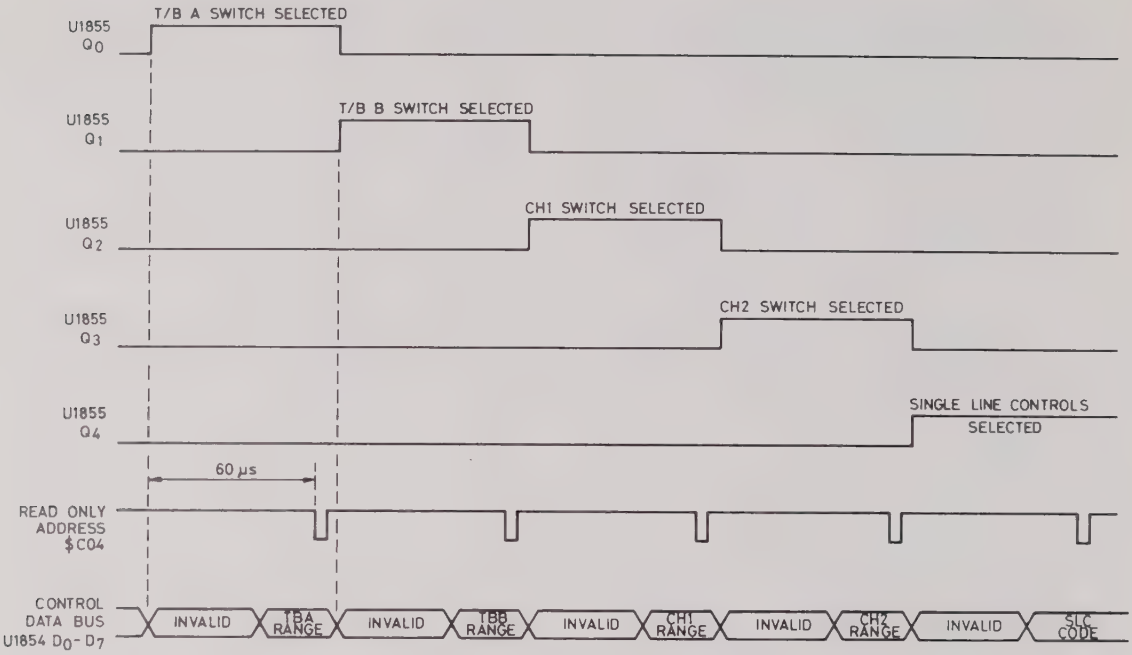


Fig. 4.16.9 Control Data Bus Timing (Typical)

clockwise. If, however, the second code matches the previous table entry the spinwheel must be rotating anti-clockwise. If, neither of these conditions exists then the software has detected an invalid sequence and no further action is taken. This sequence could occur after power – up or if the spinwheel is operated at excessive speed. In the latter case the processor assumes the direction has not been changed.

4.17 CALIBRATION FACILITIES

4.17.1 SOFTWARE VERTICAL CALIBRATION

4.17.1.1. GENERAL DESCRIPTION

The vertical measurement system consists of an 8 bit A.D.C. (analog to digital converter) and a 14 bit voltage generator for the calibrated shift system (see block diagram). Thus, a vertical shift can be added to the input signal, and the final voltage measured with the A.D.C. Since the shift voltage is known, the input signal voltage can be calculated and displayed on the screen.

The user also has the option of using a x10 probe on the input, and setting the 5110 to display the input voltage scaled by a factor of 10.

There are a number of hardware inaccuracies to be taken into account, in order to make best use of the resolution of the vertical measurement system:

1. A.D.C. gain may be inaccurately set up.
2. Y Shift gain may be inaccurately set up.
3. A voltage offset can occur in either system.
4. Another voltage offset may occur on selection of invert.
5. The gain of the x10 probes used can be inaccurate (because of resistance inaccuracies).

   In order for these inaccuracies not to affect measurements, they must be measured and taken into account.

By going through a procedure of inputting a sequence of accurately known voltages (see section 5.3.2 for detailed description of the procedure), each inaccuracy can be measured, and stored as a coefficient (in the non-voltaile RAM) to correct the final result.

The coefficients are in the range +127 to -128, representing roughly ±3% for the gain components, and roughly ±0.5cm for the offset component.

For each attenuator range there must be stored

1. An A.D.C. gain coefficient.
2. A Y shift gain coefficient.
3. An offset coefficient.

A single INVERT offset coefficient must be stored, which is applicable to all attenuator ranges.

For each of the four attenuator settings with different input resistors, there must be stored a x10 probe gain coefficient, for the probe being used.

(Obviously, if a new x10 probe is used, the x10 probe coefficients must be recalculated, or nominal values (i.e.

zero) selected. Therefore x10 probe calibration is a separate procedure, from main instrument calibration).

See Appendix 4.17.A for details of the calculation involved.

4.17.1.2 IMPLEMENTATION

A.D.C. gain is measured by inputting an accurately known 3cm signal, with Y shift set to zero, followed by a -3cm signal.

Comparing the measured A.D.C. readings, with the correct value gives the correction factor.

Y shift gain is measured by inputting an accurately known 6 or 7½cm signal, and automatically adjusting the Y shift position, until the A.D.C. reads zero; then inputting the inverse signal and again adjusting Y shift until A.D.C. = zero (mid scale).

The voltage offset is calculated from the difference between the two Y shift values.

Invert offset is measured by comparing the Y shift value for A.D.C. = zero when inverted with that when not inverted.

Because of the nature of the calculations, it is important that no external offsets are introduced, i.e. that the second input voltage is an accurate inverse of the first.

The x10 probe is calibrated in a similar way, by inputting a +10cm signal, via the x10 probe, and adjusting the Y shift for A.D.C. zero, then inputting its inverse (i.e. – 10cm) and again adjusting the Y shift for A.D.C. = zero.

The calculations do not require that the input signals be an exact number of cm or volts, only that they be accurately known. Thus, an input of roughly the right size can be used, if measured with a DVM, and the measured voltage entered via the keyboard of the instrument, for use in the calculation.

However as stated before, an accurate inverse of the first signal *is* required (e.g. by reversing the leads).

Because of the limited range of the coefficients, the hardware may need to be adjusted before a successful calibration can take place. To aid this, the individual coefficients are displayed on the screen as they are calculated, and any trends or borderline problems can be noted.

4.17.2 SOFTWARE HORIZONTAL CALIBRATION

4.17.2.1 GENERAL DESCRIPTION

The horizontal measurement system is based around 4 cursors, which can be moved across the trace.

A crystal counter can be allocated to measure the time from start of sweep to the current cursor. When the counter is not available (because it is being use elsewhere), the *calculated* position of the cursor is converted to a time value. In order to make best use of this, the individual cursor shift calibrated by comparison with the crystal counter. However each cursor, on each time base range can have slight gain and offset inaccuracies that would affect the resulting time reading.

A set of correction coefficients is stored (in non-volatile RAM) and is used to modify the nominal time reading for each cursor (based on it nominal position).

For details of the calculation used, see appendix 4.17.A.

The actual coefficients required are as follows:-

1. For each timebase range (and for both timebases) a cursor 2 gain coefficient and a cursor 2 offset coefficient are required.
2. Further, cursors, 1, 3 and 4 need a relative gain and offset coefficient (i.e. relative to cursor 2). These relative coefficients apply on all timebase ranges and only need be calculated on one suitable middle range.

The coefficients are in the range +127 to -128. For the gain coefficients, this corresponds to roughly ±3% gain inaccuracy. For the offset coefficients, it corresponds to roughly ± 1mm (or ± 10mm on x10 expansion), except on the four fastest timebase ranges, where offset range is expanded to ± 8mm (x1).

4.17.2.2 IMPLEMENTATION

On the first timebase range to be calibrated, cursor 2 coefficients are calculated and then the relative coefficients for the other cursors are calculated. On all other ranges, only cursor 2 coefficients are calculated and stored.

In practice, where possible, cursor 1 is used in place of cursor 2, for the actual measurement. The results are, however, used to produce cursor 2 coefficients by suitable conversion. Thus, when calibrating timebase A, all four cursors are calibrated on the first range and their respective coefficients stored. On all other ranges cursor 1 is used for the measurements. This has the consequence that the values displayed for cursor 1 on the screen, on the First range to be calibrated, are values relative to cursor 2 while on all other ranges the cursor 1 values are Absolute values.

When calibrating timebase B, cursor 1 is not available, so cursor 2 is used for all the absolute measurements.

The cursor is calibrated by positioning it a nominal 0.5 Divs from start of sweep, and measuring the time from start of sweep to that cursor, using the delay counter.

The cursor is then moved to a nominal 10.5 Divs from start of sweep and the delay counter is used to measure the actual delay again.

By substracting these two times and comparing them with the theoretical time, the gain correction coefficient can be obtained. By comparing the 0.5 div reading with the theoretical value, the offset correction coefficient is obtained. At the faster timebase ranges, more than one sweep is used to accumulate a sufficiently large count in the delay counter, for an accurate calculation.

50ns, on the 50ms/Div range, the delay counter is started and stopped 1000 times, before its final total value is read.

At	50ns/Div	1000	accumulations
	0.1μs/Div	100	"
	0.2μs/Div	100	"
	0.5μs/Div	100	"
	1μs/Div	10	"
	2μs/Div	10	"
	5μs/Div	10	"
	10μs/Div	1	sample

As a further problem, timebase start of sweep delays become appreciable on the top 3 or 4 timebase ranges. They are of the order of 15ns on timebase A, and 70ns timebase B. The calculations takes account of this, so the calibrated readings do not appear to have this offset.

Furthermore, on the top four timebase ranges (both timebase A and timebase B) the range of allowable offset is increased from ±1mm to ± 8mm, as mentioned above, to allow for the large effect of these delays.

Because of the limited range of the correction coefficients, the hardware may need to be adjusted before a successful software calibration can be completed. To aid this, each coefficient is displayed on the screen as it is calculated. Thus any trends or border-line problems can be noted.

4.17.3 D.A.C. VOLTAGE GENERATOR SELF-ADJUSTMENT

4.17.3.1 GENERAL DESCRIPTION

The voltage generator is a 14 bit D.A.C. (digital to analog converter) comprising two D.A.C.'s combined together, see block diag. Fig. 4.17.1 and section 4.14.

The two D.A.C.'s will be referred to as the major D.A.C. and the minor D.A.C., because one D.A.C. contributes the 8 most significant bits, while the other contributes the 6 least significant bits in between.

Thus the major D.A.C. takes 256 steps, between 0 and 255, and the minor D.A.C. takes 64 small steps for each one of the major D.A.C. (e.g. between 96 and 159). So the gaps between the major steps are filled in by the minor steps.

Because the minor D.A.C. is an 8 bit device, it has 256 steps available, and use is made of this range in removing non-linearity in the major D.A.C.

The major D.A.C. can have errors of ½ its l.s.b. These, unfortunately, correspond to ±32 l.s.b.s in the minor D.A.C. The resulting effect is shown in Fig. 4.17.2b. (heavy pecks). The solution may be inferred from this diagram. The minor D.A.C. can pick its range of 64 steps from a range of 192 (light pecks on Fig. 4.17.2b). One of these various start positions will be correct to bring the ramp back to its linear and monotonic position.

Apart from major D.A.C. non-linearities, there is the problem of setting up the two D.A.C.'s to match each other correctly, for gain (i.e. the major D.A.C. should have a gain exactly 64 times that of the minor). D.A.C. gain mismatch would have the effect shown in Fig. 4.17.2c.

Very minor gain errors can be taken out by the same method as before, but the processor must establish when the gain is correct.

The solution is for the 5110 to construct a table of 256 coefficients, one for each major D.A.C. step. These are stored and used as the start count for the minor D.A.C. table. e.g. table (162) is the coefficient for major D.A.C.

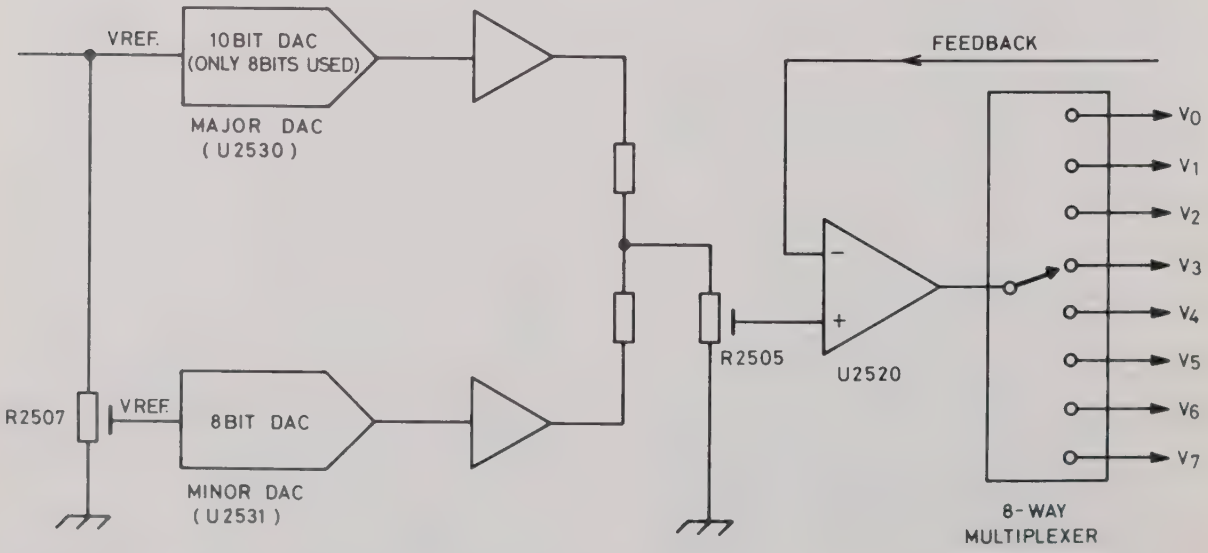


Fig. 4.17.1 Schematic of 14Bit D.A.C.

= 162. If table (162)= 37, then while major D.A.C.=162, the minor D.A.C. must travel between 37 and 101. The step above (major=162) + (minor=101) is (major=163) + (minor=table 163).

The table is calculated by using a precision comparator to adjust the D.A.C. output for montonicity by comparing two of the D.A.C.'s 8 outputs, V0 and V1. For each value N, of the major D.A.C., the minor D.A.C. is adjusted until the output is +½l.s.b. greater than the maximum D.A.C. value with major D.A.C. = N−1. For example to calculate table (163) as in the example above, one input to the comparator is major = 162, minor = 101).

The other input to the comparator is major = 163, and the minor is adjusted until the 2nd input is just greater than in 1st input. The comparator hardware is shown in block form in Fig. 4.17.3. Two similar voltage generator outputs, V0 and V1, are amplified in by a differential op. amp and compared. The output of the comparator is available to the microprocessor. To cancel out any system offsets, there is a preset potentiometer, RV2518, for manual adjustment, and a third voltage generator output V2 for automatic adjustment by the software. V2 is scaled down to be a very fine adjustment. In fact, it is roughly 64 times more sensitive than V0 or V1.

4.17.3.2 IMPLEMENTATION

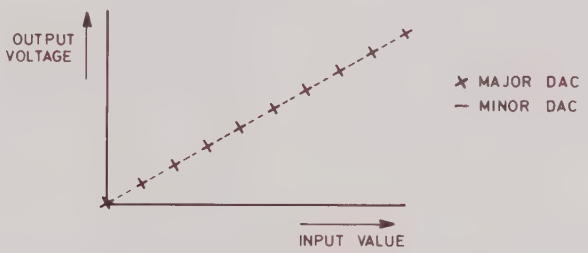
The user initiates the self adjustment by selecting General mode, option 81.

The first thing to happen is offset adjustment. With V0 = V1 = half scale, V2 is adjusted until the comparator indicates they are equal. The value of V2 is a measure of the offsets in the system, and is displayed on the screen as a number between +96 and -128, enabling RV2518 to be adjusted if necessary.

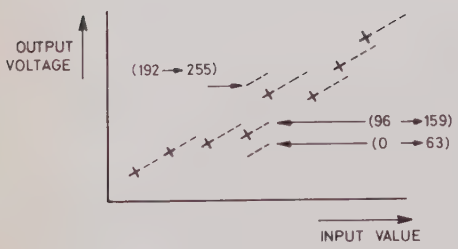
Then for each of N = O to N = 255, a value for table (N) is calculated, stored in table (N), and displayed via STORE 1, so that the contents of "table" appear on the screen for inspection. When all 256 coefficients have been calculated, the cycle starts again, so that hardware can be adjusted for optimum.

If at any stage, the sequence fails, because the hardware is not within range, nominal values of 96 are put into all succeeding table (N) entries, and the cycle restarts.

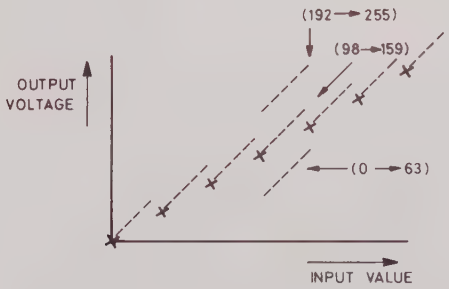
Fig. 4.17.2 Effects and Errors in Combining Major and Minor DACs



a) Theoretical Combination of Major & Minor DAC



b) Results of ± 1/2 Bit Non-Linearity in Major DAC



c) Result of Gain Mismatch Between Major & Minor DAC

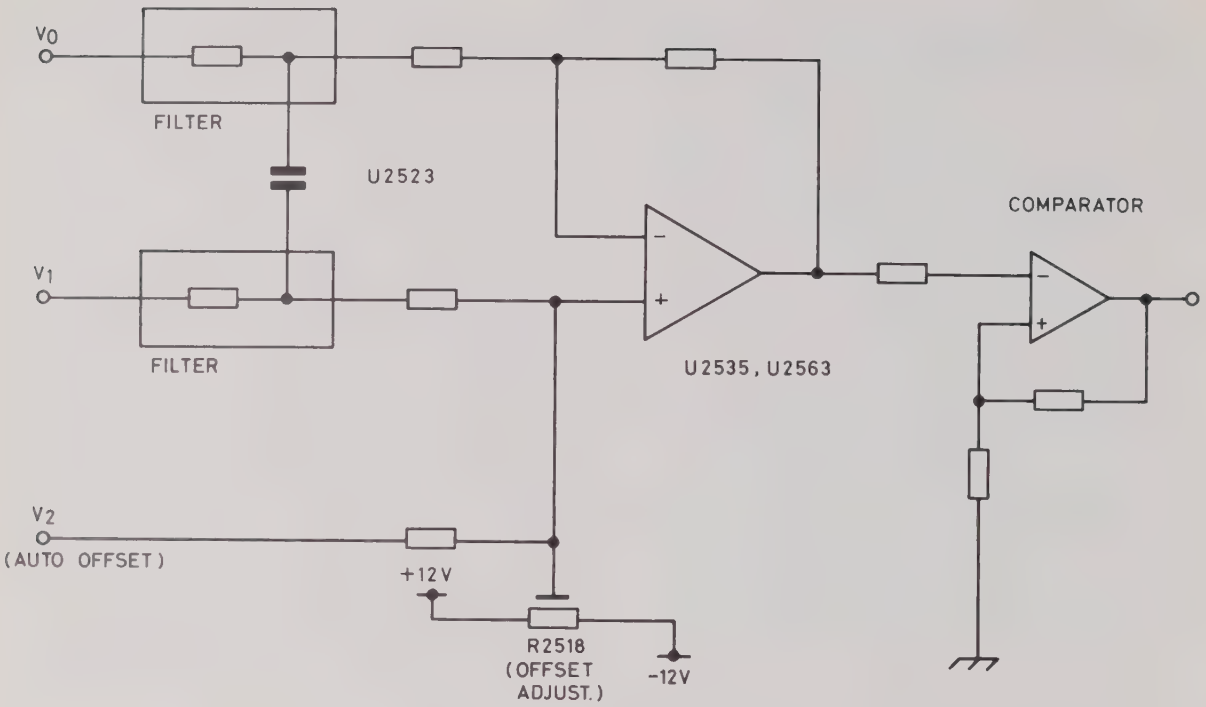


Fig. 4.17.3 Block Schematic of Precision Comparator

4.17.A APPENDIX A

Software calibration detailed equation

1. VERTICAL CALIBRATION

The equation used to calibrate the vertical readings to take account of hardware inaccuracies is:-

$Vin = (1 + \delta)(1 + \propto adc)\, Vadc - (Vyshift + \beta + j)(1 + \propto Yshift)(1 + \delta)$

where

Vin is actual input voltage
Vadc is actual ADC voltage
Vyshift is nominal Y shift voltage

and the coefficients, appropriately scaled are:-

$\propto$ adc is ADC gain correction
$\propto$ yshift is yshift gain correction

β is offset correction
j is invert offset correction
δ is probe gain correction, if applicable

(note that $\delta = 0$ if x1 probe is selected on Vertical menu, options 11 or 12)

2. HORIZONTAL CALIBRATION

The equation used to calibrate the horizontal readings to take account of hardware inaccuracies is:-

$T = (Tnom + \beta c2 + jc)(1 + \propto c2 + \gamma c)$

where

T is actual time from start of sweep to cursor
Tnom is nominal time based on nominal cursor position
βc2 is cursor2 offset correction coefficient
jc is (current cursor offset)-(cursor2 offset) coefficient
$\propto$ c2 is cursor2 gain coefficient
γ c is (current cursor gain)-(cursor2 gain) coefficient

4.17.4 VOLTAGE CALIBRATOR (SEE X OUTPUT AND CALIBRATOR CIRCUIT DIAGRAM)

A 1KHz 1V ± 1% squarewave is provided on the front panel as a means of calibrating the Y amplifier and compensating probes. A 1KHz 1mA signal is also available into a shorting link connected between the calibrator output and the earth terminal. The circuitry is mounted on the X Amplifier and Calibrator PCB and consists of an operational amplifier U1901 connected as a relaxation oscillator. When the output voltage from U1901 is low the current from the +12V supply through R1914 and R1905 passes through D1901 to the operational amplifier. On going high the amplifier output turns D1901 off and D1902 on. R1914, R1905, R1906 and R695 are now connected in series through D1902 between +12V and OV. R1914 is adjusted to give 1V across R695. C1903 limits the maximum slew rate of the output edges.

Refer to the waveform diagram Fig. 4.17.4. The voltage Vm is at the mean level of the output voltage Vo. If Vo is a squarewave with a 1:1 mark to space ratio swinging symetrically about OV Vm sits at OV. When Vc becomes equal to V_H in amplitude the oscillator changes state. The frequency of oscillation is thus determined by the hysteresis voltage V_H (Vo divided by the ratio of R1901 to R1903) and the rate at which C1902 is charged by the current Ic through R1904. Both V_H and Ic are directly proportional to Vo. As, however, the frequency of oscillation is inversely proportional to V_H and directly proportional to Ic it tends to be independent of the value of Vo. If Vo does not swing symmetrically about OV,Vm moves to sit at the mean level of Vo, V_H and therefore Vc giving symmetrically about this point. The charging current through R1904 is now equal on both half cycles of the squarewave and a 1:1 mark to space ratio is maintained.

4.17.5 TIME CALIBRATOR (SEE TRIGGER PREAMP CIRCUIT DIAGRAM)

A squarewave time calibrator is provided on the front panel. Its period can be programmed to lie between 40nsecs and 344 secs. This output is an AC coupled ECL signal swinging ±0.4V about OV derived from the Q output of U690b situated on the X Attenuator PCB. The SELECT TIME CAL I/P signal on pins 656 and 654 of this PCB consists of 10nsec pulses at twice the frequency of the Time Calibrator. This frequency is halved and a squarewave produced by the bistable U690b (see also Delay System section 4.6.).

4.18 GPIB SUB-SYSTEM

4.18.1 BLOCK DIAGRAM & GENERAL DESCRIPTION

The GPIB sub-system contains the interface between the microprocessor and the IEEE 488 bus, for connecting the instrument to an external controller. The IEEE 488 bus is a standard interface between instruments, that allows two way communication between them. For a description of the IEEE 488 bus, reference is made to that IEEE standard. Also contained on this assembly are five 2k x 8 bit RAMs and one 16k x 8 bit PROM for use by the microprocessor. Because of the processor's limited addressing range, this extra RAM and ROM is paged, so that several blocks of memory occupy the same address space. The processor differentiates between blocks by driving the hardware to select a different page.

As some of the RAM is used to store the eight pairs of machine state stores, its contents must not be lost when the instrument is turned off. For this reason the board contains a backup battery that gives the RAM sufficient power to maintain its contents until power is restored.

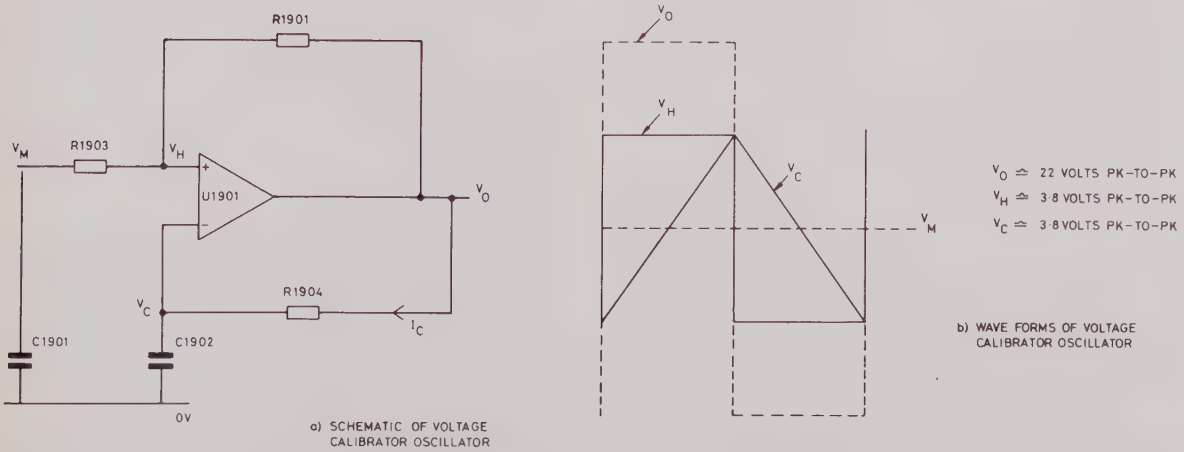
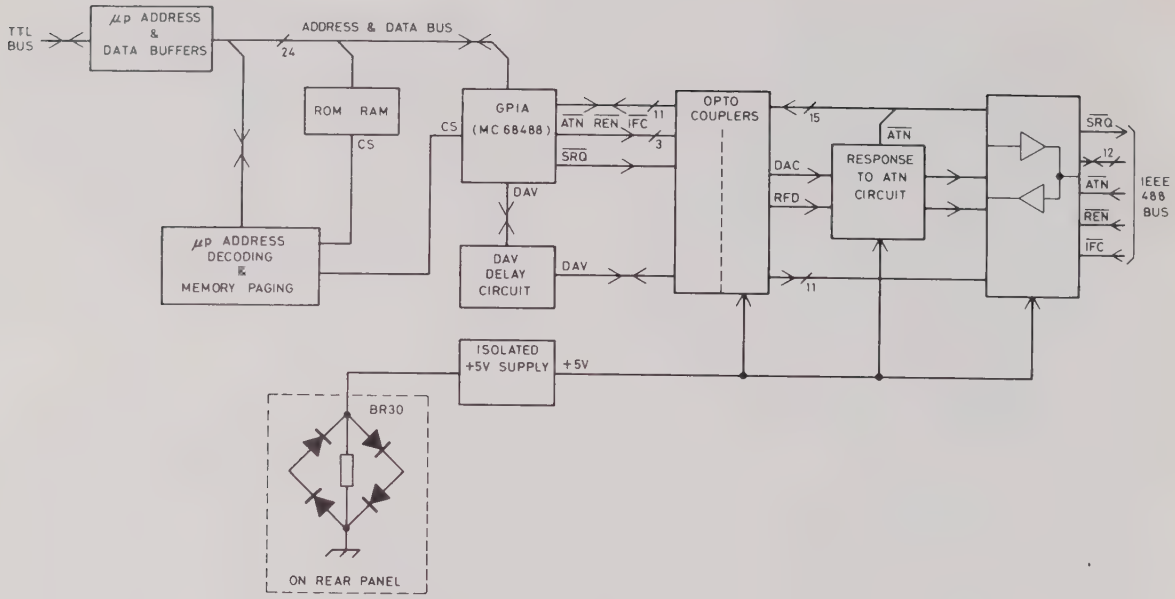


Fig. 4.17.4 Voltage Calibrator



GPIB Subsystem Block Diagram

The actual work of handling the interface between the microprocessor and the IEEE 488 bus is performed by the GPIA integrated circuit. This handles the data transfer, handshakes and interrupt generation.

To prevent problems due to multiple/noisy earth return paths, when the instrument is connected, via the IEEE 488 bus, to a distant controller and other instruments, the bus is isolated by a set of opto-couplers.

These opto-couplers cause their own problems, due to their slow response. It is therefore necessary to firstly, delay the Data Valid Line (DAV) until the data lines have settled, and secondly to make the handshake lines RFD and DAC respond immediately to an external attention signal (ATN). These circuits are explained in detail in sections 4.18.4 and 4.18.5.

4.18.2 ROM AND RAM ADDRESS DECODING AND PAGING

The Random Access Read/Write memory (RAM) on this board consists of five 2k x 8 bit CMOS packages U2953–U2957. The Read Only memory is a 16k x 8 bit EPROM package U2951. All five RAM packs occupy the same address space ($2000 to $27FF) The eprom is configured as two 8k by 8 bit segments, both occupying the same address space ($2000–$3FFF). For the microprocessor to select which of the numerous memories (all occupying the same address space) it requires, it writes to the four bit latch U2965. The outputs of U2965 are decoded into one of 6 lines by U2964 which in turn drive the chip select lines ($\overline{CS}$) of the RAM & ROM. Note that the chip select line of the RAMs (U2953–U2957 pin 18) are connected via analog switches (U2964a, U2950a, b, c, d). This is so that, in case of a power-down sequence, all the RAM is deselected, so its contents are preserved (though the RAM has a backup battery supply, as do U2946 & U2950, the rest of the circuit does not). The analog gates are driven by the 'external' line B13 from the processor.

A11 16 address lines from the processor AO to A15) are buffered (by U2967, 2968a and b). AO to A10 go to the address inputs of the RAM, and AO to A12 go to the address inputs of the EPROM (to address their contents). All to A15 are combined, via gates U2963a, U2966a, c, d and two-line, to 1-out-of-4 line decoder U2962a to give the four putputs Q0 to Q3 from U2962a. QO (U2962 pin 4) goes low for any address in the range $2000 to $27FF. Q1, Q2 and Q3 are combined together by U2961b to give the ROM CS line, (U2961 pin 8) which goes low for any address in the range $2000 to $3FFF. Inputs to U2961 (pins 9, 10, 12) decode all addresses from $2800 to $3FFF while pin 13 decodes address $2000 to $27FF, dependant on the value stored in the latch U2965.

The "IEEE ADDRESS" Line is an address decode line (from the CPU board) which goes low for any address between $0A00 and $OBFF. When combined with address line A8, by U2962b, two lines are produced, one of which, U2962 pin 12 (IEEE $\overline{CS}$) goes low for addresses between $OAOO and $0AFF and another, U2962 pin 11 ($OBxx) goes low for addresses between $0B00 and $0BFF.

All these various address decode lines are used to select the appropriate chip when the microprocessor addresses it, as shown in Fig. 4.18.1.

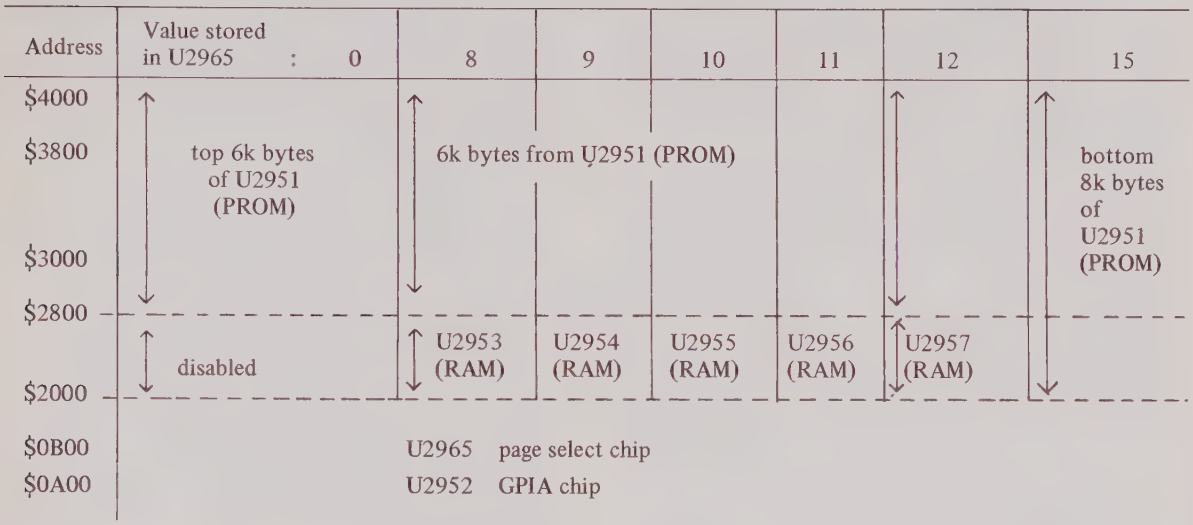


Fig. 4.18.1 I.E.E.E. Address Map

The other lines from the TTL bus are the data lines DO to D7, the READ/$\overline{\text{Write}}$ line, the Reset line, the IEEE interrupt line, and the μE out & $\overline{\mu\text{E}}$ out lines.

The data lines are buffered by the bidirectional, tristate buffer U2969. This is enabled (U2969 pin 19) only when a chip on the IEEE board is addressed. U2961a and U2963d combine the relevant address decode lines to put a low on U2969 pin 19 whenever a valid address is decoded. The direction of the buffers in U2969 is decided by the microprocessor read/$\overline{\text{write}}$ line, via U2966c.

The Read/$\overline{\text{Write}}$ line (B39 from the mother board), in addition to determining the direction for the data line buffer U2969, goes to the R/$\overline{\text{W}}$ line of U2952, and is combined with the clock $\overline{\mu\text{E OUT}}$ to drive the $\overline{\text{WE}}$ line of the RAM (U2953–57). Finally it ensures that U2965 is only addressed when the microprocessor is $\overline{\text{writing}}$ to it.

The IEE Interrupt signal, generated by the GPIA chip U2952 is sent to the CPU board via motherboard connection B95. The μEOUT & $\overline{\mu\text{EOUT}}$ lines have the normal functions of determining the timing of the bus accesses. The Reset line pulses low on power-up to reset the hardware (U2965, U2952).

4.18.3 GPIA CIRCUITRY & OPTO-COUPLERS

The interface between the microprocessor and the IEEE 488 bus is controlled by the GPIA chip. This is an LSI device that, in addition to performing IEEE 488 handshakes, generates interrupts to the microprocessor when required. Its function will not be described here.

On the microprocessor bus side it has the following signals, $\overline{\text{CS}}$, TRIG, CLK, IRQ, RESET,, R/$\overline{\text{W}}$, RSO–RS2, D0–D7. D0–D7 are bidirectional data lines, RSO–RS2 are address lines, $\overline{\text{CS}}$, CLK, IRQ, RESET, R/$\overline{\text{W}}$ have the usual microprocessor bus functions, and TRIG is an output (controlled by the IEEE 488 bus) to the timebase board, via U2947b and U2943j, that can act as a timebase trigger signal (it responds directly to the bus control function Group Execute Trigger).

On the IEEE 488 bus side are the following signals: ATN, $\overline{\text{IFC}}$, $\overline{\text{REN}}$, $\overline{\text{SRQ}}$, $\overline{\text{EOI}}$, $\overline{\text{DAV}}$, RFD, DAC, T/R1, T/R2, $\overline{\text{IBO}}$–$\overline{\text{IB7}}$. IBO–IB7 are bidirectional data lines, T/R1 and T/R2 are transmit/receive lines that control the direction of various buffers, $\overline{\text{DAV}}$, RFD & DAC are the handshake lines and $\overline{\text{ATN}}$, $\overline{\text{IFC}}$, $\overline{\text{REN}}$, $\overline{\text{SRQ}}$ & $\overline{\text{EOI}}$ are various IEEE 488 bus control lines.

All of these lines are separated from the IEEE bus by opto-couplers to prevent earth-loop problems (U2921–27, U2931–38). U2944 and U2945 are buffers to drive the data lines in the required direction (determined by T/R1). U2947a, c, d, e, g buffer the T/R1 & T/R2 lines. The bidirectional lines, $\overline{\text{DAV}}$, DAC, RFD and $\overline{\text{EOI}}$ are buffered in the direction from opto-couplers to U2952 by the buffers in U2942, as controlled by the transmit/receive control lines T/R1 and T/R2.

U2943, U2941b, U2941a, U2947h drive various lines in either direction. Note that the $\overline{\text{DAV}}$ (data valid) line is diverted through circuitry involving U2948 & U2949 – see section 4.18.4.

On the other side of the opto-couplers the lines are again buffered. U2914 buffers the outgoing data lines and U2904, U2903 & U2902 combine the data lines of both direction onto the IEEE bus (and also handshake lines DAC & RFD and control line $\overline{\text{EOI}}$. T/R1 & T/R2 control the direction of all the buffers.

U2901 buffers the final signals ($\overline{\text{ATN}}$, $\overline{\text{IFC}}$, $\overline{\text{REN}}$, & $\overline{\text{SRQ}}$). Note that the $\overline{\text{ATN}}$ signal combines with the outgoing DAC & RFD lines in the Response to ATN circuit – see section 4.18.5.

4.18.4 DAV DELAY CIRCUIT

Because of the signal delay through the opto-couplers the "data valid" signal in both directions must be delayed until it is certain that all opto-coupler outputs have settled. This is done by the monostable circuits based around U2948 and U2949. The circuits are very similar and work on the DAV signals in either direction to delay that signal by, typically, 70μs.

As both monostables are similar, only one will be described.

A positive edge on the clock input (U2948 pin 11), signifying DAV is true produces a negative pulse of duration 70μs on the Q output, U2948 pin 12. The action of this type of monostable is as described in section 4.6.2. The trailing edge of this pulse clocks the following bistable (U2948 pin 3) and the output from pin 1 is a delayed version of the DAV input. When DAV goes false the set line (U2948 pin 6) goes high and the output follows DAV immediately (see fig. 4.18.2).

4.18.5 RESPONSE TO $\overline{\text{ATN}}$ CIRCUIT

The IEEE 488 bus requires a very fast response from the instrument to a controller asserting attention ($\overline{\text{ATN}}$). The slow response time of the opto-couplers makes it necessary to include an additional circuit with a faster response. This circuit has the function of pulling false (i.e. LOW) the outgoing data-accepted and ready-for-data handshake lines (DAC & RFD), until the handshake lines have responded through the opto-couplers.

Whenever the $\overline{\text{ATN}}$ line from the bus changes state, a narrow pulse is produced at the output of the exclusive OR gate U2912b. This clocks the flip-flop U2911a, and its $\overline{\text{Q}}$ output pin 6 goes low for about 50μs, until U2915c resets U2911a.

The negative $\overline{\text{Q}}$ output pulse disables the AND gates U2916a & b, forcing their outputs, DAC and RFD, low for that time. After that time, control of the lines is returned to the GPIA chip U2952. Note that for quicker response to $\overline{\text{ATN}}$ going HIGH, the opto-coupler U2932 has a cascode type output, using Q2901. (Because turning off the opto-coupler is slower than turning it on, speedup is only required in the one direction). See Fig. 4.18.3 for timing diagram.

Because of the poor rise-time of the opto-couplers, the buffers that follow then include hysteresis to speed up their edges.

4.18.6 POWER SUPPLY AND BACKUP BATTERY

This assembly has four power supplies. Firstly +5V & -5V comes already regulated from the motherboard. Secondly, an unregulated positive supply from the motherboard is converted to +5V regulated supply by U2960 & C2960, C2953 to supply the five RAM chips. Finally, an isolated winding from the transformer is used to generate an isolated +5V supply for use by the IEEE 488 bus circuitry on the far side of the opto-isolators. Diodes D2901–04 rectify the supply, which is smoothed by C2907–09 and regulated by U2905 with C2905.

The isolation is not total, as this IEEE earth is in fact connected to the main instrument chassis by the circuit of diodes and a resistor shown in the block diagram Fig. 4.18.1. This is for reasons of safety.

In addition to these supplies, the RAM is supplied with a back-up voltage by the battery B2901. Diode D2951 prevents reverse voltages which would damage the regulator U2960. When the power is on, the battery is trickle-charged from the +5V supply through R2958.

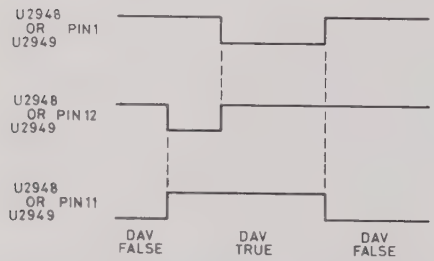


Fig. 4.18.2 DAV Delay Timing Diagram

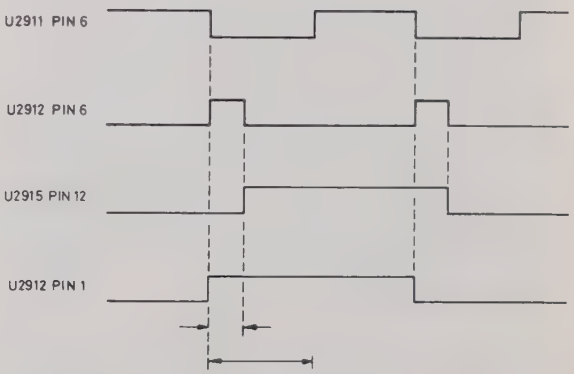


Fig. 18.3 Response to $\overline{\text{ATN}}$ Timing Diagram

5.1 GENERAL

The instrument is protected electrically by 4 fuses.

1. FS1, mounted in a holder on the rear panel, is in the incoming supply line. This is a 1¼" slow blow type. A 2A rating (part number 452193) is required for the 220/240V range of 4A rating (part number 452194) for the 100/120V ranges.
2. FS1050, mounted on the power supply PCB behind the moulded plastic cover, protects the +60V and +120V supplies. It is a 20 x 5mm slow blow type (part number 33685) with a 500mA rating.
3. The +5V supply is protected by a 10A 1¼" fuse FS10 (part number 12991) mounted on the capacitor support bracket at the side of the instrument (see fig. 5.2.1).
4. The instrument is thermally protected against overheating should say, the fan stop, by thermal fuse FTH1 set to open at 75°C.

The following sections give information on obtaining acess to all internal controls and removal of the various printed boards and assemblies as may be necessary during servicing.

If, during servicing, a component needs replacing, it is recommended that it is carefully desoldered using either a vacuum desoldering pump or desolder braid, taking care not to damage the delicate copper track. It will often assist removal if the component is first cut away leaving as much of the leads as possible connected to the PCB enabling the leads to be removed independently.

If a fault cannot be cleared it is recommended that the instrument be returned to the manufacturer for repair. When faults have been cleared, it is advisable for at least those parts that have been repaired to be recalibrated to ensure that the instrument conforms to specification.

5.2 MECHANICAL ASSEMBLY

GENERAL

Figures 5.2.1 to 5.2.8 illustrate the internal layout of the instrument and access to the various controls. Figures 5.2.9 to 5.2.18 show the position of the controls and connectors on the major boards as seen from the component side, with the exception of the X output board which is usually seen from the solder side.

WARNING: HIGH VOLTAGES ARE EXPOSED WHEN THE COVERS ARE REMOVED AND THE INSTRUMENT MUST ONLY BE WORKED ON BY SUITABLY QUALIFIED PERSONNEL.

5.2.1 TO REMOVE THE Y PRE-AMP

Disconnect instrument from supply and remove top and bottom covers.

Prise off knob caps, and remove knobs/screws from VOLTS/DIV UNCAL and attenuator switches.
Remove retaining nuts from attenuator switches.
Carefully unsolder delay line leads from pins 501,2,3.
Noting the order of leads.

HANDLE DELAY LINE BY OUTER COVER ONLY.
AVOID UNDUE FLEXURE OF TERMINATIONS.

Unsolder composite trig co-ax from pins 504, 5.
Remove trig view lead, PLGG.
Remove 3 screws from PCB, 2 at rear corners, 1 halfway back on card frame side. (labelled 'A' on Fig. 5.2.2).
Ease preamp backwards and downwards until plugs on trackside of PCB are accessible.
Remove remaining plug leads, noting their positions.
Unsolder trig coax leads from trig pre-amp board (rear of attenuator switches).

Re-fit by reversing removal procedure. When fitting the header leads to SKM and SKN support the rear of daughter boards to avoid damaging solder pin connections to mother board. It is helpful to attach a loop of string to the lead from PLNN before inserting pre-amp.

5.2.2 ACCESS TO Y OUTPUT & SAMPLING PCB

WARNING: HIGH VOLTAGES EXIST ON THIS PCB.

For fault diagnosis it is possible to operate the PCB whilst removed from the instrument. In which case only the three connections between the Y Output PCB and the Y Output Module (one wire and two resistors) need to be removed. For complete removal all connections should be removed.

Access to many components may be obtained by prising off the rear left-hand side cheek with a screwdriver in the slot provided. (See Fig. 5.2.3).

To remove the complete assembly from the instrument first remove the Intensity, Focus and Scale knobs by prising off caps and removing screws/nuts as necessary. Next remove the mains on/off switch by undoing the countersunk screw in the top of the front panel shown in Fig. 5.2.1 and the screw securing the bracket to the PCB. Remove the screws securing the PCB to the X Output assembly, and to the Y Output module bracket. (labelled 'B' in Fig. 5.2.3).

The whole assembly may now be removed by sliding backwards and lifting the rear end out first.

To operate the assembly for fault diagnosis the front mains on/off switch should be refitted with the front panel screw only and the assembly secured with a screw mounted through the central rear PCB hole into the X Output amplifier.

5.2.3 TIMEBASE

1. Remove Card Frame as detailed in section 5.2.13.
2. Remove all accessible sockets from the front of the Timebase PCB and unsolder the co-axial cable from pins 1402 and 1401.
3. Remove the three screws at the top of the PCB.
4. Lift the top of the board forward from under the centre bar.
5. Ease the board upwards releasing the bottom of the board from the plastic holding clips.
6. Carefully continue to lift the board upwards unplugging sockets CB, CD, BX and BY as they become accessible.
7. The PCB can now be completely withdrawn from the instrument.

8. This PCB can be replaced by reversing the above procedure.

The timebase can be operated external to the instrument for test purposes as shown in Fig. 5.2.5. The board is held between a front and rear Card Supports (Gould Part Nos. 452351 and 452352 respectively) mounted by screws inserted into the rear of the end pillars on the centre bar.

1. Carry out the procedure for the removal of the Timebase. As PCB is not being completely withdrawn it should not be necessary to unsolder the co-axial cable or unplug sockets. Ease must be taken however to avoid placing undue stress on sockets or cables.
2. When the timebase has been lifted out sufficiently it can be moved between the lead supports and clamped as shown in Fig. 5.2.5.

5.2.4 X OUTPUT & CALIBRATOR

1. Remove the four screws and washers in the four corners of the X Output and Calibrator PCB. (labelled 'F' in Fig. 5.2.1).
2. Through the slot in the PCB remove the two X Output connectors from the side-pins of the c.r.t.
3. Raising the PCB sufficiently unplug socket BN from the component side.
4. Raising the PCB further unplug sockets AA, W, Y, G, AB, Z and CR.
5. Unsolder lead to pin 1901.
6. Unsolder co-axial leads from pins 1902, 1903, X4 and X5.
7. Unplug sockets AF and AR from the Tube Base PCB.
8. The X Output and Calibrator can now be withdrawn from the instrument.

5.2.5 ACCESS TO TRIGGER AMPLIFIER ASSEMBLY

'A' & 'B' external trigger attenuator compensation components are freely accessible from the bottom of the instrument.

Access to 'A' and 'B' trigger level centre presets is from the right hand side of the instrument below the side bar.

Access to the X-Y calibration preset is from the right hand side of the instrument, but it is necessary to first remove the front side cheek with a screwdriver placed in the slot provided.

Many components are accessible for fault diagnosis and servicing with the Trigger Amplifier installed in the 5110 frame.

Where it is necessary to remove the complete Trigger Assembly, the card frame must be removed first. See section 5.2.13. Then remove the control knobs listed below by prising off caps and removing screws or nuts as necessary.

Contrast
Trace Separate
A timebase uncal and range
B timebase uncal and range
A trigger level
B trigger level
Hold-Off

Remove the screw securing the earth braid to the right hand side bar, and unsolder the two trigger output coax cables. Also pull off multi-way connectors PLAJ and PLBM from the Trigger Assembly and PLJJ from the Keypad Assembly.

The Trigger Assembly is secured to the front panel by the earth pillar and two screws. The earth pillar should be unscrewed by inserting a small bar in wire hole. The two screws are located at the top next to the Contrast and Trace Separate controls.

5.2.6 ACCESS TO KEYPAD ASSEMBLY

Access to some components is possible at the top of the instrument, but in general it will be necessary to remove the card frame first – see section 5.2.13 for full details.

With the card frame removed, access is possible to all components on the Keypad Daughter PCB. For access to the Keypad Mother PCB and Keypad Encoder PCB it is necessary to remove the keypad Assembly from the 5110 frame.

If it is necessary to fault-find the assembly with the instrument running, the assembly should be removed from the instrument and the card frame replaced. Trouble-shooting the keypad and spinwheel circuitry is possible by re-connecting the keypad to the card frame only. However, extension leads for PLJJ, PLJK, PLJL, PLKK, PLKL will be required for diagnosis of faults in other functions.

To remove the keypad Assembly, first remove connectors PLJJ, PLJK, PLJL (Daughter PCB).

Now remove the shift control knob (remove push-fit cap and undo nut).

Four screws retain the keypad to the front panel and must be removed. Two of these screws are positioned at the top of the keypad Mother PCB on either side of the central hexagonal pillar. The remaining two screws are positioned at the bottom of the keypad Mother PCB on either side of the Spinwheel mounting bracket.

The connectors PLKK, PLKL may be removed as the assembly is withdrawn.

Refitting is a reversal of the above procedure.

5.2.7 CATHODE RAY TUBE

1. Remove X Output and Calibrator PCB as detailed in Section 5.2.4.
2. Unsolder the capacitors between the c.r.t. side-connectors and the tube-shield. Remove all side connectors from the c.r.t. marking all leads to assist with replacement. Socket BN can now be removed.
3. Remove the E.H.T. oscillator top-screen, remove the final anode socket from the top of the multiplier and discharge the final anode and multiplier as in section.

   WARNING: BEWARE HIGH VOLTAGES.
4. Unsolder the earth screen lead for the final anode from pin 1001.

5. Unsolder the braiding between the Y Output Module and the tube shield.
6. Remove SKK from Y Output and Driver PCB. As this socket is reversible care must be taken to insert it in its present direction on reassembly.
7. Remove sockets, AH, AG, AS, AP and CM from Tube Base PCB.
8. Remove graticule illumination bulbs from the c.r.t. support moulding at the front of the instrument.
9. Unclip the delay line from the two mounting clips on top of the c.r.t. shield.
10. Inlatch the PCB supports at the bottom of the Tube Base PCB
11. Remove the two screws securing the rear of the c.r.t. shield to its mounting bracket.
12. Unclip and remove the bezel from the front of the instrument.
13. Carefully supporting the front of the c.r.t. remove the four screws from the c.r.t. support moulding.
14. The c.r.t. can now be slid towards the rear of the instrument and when clear of the front panel surround, lifted out.
15. Remove the support moulding and filter from the face of the c.r.t.
16. Remove the c.r.t. socket.
17. Unsolder the earth braid between rear of Tube Base PCB and tube shield.
18. Loosen the two hex head screws on either side of the tube-shield neck which clamp the rear tube support moulding.
19. The tube base PCB can now be removed from the tube-shield neck.
20. Carefully withdraw the c.r.t. forward from the shield. The leads to SKK and the E.H.T. cable are to be passed through their associated grommets in the shield. It will be necessary to remove the EHT cap and the contact inserts from the plastic housing of SKK in order to completely withdraw the cables through the grommets.
21. Take care not to damage the c.r.t. side pins. Do not knock or stress the shield as this can damage its magnetic properties.
22. The c.r.t. is replaced by reversing the above procedure but clamp the rear tube support moulding after the c.r.t. has been pushed forward in the shield to meet the front panel moulding. Ensure that the Tube Base PCB is mounted vertically before tightening the clamp.
23. WARNING: Although the danger of implosion with this type of c.r.t. is slight, great caution should nevertheless be used when handling the c.r.t. It is advisable to wear protective clothing in particular some form of suitable eye protection.

5.2.8 TUBE-BASE PCB

1. In order to remove the Tube Base PCB follow instructions 1 to 19 for the removal of the cathode ray tube.

5.2.9 CATHODE RAY TUBE, TUBE BASE PCB AND X OUTPUT & CALIBRATOR AS A COMPLETE ASSEMBLY

To facilitate test, the Cathode Ray Tube, Tube Base PCB and X output and Calibrator PCB can be removed from the instrument and mounted as a running assembly.

1. Remove graticule illumination bulbs from the c.r.t. support moulding at the front of the instrument.
2. Unclip the delay line from the two mounting clips on top of the c.r.t. shield.
3. Unlatch the PCB supports at the bottom of the Tube Base PCB.
4. Remove the four screws in the four corners of the X output and Calibrator PCB.
5. Through the slot in the PCB remove the two X Output connectors from the side pins of the c.r.t.
6. Raising the PCB sufficiently unplug socket BN from the component side.
7. Raising the PCB further unsolder the earth braiding between the Y Output Module and the tube shield.
8. Remove the Y Output connectors to the c.r.t. side-pins.
9. Remove the two screws securing the rear of the c.r.t. shield to its mounting bracket.
10. Unclip and remove the bezel from the front of the instrument.
11. Carefully supporting the front of the c.r.t. remove the four screws from the c.r.t. support moulding.
12. The c.r.t. can now be slid towards the rear of this instrument and when clear of the front panel surround lifted straight up.
13. When the c.r.t. has been raised sufficiently, move it forward until the bottom of the c.r.t. support moulding is resting on the front panel surround.
14. Slip a Test Jig Mounting Bracket (Gould Part No. under the mounting lugs on rear of tube shield as shown in Fig. 5.2.5. The long leg of the mounting bracket is supported in the slot of the side-bar with the other end of the jig clipped over the centre bar.
15. Screw the tube shield to Test Jig Mounting Bracket.
16. Reinsert socket BN.
17. Lower PCB and replace the two screws between it and the Tube Base PCB.
18. Return the X Output connectors to the c.r.t. side-pins.
19. After extending the Y Output leads sufficiently plug them into the c.r.t. Y side-pins.
20. The instrument can now be run.
    WARNING: Beware of high voltages on the exposed rear of the Tube Base PCB.
21. To replace the assembly reverse the above procedure.

5.2.10 PHYSICAL ACCESS TO POWER SUPPLY

Most components are under a false rear panel.
Exceptions are:- FS10 (+5V Fuse),
All large smoothing capacitors, C1, C10, C11, C20, C30 & C52 Diodes D1 & D2, (+5V).
Access to these can be obtained by removal of the instrument top cover.

TO EXPOSE OTHER COMPONENTS – REFER TO FIG. 5.2.6.

1. Remove mains input cable from rear socket.
2. Remove four push-fit feet. Ⓐ
3. With No. 1 crosspoint screwdriver remove 7 x 3mm Ⓑ screws – four are hidden under feet.
4. Remove panel.
   NOTE: Fuse FS1050 is now accessible.
5. Fig. 5.2.6b Remove 4, 12 x 3mm crosspoint screws to Ⓔ release heatsink from rear panel.
6. Unplug cableform from PLC
   Lower assy. to place heatsink on bench.
7. To free PCB from main heatsink the 8 x 3mm screws Ⓒ must be removed.
   It is important that the sidebars remain attached to the PCB so that regulators etc. are not stressed.
8. For fault finding the power supply in this condition.

   WARNING:
   THE THERMAL SWITCH HAS MAINS VOLTAGE ON THE TWO SLEEVED TERMINALS.

   1. Replace PLC.
   2. Support main heatsink away from PCB
   3. Insert mains input.

   Care should be taken to monitor both sidebars Ⓖ and Ⓗ : Do not allow excessive temperature.
9. To expose the rear of PCB release insulation material by undoing 2 screws Ⓓ . These should be replaced if the assembly is to be handled.
10. Replacement is a strict reversal of the above. Ensure that all plugs are firmly in place before rear panel is positioned.

5.2.11 ACCESS TO EHT

1. Remove instrument bottom cover.
2. Remove two 6 x 3mm crosspoint screws holding EHT cover to EHT box sides.

   WARNING: THIS EXPOSES DANGEROUSLY HIGH VOLTAGE.

3. PCB is held into housing by four 10 x 3mm screws. (A) in Fig. 5.2.8.
4. Removal of multiplier.
   This requires safe discharge of the P.D.A. voltage (16kV) and is best accomplished in the following manner.
   a) Tape a high value resistor to the blade of a well insulated screwdriver (solder further resistors in series to give 10MΩ at 16kV).
   b) Solder one end of resistor chain to earth; (E)
   c) Holding the insulated handle of screwdriver, carefully push the other end of resistor chain under P.D.A. cap multiplier may now be further discharged with a multimeter to ensure complete discharge. Multiplier unit may be removed when two 4mm nuts are unscrewed (B).

REFITTING

This is a simple reversal of the above; however

Note 1. Cleanliness is essential around the P.D.A. area otherwise tracking may occur.

Note 2. EHT cover has cut outs to give clearance for pillars supporting tubebase board.

5.2.12 ACCESS TO POD INTERFACE PCB

The Pod Interface PCB is located at the rear of the instrument adjacent to the cooling fan. It is secured to the right-hand sidebar by two screws.

To remove the Pod Interface PCB, first remove the 20 way DIL header from the bottom of the PCB (connects to front panel Data Input socket). Next remove the rear (long) right-hand side cheek by inserting a screwdriver in the slot provided and levering off. The two screws may then be unscrewed from the hank bushes mounted in the PCB and the PCB withdrawn from the instrument. (shown as hidden detail, labelled 'E' in Fig. 5.2.4).

If required the PCB may be operated outside the instrument simply by reconnecting the 20 way Data Input header.

5.2.13 TO REMOVE THE CARD FRAME

Disconnect instrument from supply, and remove top and bottom covers.

Raise each PCB in turn and unplug leads, keeping careful note of the mounting of leads.
Unplug keypad lead from bottom front of card frame, and power supply lead from bottom rear.
Remove 6 screws holding card frame to angle brackets (labelled 'C' on Fig. 5.2.4), leaving angle brackets bolted to mainframe side bar. Note earth braids on front 2 screws. Hold right-hand side of handle out slightly, and lift out card frame.

To re-fit card frame reverse the procedure for removal, taking care that leads are routed as before. Check that no leads become trapped under the bottom inner edge of card frame, and that boot over mains input socket is not displaced.

5.3 CALIBRATION

5.3.1 HARDWARE CALIBRATION

This section details a complete procedure for adjustment of every preset control in the instrument. It is assumed that the instrument is fully functional, but with all controls incorrectly set. Some controls are interdependent, so it is recommended that the full procedure is carried out in the order given, unless it is proven that only a small section requires adjustment.

5.3.1.1 SUPPLY VOLTAGES

Set the adjustable supply voltages according to the following table.

TEST POINT SET TO CONTROL LOCATION

PLW PIN 1 (X AMP)	+5.0 – +5.1V	R1005)	
PLW PIN 5 (X AMP)	–5.0– +5.1V	R1011)	REAR PANEL
PLY PIN 4 (X AMP)	+11.9–+12.1V	R1021)	
PLW PIN 6 (X AMP)	–11.9– –12.1V	R1031)	
	–2.15– –2.25kV	R1106	EHT UNIT

5.3.1.2 BIAS

Select CH1 only, 0.5ms/cm, X-Y mode. Adjust realtime brill. to give a peak reading of +15V at R945 on tubebase PCB then set R1119 (BIAS) for just visible spot.

5.3.1.3 Y MEAN PLATE

Attach scope probes to the Y plates via 470Ω resistors. Select any menu. Note that this produces two symmetrical waveforms on the test scope. Set the crossover point of the two waveforms between +31 and +32V by adjusting A.O.T. resistor R3042 (Y Output and Sampling PCB).

5.3.1.4 X MEAN PLATE

Connect scope probes to the X plates via 470Ω resistors. Select any menu. Note that this produces two symmetrical waveforms on the test scope. Set the crossover point to +30V – +31V by adjusting R1917 (X amp PCB).

Select X expansion OFF. 'A' timebase only, 0.1ms/cm, test scope timebase 0.5ms/cm. Set the crossover of the ramp waveforms to +30V – +31V by adjusting R1961. Select X expansion on. Set the crossover of the ramp waveforms to +30 – +31V by adjusting R1963 (X Amp PCB).

5.3.1.5 FOCUS AND ASTIG

Select any menu, set to low brill. Adjust FOCUS and ASTIG (R1982, X Amp PCB) alternately for best definition, with vertical and horizontal lines equally sharp.

5.3.1.6 GEOMETRY, TRACE ROTATE

Select CH1 50mV/cm, AUTO TRIG, 'A' timebase only, 1ms/cm. Ground CH1 input, and set trace parallel to horizontal graticule lines with the TRACE ROTATE control (front panel).

Select CH1 AC coupled, and apply a 1MHz sinewave of 400mV p-p amplitude. Set the GEOMETRY control (R1984, X Amp) for the best compromise of X and Y edges for straightness and alignment with graticule lines.

5.3.1.7 POWER FAILURE

Set R80 (CPU card) clockwise. Reduce mains input to 210V and adjust R2080 until "POWER FAILURE" error message is displayed. Increase mains to 216V, press RESET (MPU card) and check that instrument returns to normal operation.

5.3.1.8 VOLTAGE GENERATOR

1. Connect a DVM of 0.1mV resolution between pins 2 and 3 of each of the following op. amps and set to zero (±0.1mV) with the corresponding preset.

Measure between pins 2 & 3 of:	Adjust
U2520	R2506
U2532	R2503
U2533	R2504
U2510	R2583
U2511	R2584

2. Carry out "DAC SELF ADJUST" procedure, see section 5.3.2.2.
3. Connect a DVM of at least 0.1% accuracy between pins 3 & 5 of PLAK.
   Set cursor 1 to extreme left, cursor 2 to extreme right. Set DVM reading to 8.19 – 8.21 volts by R2505.

   Note: R2581 and R2582 are adjusted during Y calibration. R2583 and R2584 may also require slight adjustment at this stage if centreline reading of zero does not correspond with physical screen centre.

5.3.1.9 Y CHANNELS

1. Disconnect PLCN from V GEN PCB, and link pins 4 to 5 and 1 to 3 in the free end of the lead.
2. Apply a 10MHz square wave, select A ramp, 10ms/cm and adjust R178 for zero tilt.
3. Fit a 50Ω termination to CH1 input BNC. Select CH1 only, 5mV/cm, A timebase only, 0.1ms/cm. Adjust R179 to give no trace movement on changing from AC to DC input coupling.
4. Remove input signal, adjust R197 for no trace movement on switching CH1 from 20mV to 50mV/cm.
5. Adjust R180 for no trace movement on switching between 2mV/cm and 5mV/cm.
6. Adjust R182 for no trace movement on inverting CH1.
7. a) Set CH1 to 10mV/cm, apply a 60mV square wave from a calibrator, and adjust R181 to give 6cm deflection.
   b) Set CH1 to 2mV/cm, apply a 12mV squarewave from a calibrator and adjust R183 for 6cm deflection.
8. Repeat items 2–7 for CH2, setting the corresponding 300 series controls.
9. Adjust R163 to centre CH1 trace.
10. Adjust R363 to centre CH2 trace.
11. Select ADD mode, and readjust R163 to centre trace.
12. Select CH1, and adjust R541 to centre trace.
13. Select CH2 and re-adjust R363 to centre trace.
14. Re-check that trace is centred for CH1, CH2 and ADD modes within ±0.1cm.
15. Re-connect PLCN to V GEN.
16. **ATTENUATOR COMPENSATION.**
    Apply a 1KHz squarewave to each channel in turn. Adjust trace for a flat top, using the trimmers listed below.

RANGE	TRIMMER	
	CH1	CH2
0.1V/cm.	C65	C66
1V/cm.	C67	C68

17. **INPUT CAPACITANCE**
Apply a 1KHz square wave to each channel in turn via a 1MΩ, 22pF standardiser. Adjust the trace for a flat top, using the trimmers listed below.

RANGE	TRIMMER	
	CH1	CH2
10mV/cm	C69	C70
0.1V/cm	C71	C72
1V/cm	C73	C74

18. **PULSE RESPONSE**
Apply a fast-rise, 1MHz square wave to CH1. Set CH1 to 10mV/cm and adjust input to give 5cm amplitude. Adjust C3022, C3023 (Y output and sampling PCB) and C534 and C513 (Y Preamp) for optimum pulse response. Apply the pulse to CH2, and adjust C544. C513 may require a slight re-adjustment to give the best compromise between channels. C142 or C342 may be removed to improve channel matching. Check channel bandwidths, and if necessary, repeat above procedure for the best compromise between pulse response and bandwidth.

19. **Y SHIFT AND ADC.**
Check that GND buttons are not engaged and do not operate them during this action.

Cancel existing software corrections on the Y axis (select GENERAL MODE 83).

Select CH1 20mV/cm 'A' only, 0.2ms/cm and apply a 1KHz 120mV p-p square wave from a calibration source. Select cursors 1 and 2, place cursor 1 on the centre of the negative half cycle, and cursor 2 on the centre of the positive half cycle.

19a. Select CALCULATION MODE 41, and enter 1 2 when cursor selection is requested. Adjust R2660 (Acquisition PCB) until voltage between cursors reads 120mV ±1mV. Remove signal, QUIT, adjust ℄ reading to zero by Y shift and set cursor reading to OV by adjusting R2669.
Repeat from 19a until no further adjustment is required.

19b Remove input, and adjust CH1 shift for a centre line reading of zero. Centre trace on screen by adjusting R2584 (V GEN). Apply +120mV to CH1, adjust CH1 shift to give a centre line reading of +120mV and centre trace on screen by adjusting R2581. Repeat from 19b until no further adjustment is required. Apply −120mV shift trace to centre screen and check for a centre line reading of −120mV ±1mV. Repeat for CH2, adjusting R2583 for zero, and R2582 for +120mV ±1mV.

Carry out Y software calibration procedure, see section 5.3.2.4.

5.3.1.10 TIMEBASES
Since this operation requires many changes between Xtal and analogue time, it is recommended that the 'D' button facility is used to alternate between them. This may be achieved by setting TRIGGER MODES 11 and 12 on the 'D' button with the following sequence:-

S,911,S,D11,Q,12,S,D,21,Q .

Options on 'D' button can now be used to force Xtal or analogue time reading as required.

No Y signal is required.

Cancel existing horizontal software correction (GEN MODE 82).

1. Select A timebase only, AUTO TRIG, 10μs/cm.
2. With analogue time displayed, select cursor 1 and adjust it to read 10μs.
3. Change to Xtal time, and adjust R1613 (Timebase PCB) to read 10μs ±0.01.
4. Change to analogue time, set cursor 1 to read 90μs.
5. Change to Xtal time, adjust R1275 (Timebase PCB) to read 90μs ±0.5.
6. Repeat items 2–5 until no further adjustment is required.
7. Select 2μs/cm, set cursor 1 to 18μsec analogue time.
8. Change to Xtal time and adjust C1251 (Timebase PCB) for 18μs ±0.1.
9. Select 0.5ms/cm, set cursor 1 to 4.5ms analogue time.
10. Change to Xtal time and adjust R1255 to 4.5ms ±0.03.
11. Re-check from 1, since the controls are slightly interactive if large adjustments are required. Items 1 to 20 are summarised in the table below for quick reference:-
(figures in square brackets relate to B ramp)

REPEAT TO CONVERGENCE	A	10μs/cm	Cursor 1	10μs
	X	"	R1613[R1391]	10μs ±0.01
	A	"	Cursor 1	90μs
	X	"	R1275[R1375]	90μs ±0.05
	A	2μs/cm	Cursor 1	18μs
	X	"	C1251[C1351]	18μs ±0.01
	A	0.5ms/cm	Cursor 1	4.5ms
	X	"	R1255[R1355]	4.5ms ±0.03

12. Select 'B' timebase only, (HOR 03) B starts with A (TRIG 18) and repeat above sequence, using the controls shown in square brackets in the table. Use cursor w, with T/B A set one range slower than 'B'

5.3.1.11 X AMP GAIN

1. Select A timebase only 0.5ms/cm, X expansion OFF.
2. Set timecal output to 0.5ms. (GEN MODE 88, 89).
3. Attach probe from CH1 to timecal output and select CH1 0.1V/cm.
4. Adjust R1946 (X amp) to give one marker/cm.
5. Set timecale output to 50μs (GEN MODE 89).
6. Select X expansion ON, X tracks cursor OFF (HOR 11,12).
7. Adjust R1948 (X Amp) to give one marker/cm.
8. Set timecal output to 40ns (GEN MODE 89).
9. Set A timebase to 50ns/cm.
10. Set C1906 and C1924 to minimum capacitance, then increase them equally to give one cycle per 8cm.

5.3.1.12 DISPLAY GAIN AND OFFSET

1. Select CH1, A timebase only 0.1ms/cm. Apply a sinewave input to give approx. 2 cycles of 6–6cm amplitude.
2. Store CH1, and display stored trace, DO NOT ADJUST Y SHIFT AFTER STORING TRACE.
3. Adjust R2735 (Data Display PCB) to centre alpha-numeric display in X direction.
4. Adjust R1915 (X amp) until replayed trace is displayed to some X scale as real-time. (Front panel X shift may be adjusted as required).
5. Adjust R2720 until stored trace is in exact registration with realtime (Slight adjustment of X shift and R1915 may be required).

5.3.1.13 ADC PULSE RESPONSE

1. Select A timebase only 0.1ms/cm. CH1 10mV/cm. Apply a 10KHz fast rise squarewave of approximately 5cm amplitude.
2. Set up both 'D' button selections to store CH1. Sequence S511141719SD31 [ ].
3. Display stored trace, and adjust R3174 (Y output/sampling) for a flat top, using the 'D' button to obtain a fresh stored trace after each adjustment.
4. Select 'A' timebase 50ns/cm. Apply 1MHz fast rise squarewave.
5. Adjust C3161, C3155 and R3161 for best pulse response, storing a fresh trace after each adjustment.
6. Check the stored trace bandwidth, and, if necessary, repeat 5 for best compromise between pulse response and bandwidth.

5.3.1.14 TRIGGER SYSTEM

1. Select 'A' timebase 0.1ms/cm. Apply a 5KHz sinewave of 2cm amplitude to CH1, select A trig. source = CH1, AC coupled. Set A trig level to centre. Adjust R720 (Trig. PCB) until trigger point (start of trace) is in the centre of the waveform.
2. Adjust R184 (Y pre-amp– for no trace movement on switching from AC to DC trig. coupling.
3. Apply signal to CH2, and adjust R384 (Y pre-amp) for no trace movement on switching from AC to DC trig coupling.
4. Select COMPOSITE TRIG and adjust R556 (Y preamp) for no trace movement on switching from AC to DC trig. coupling.
5. Select TRIG VIEW, and adjust R582 (Y preamp) to bring trigger point to centre horizontal graticule line.
6. Trig view amplitude should be within ± 5% of corresponding Y channel. Adjust A.O.T. R599 (Y preamp) for best compromise between CH1 and CH2 trig. sources.
7. Select External Trig. Apply a 0.25V 1KHz squarewave to 'A' external trig socket, ÷ 10 out. Adjust C602 for a square corner on on the trig. view waveform.
   Engage ÷ 10, increase input to 2.5V and adjust C607 and C609 for a square corner.
8. Select B starts on B trig B ONLY. Set 'A' timebase to 0.2ms/cm, 'B' to 0.1ms/cm. Apply a 5KHz sinewave of 2cm amplitude to CH1, and set both trig sources to CH1, AC coupled. Set 'B' trig. level to centre, and adjust R820 (Trig. amp) to give trigger point in centre of waveform.
9. Apply a 2.5V 1KHz squarewave to B external input, ÷ 10 out. Check that test 'scope and probe are correctly compensated by observing the signal source directly, then connect probe to R804 (trig amp, 560Ω). Adjust C652 for a square corner. Increase input to 5V, select ÷ 10 and adjust C657 and C659 for a square corner.
10. Apply a 1MHz fast rise squarewave to A external input, ÷ 10 out, to give 3cms amplitude on trig. view. Set A timebase to 50ns/cm A ONLY and adjust C525 (Y pre-amp) for best compromise between bandwidth and pulse response.

5.3.1.15 X-Y MODE

1. Select CH1, and apply a 1KHz squarewave to CH1. Adjust for 8cm amplitude. Select CH2, with input still to CH1, A trig to CH1. Select X-Y mode and adjust R715 (trig amp) to give 8cm horizontal deflection.
2. Apply input to CH2, select A trig to CH2, Y mode to CH1 and check that horizontal deflection is 8cm ± 15%.
3. Select external trig. Apply 400mV to the external A input, and check that the horizontal deflection is 8cm ± 15%.
4. Apply a 500KHz sinewave to CH1 and CH2 inputs, to give 5cm amplitude in DUAL Y mode. Select X-Y mode, A trig. source CH1, Y mode CH2. Elipse should be <2mm wide, adjust A.O.T. C709 if necessary.

5.3.1.16 INTERNAL CALIBRATOR

Attach a DVM to the "1V CAL" output. Attach a flying lead to inner end of C2, shown * on fig. 5.2.12. (X amp PCB). Ground the lead to the instrument chassis to stall the oscillator. If DVM reads zero, momentarily release the ground connection, and ground again. Repeat until a reading of approximately 1V is obtained (There is a 50% chance that the oscillator will stall in the "zero" state). Adjust reading to 1.00 ± 0.005V with R1914 (X amp).

5.3.1.17 POD DELAY

Attach word trigger pod.
Connect negative going 1MHz squarewave of 2.5 volts amplitude to CH1 input, both pod qualifiers and all 8 pod inputs.
Select on pod:- D1 = 1, D2–8 = X, Q1 = 1, ECL.
Select CH1, 'A' timebase 0.1μs/cm, BIN Display ON (Calculation Mode 14).

Move cursor 1 along trace, and check that display reads 1111 1111 when cursor is on positive half cycles, and 0000 0000 on negative half cycles. Check that change of display coincides with cursor on vertical section of waveform. If not, adjust R1596 (Timebase) to obtain the best compromise for all edges (positive and negative).

5.3.1.18 PLOTTER OUTPUTS

1. Attach a DVM to the plotter X output.
2. Reset the plotter (MEM MODE 39) and set output to zero ±2mV by R2762 (Data Display card).
3. Set X to full scale (MEM MODE 41) and set output to 1.024V ± 2mV by R2771 (Data Display card).
4. Attach DVM to Y output.
5. Reset Plotter (MEM MODE 39) and set output to zero ± 2mV by R2764 (Data Display card).
6. Set output to + FSD (MEM MODE 42) and set to + 0.406V ± 2mV by R2763.
7. Set output to –FSD (MEM MODE 43) and check that output reads –0.410V ±2mV.

5.3.1.19 20MHz OSCILLATOR

Select PRE-TRIG CAPTURE mode, and ARM without a trigger source to run oscillator continuously. Adjust R2635 (Acquisition PCB) for 20MHz ± 5% at U2663 pin 8.

5.3.1.20 100MHz OSCILLATOR

Adjust L1541 (Timebase PCB) for maximum signal at U1591 pin 15 (Timebase PCB).

5.3.1.21 FLY-BETWEEN BLANKING

Select any menu, and adjust A.O.T. resistors R2710, 2713, 2778 (Display PCB) for minimum "tail" between dots of characters.

5.3.1.22 BLANKING LEAD TIME

Select Dual channel and shift CH1 to + 3cm and CH2 to –3cm. Set 'A' timebase to minimum speed, with high brill. Adjust C2405 (Display Management PCB) for minimum "tail" between moving spots.

5.3.2 SOFTWARE CALIBRATION PROCEDURES

5.3.2.1 GENERAL

These procedures take place after the instrument hardware has been manually calibrated and increase the accuracy of the instrument's measuring system, by storing various correction coefficients. Thus, hardware calibration must be satisfactory before software calibration will be successful. However, the various routines do give some assistance to the user, if the hardware is not within range.

In general, software calibration should only be required in three circumstances: on first leaving the factory; if the non-volatile R.A.M. is corrupted (e.g. battery failure); or if any of the relevant hardware is altered.

Software calibration can be used at any time, to obtain higher short term accuracy, and x10 probe calibration is required whenever the probes are changed.

General Mode, option 81 (Voltage generator DAC Self Adjust) is **essential** in the above three circumstances, and is not recommended at any other time, because it affects the calibration of the whole instrument.

The other options, General Mode options 51–56 are not required, except in the above three circumstances, but can be used at any time. In general, software calibration does not affect the trace on the screen, only the accuracy of the time and voltage readings displayed on it. x10 probe calibration (i.e. General Mode options 53 and 54, CH1 and CH2 calibration from probe tip) must not be selected if the relevant channel has not been calibrated from the BNC input. i.e. option 55 must be performed before option 53, and option 56 before option 54.

Probe tip calibration is in fact an exception in that it should be performed anew whenever a different x10 probe is chosen (or if probes are swapped from one channel to another). To avoid this the user can select General Mode option 84 (select default probe calibration) in which case calibration reverts to the 2% accuracy of the probe itself.

5.3.2.2 VOLTAGE GENERATOR DAC SELF ADJUST. (GENERAL MODE OPTION 81)

INTRODUCTION

As stated before, this option should be used only when necessary, as it affects the software calibration of the whole instrument.

Furthermore, the routine uses Store 1 to display the results of the calibration, so any information in Store 1 is lost. The hardware of the Vgen system can only be accurately set up with the help of this routine, so it is designed to cycle repeatedly until the user presses "QUIT".

In operation, the user selects option 81, and the routine calculates a new set of coefficients and displays them on the screen, then calculates another set. The user adjusts the hardware until they are satisfied and then prsses "QUIT" once. This temporarily stops the cycle from repeating, for observation. The user then has the choice of pressing "[ ]" to continue or "QUIT" to stop the routine if they are satisfied with the result. A cycle normally take about 5 seconds, unless the hardware is in need of large adjustment.

OFFSET ADJUSTMENT

The first adjustment required from the user is of RV2518. At the end of each cycle, a new offset is calculated and idsplayed on the top left of the screen (of the form "OFFSET = –63"). The number is in the range +96 to –128. RV2518 should be adjusted until offset is ±10.

GAIN ADJUSTMENT

When the offset is correct, the user should observe the displayed contents of store 1, and adjust RV2507 as follows. The screen shows the results in the form of a

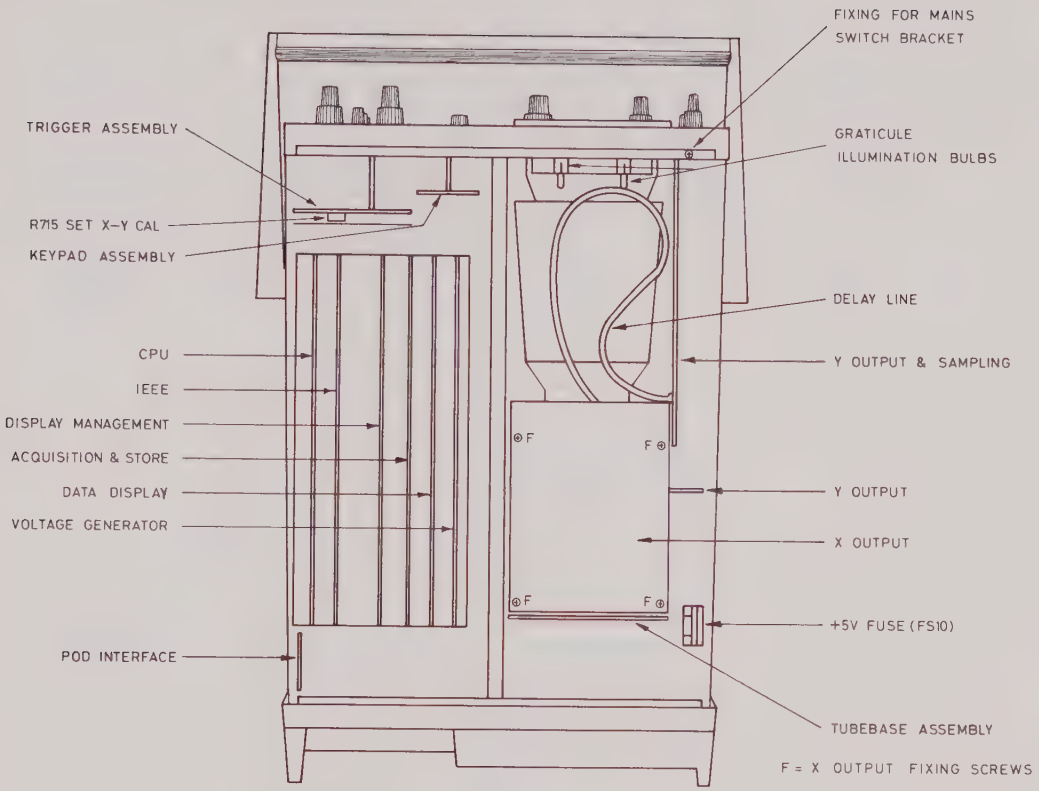


Fig. 5.2.1 View of Top of Instrument

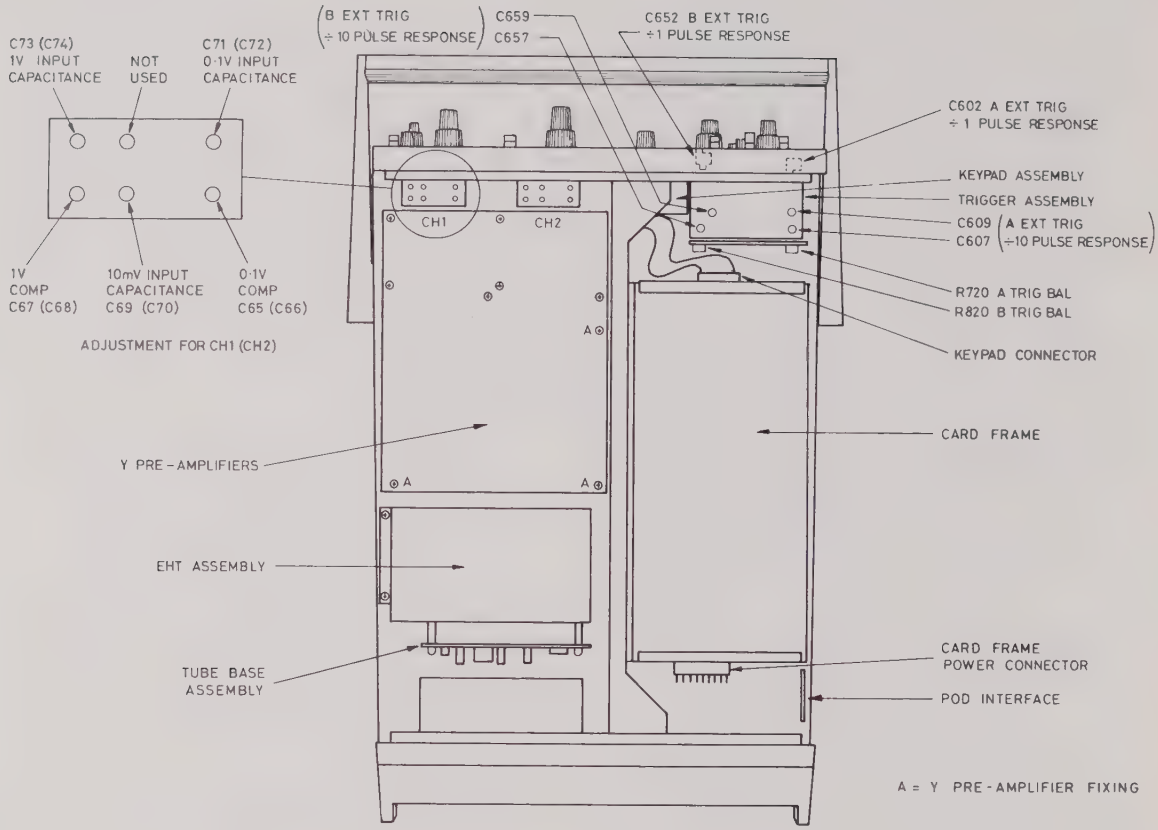


Fig. 5.2.2 View of Base of Instrument

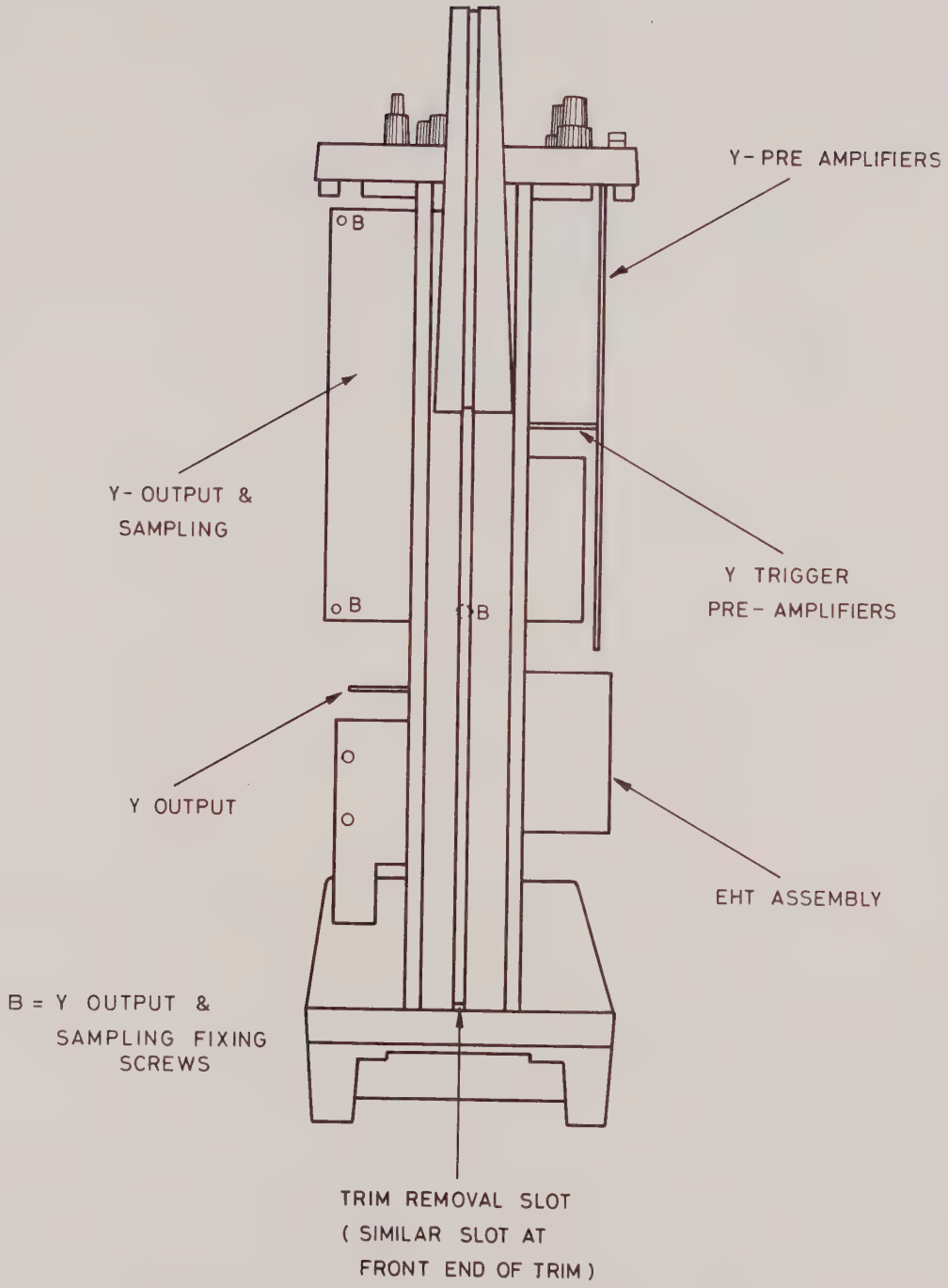


Fig. 5.2.3 View of Left Hand Side of Instrument

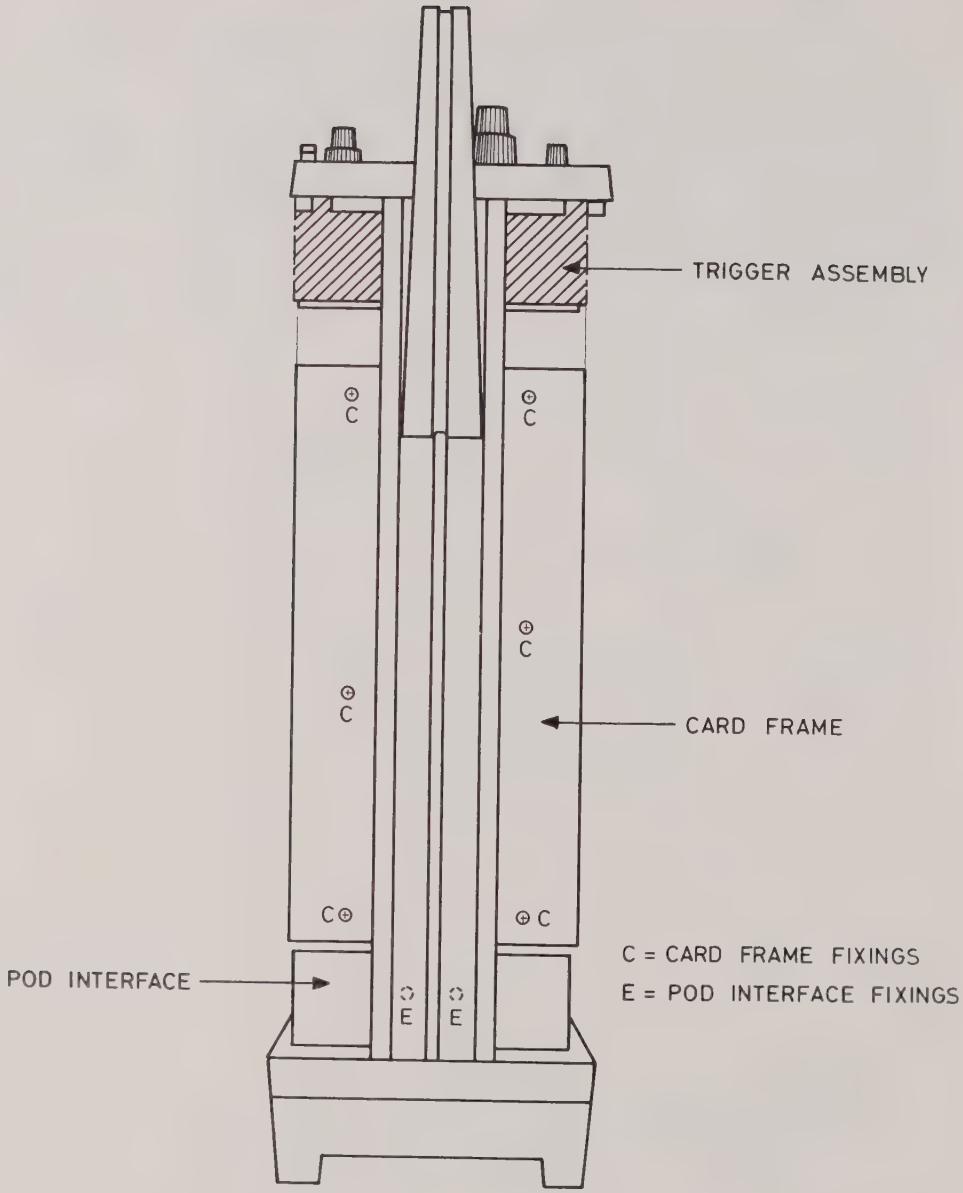


Fig. 5.2.4 View of Right Hand Side of Instrument

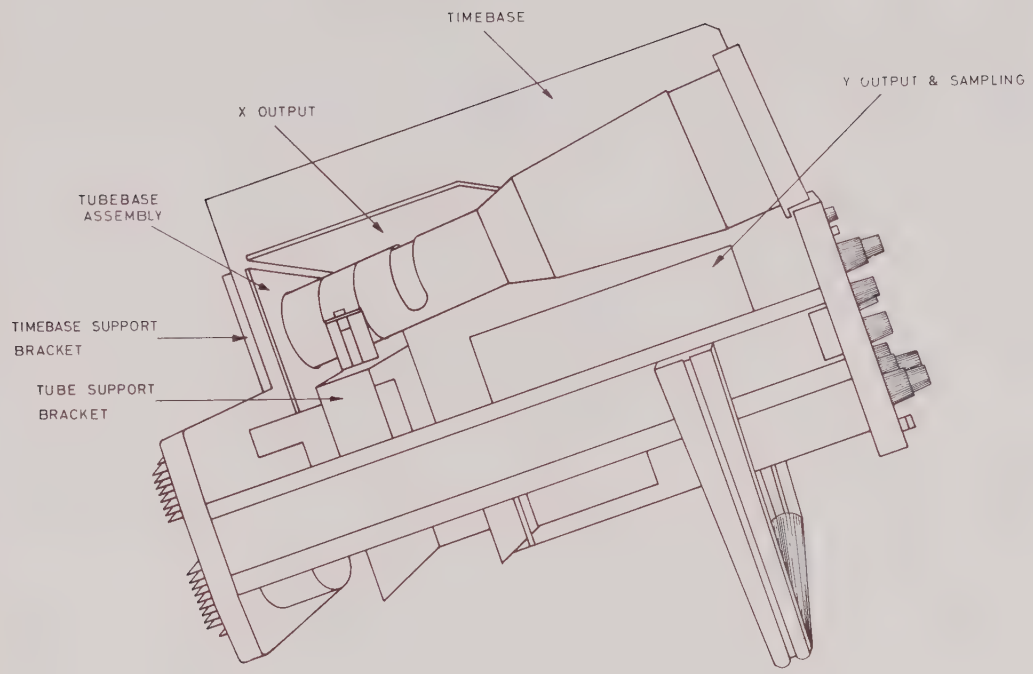
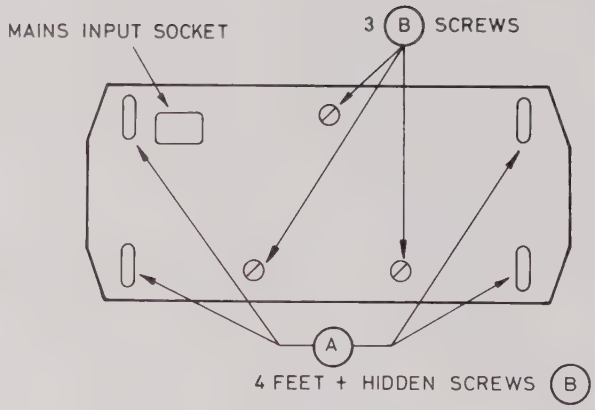
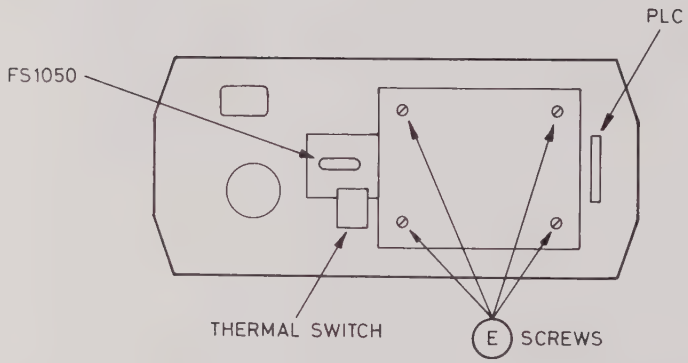


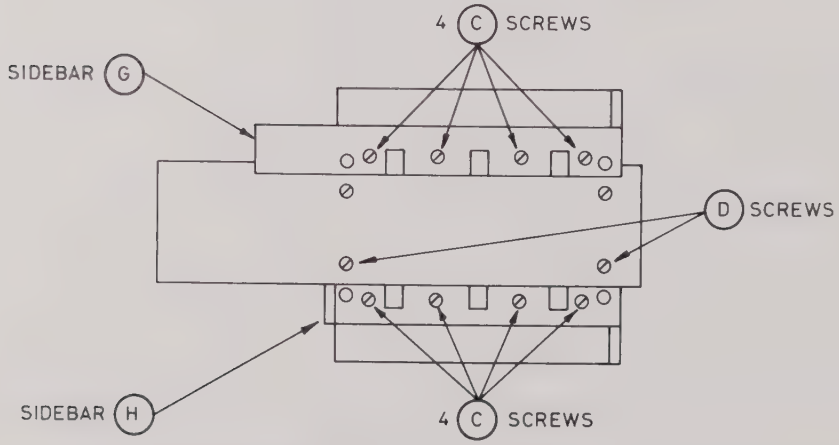
Fig. 5.2.5 Timebase, Tubebase and X-Output Assemblies in maintenance Position



a. INSTRUMENT REAR VIEW.



b. FALSE REAR PANEL REMOVED.



c. UNDERVIEW OF HEATSINK/PCB ASSY.

Fig. 5.2.6 Physical Access to Power Supply

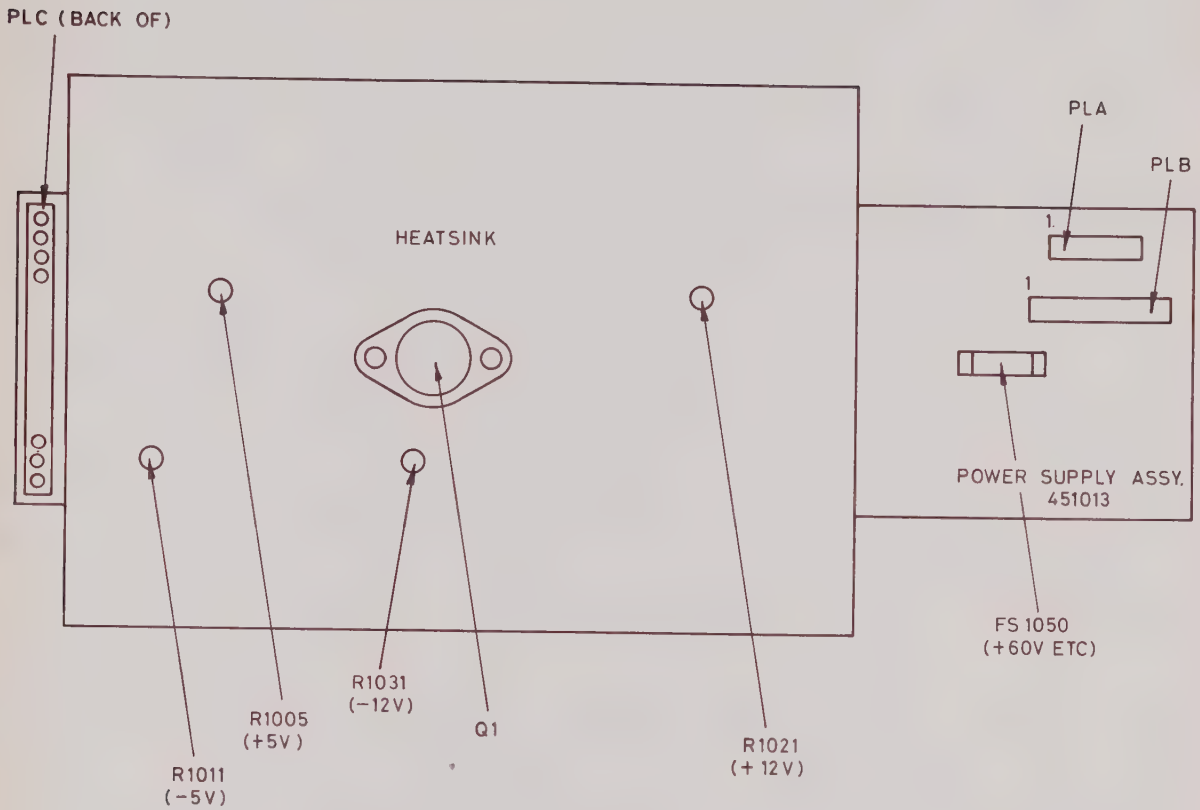


Fig. 5.2.7 Location of Power Supply Adjustment Potentiometer

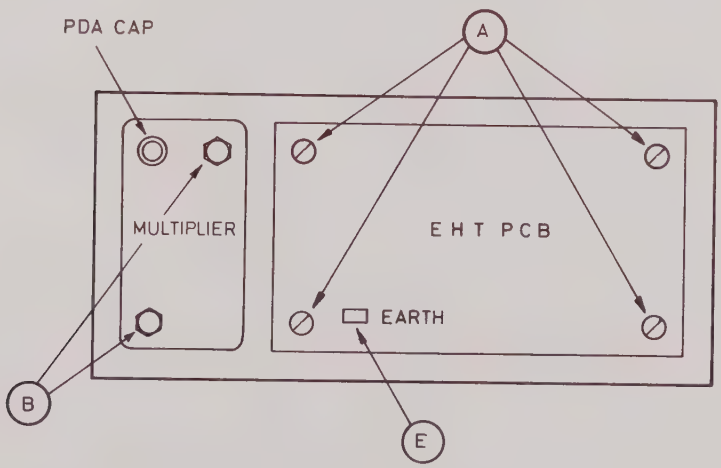


Fig. 5.2.8 Access to E.H.T. Assembly

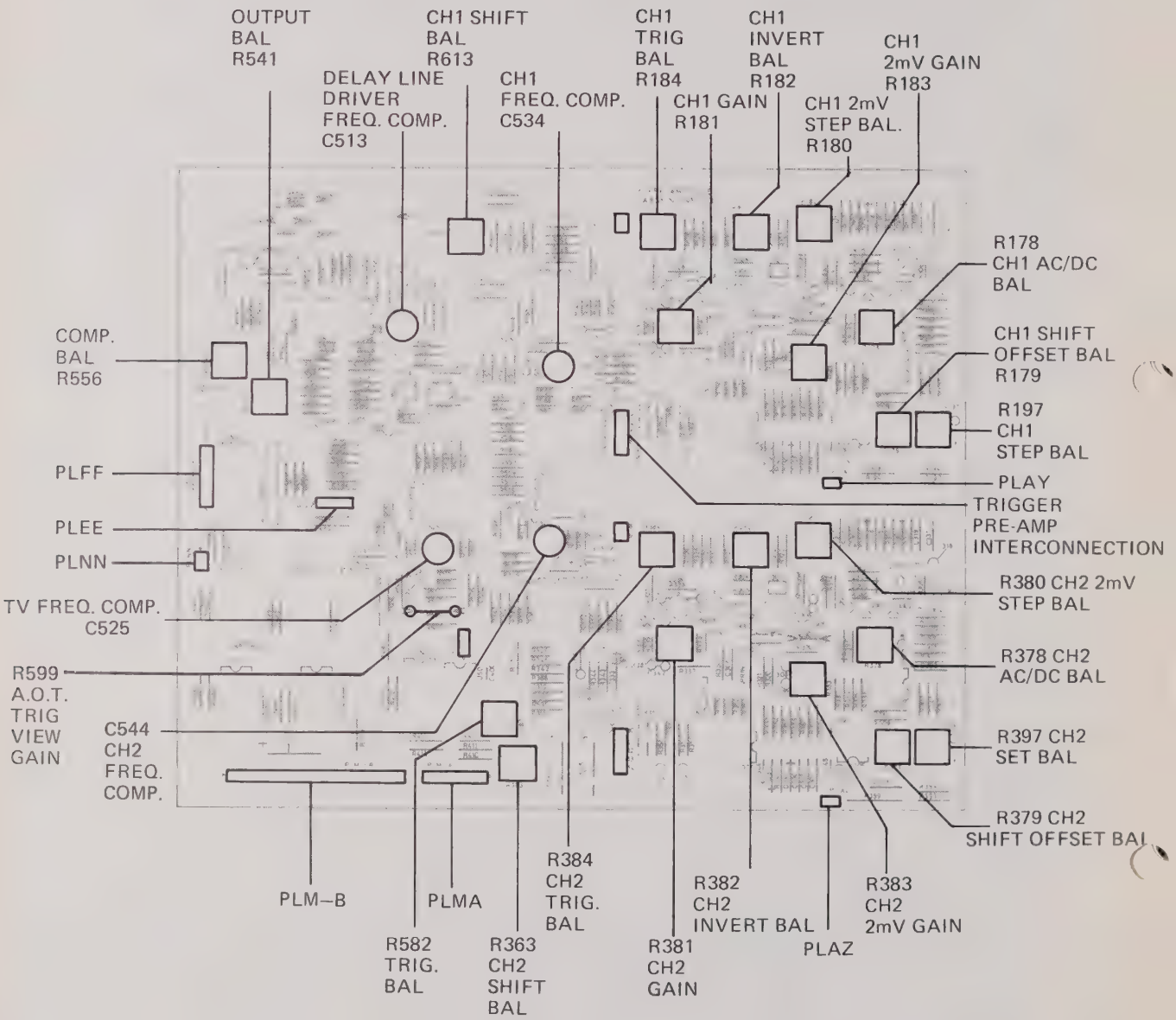


Fig. 5.2.9 Y Pre-Amp PCB

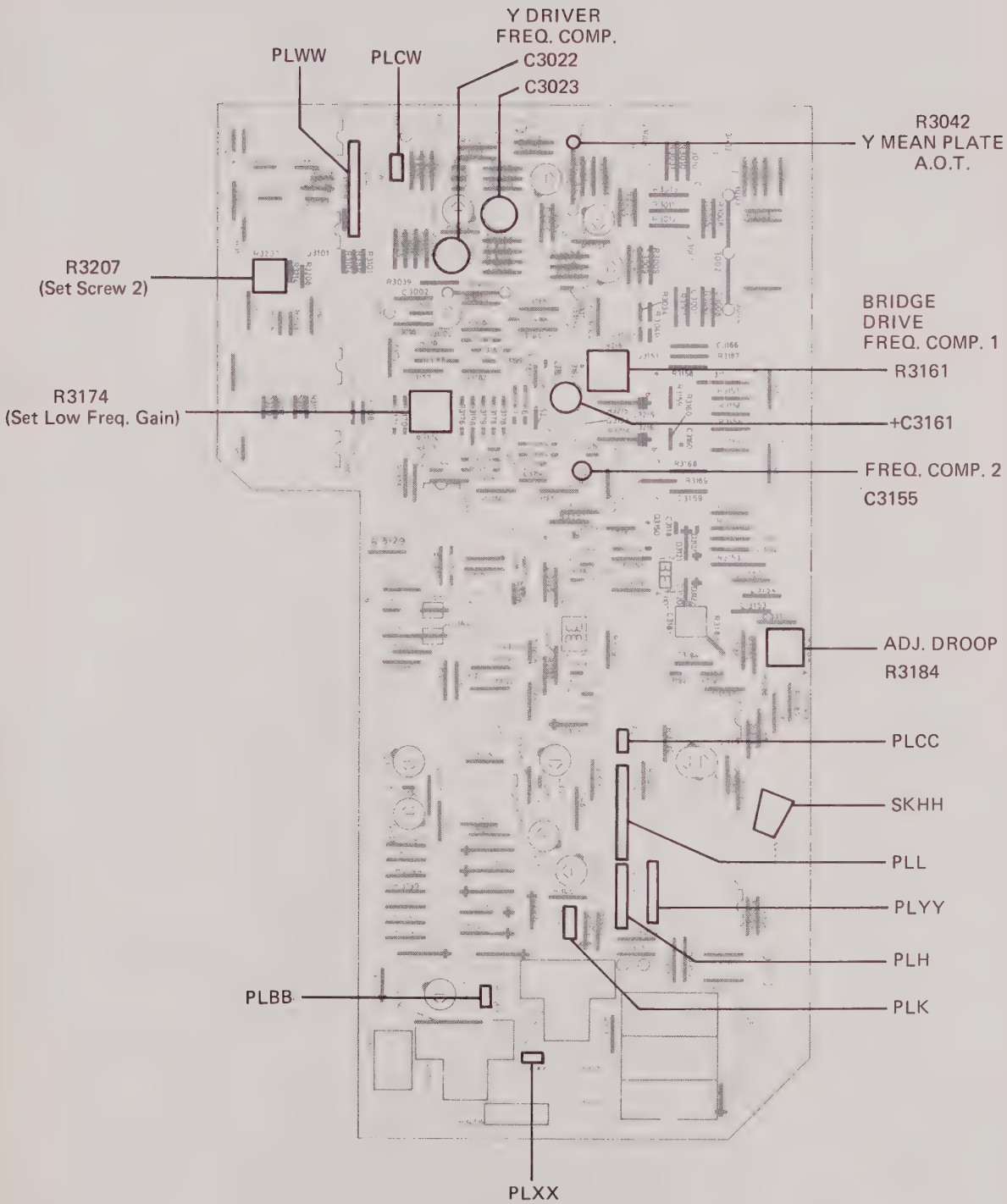


Fig. 5.2.10 Y-Output and Sampling PCB

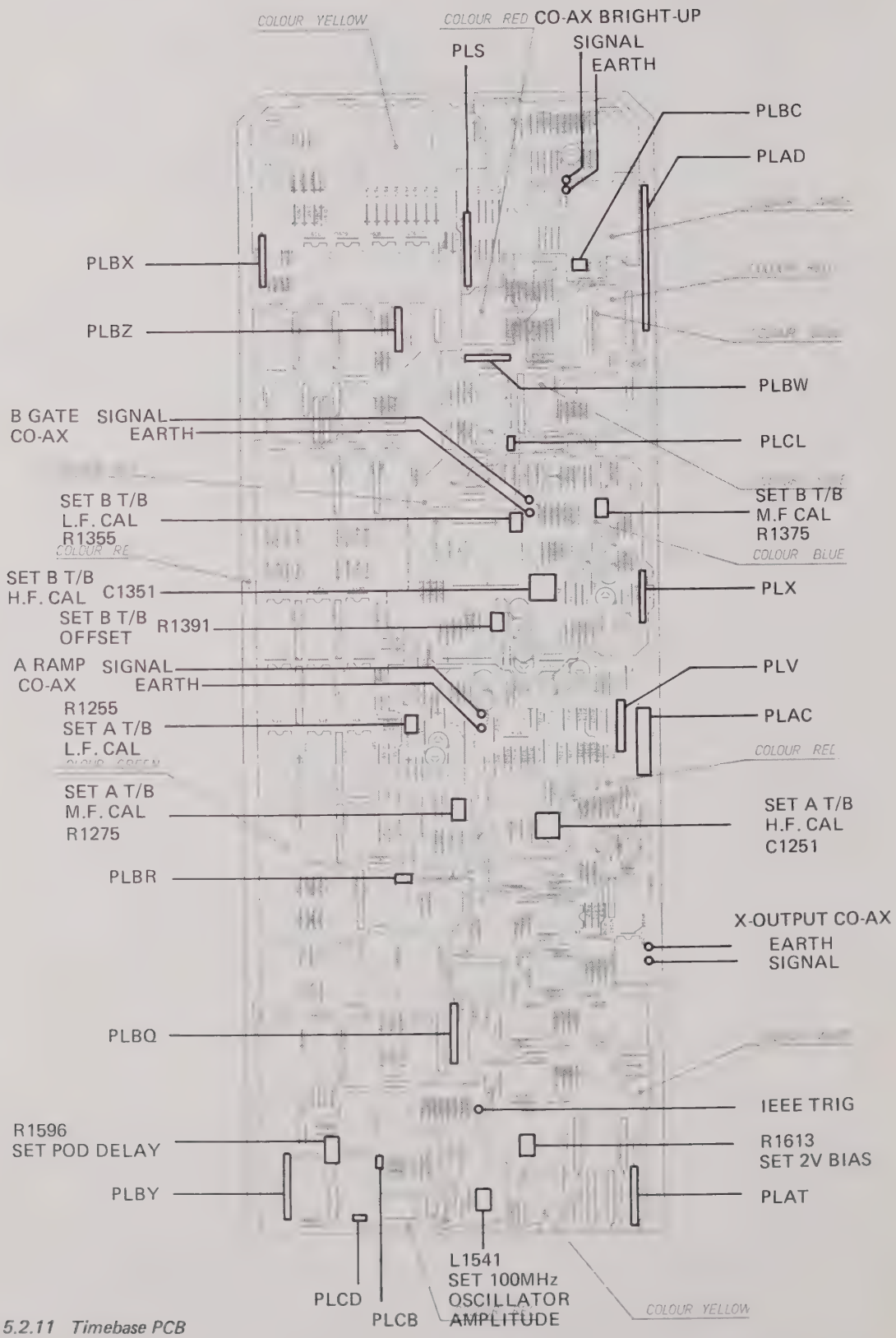


Fig. 5.2.11 Timebase PCB

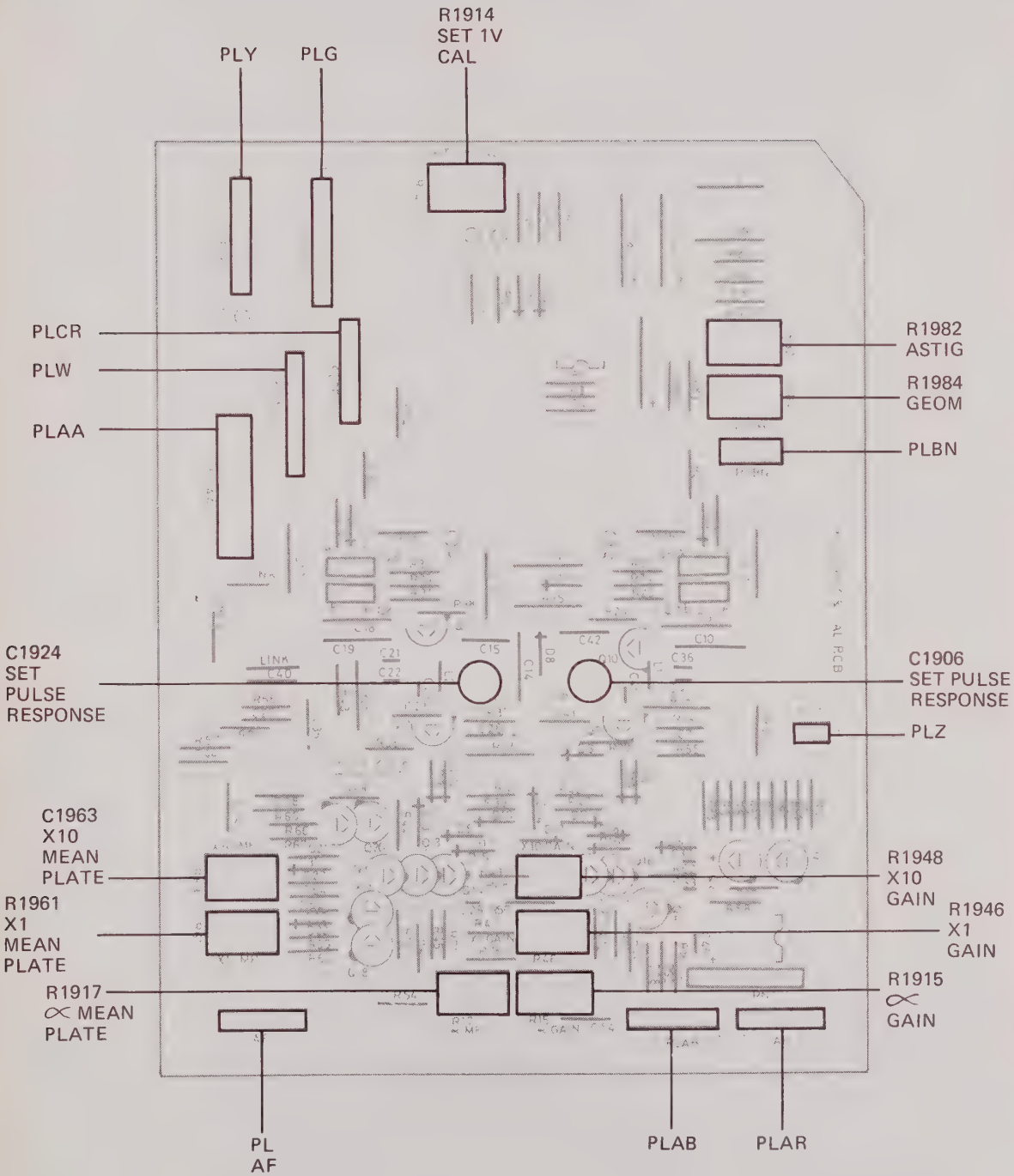


Fig. 5.2.12 X-Output & Cal PCB

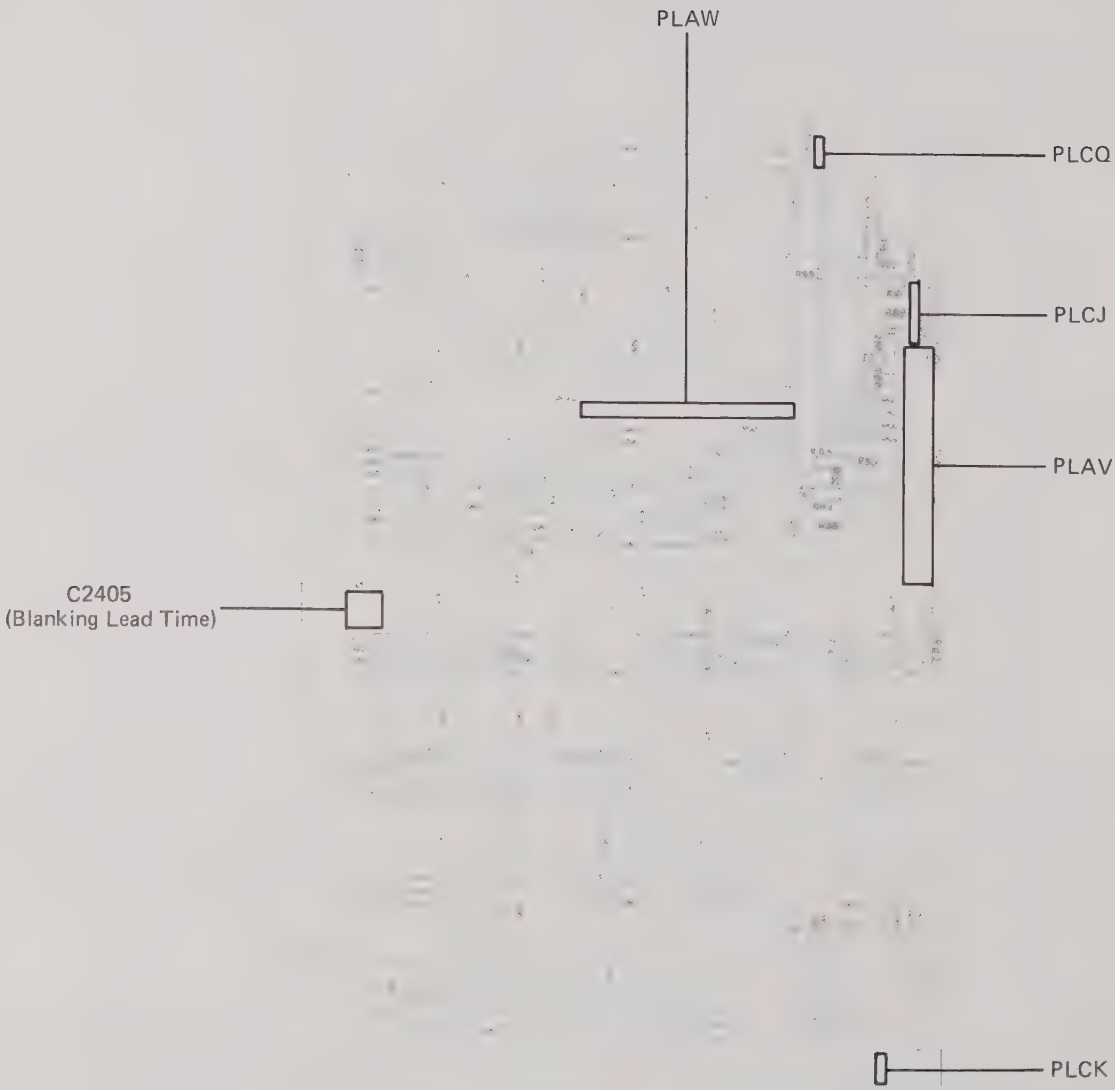


Fig. 5.2.13 Display Management PCB

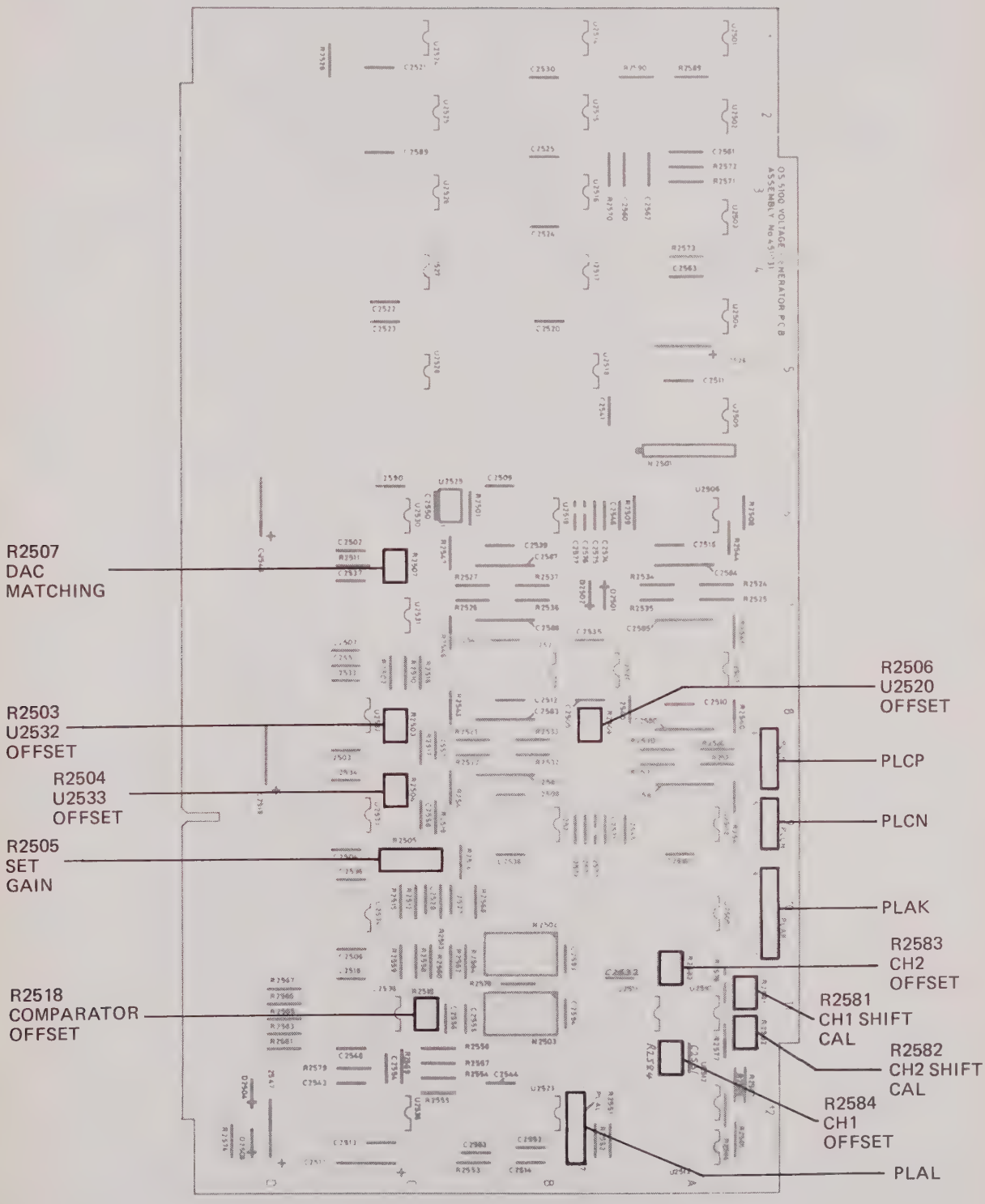


Fig. 5.2.14 Voltage Generator PCB

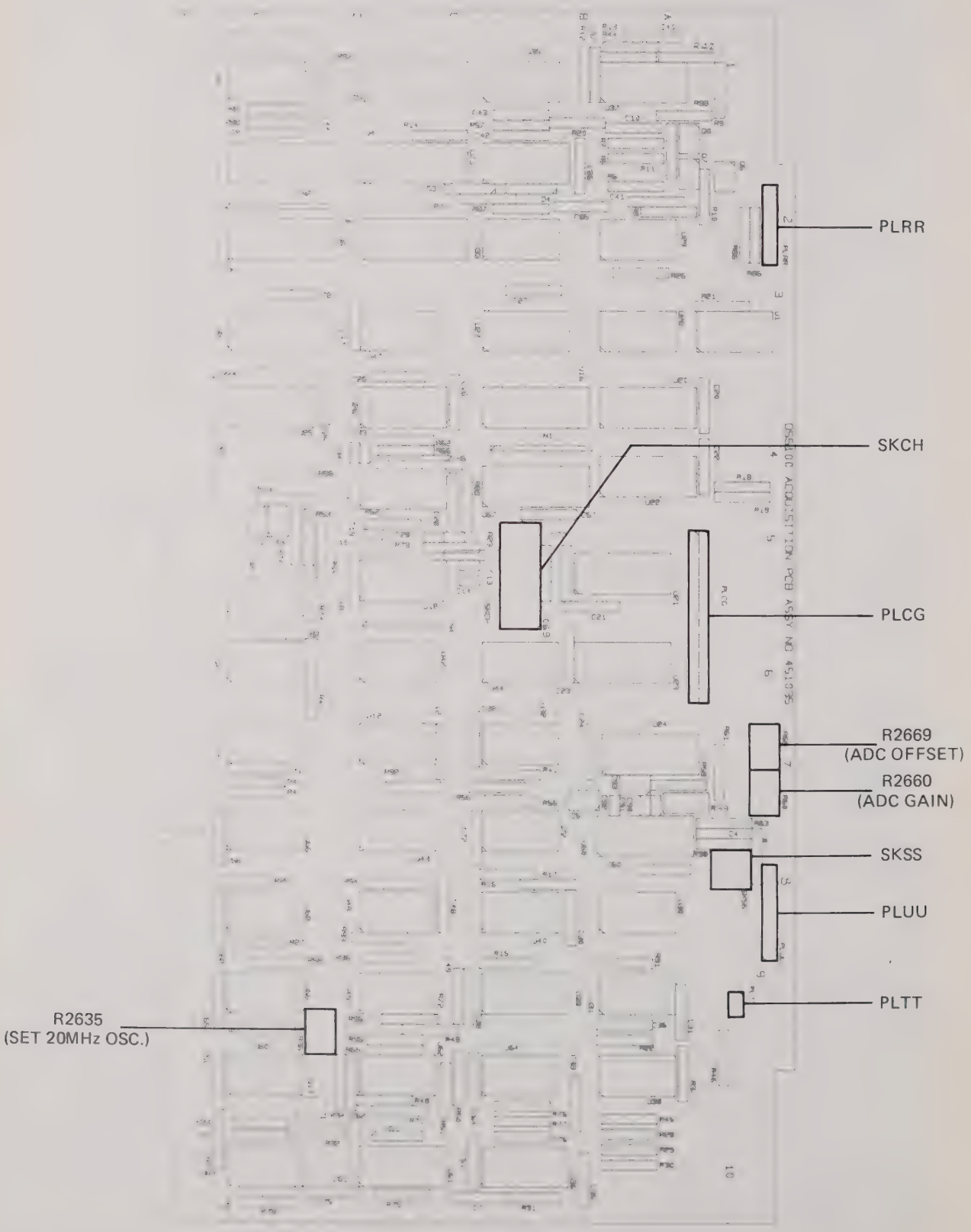


Fig. 5.2.15 Data Acquisition PCB

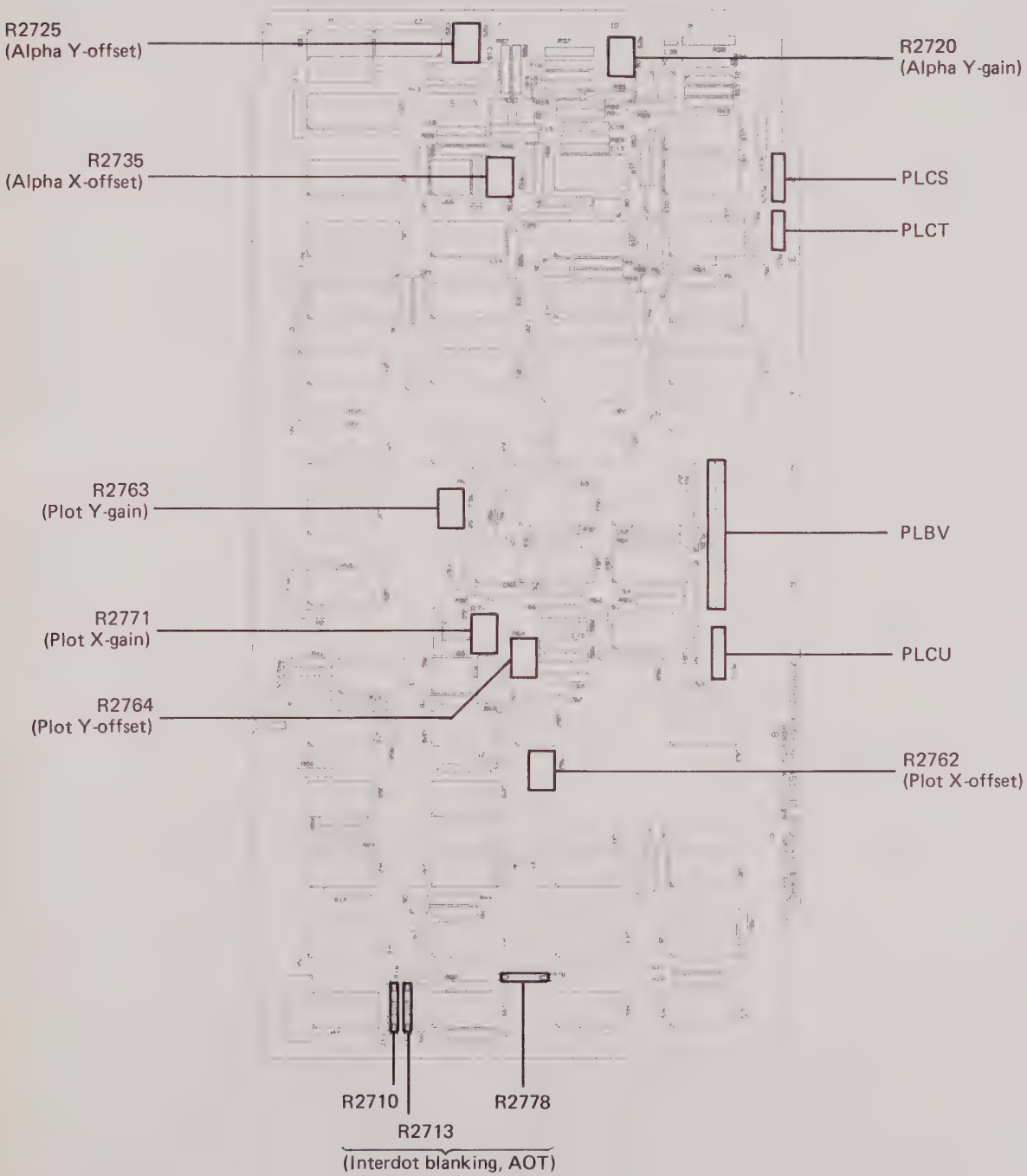


Fig. 5.2. 16 Data Display PCB

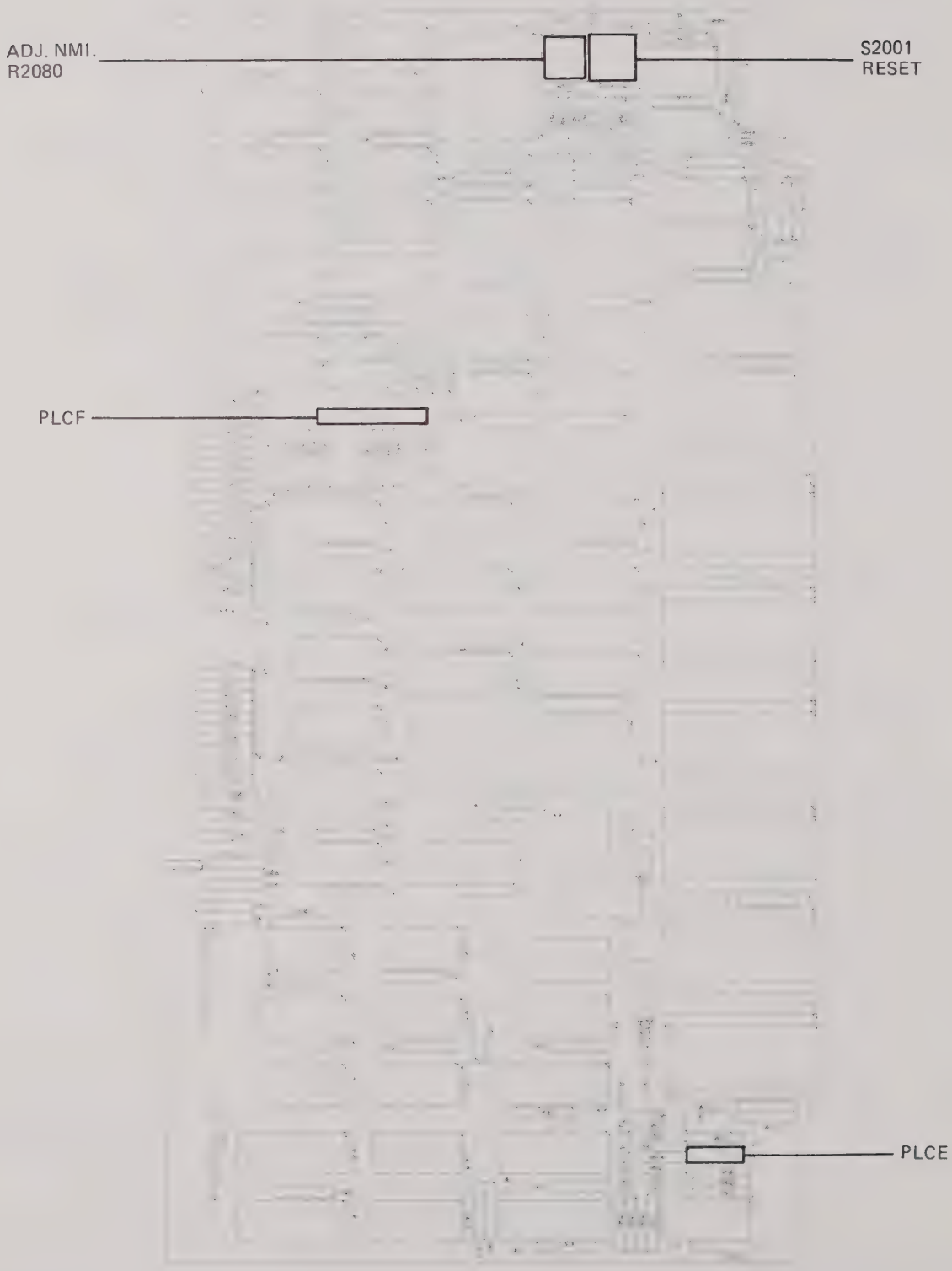
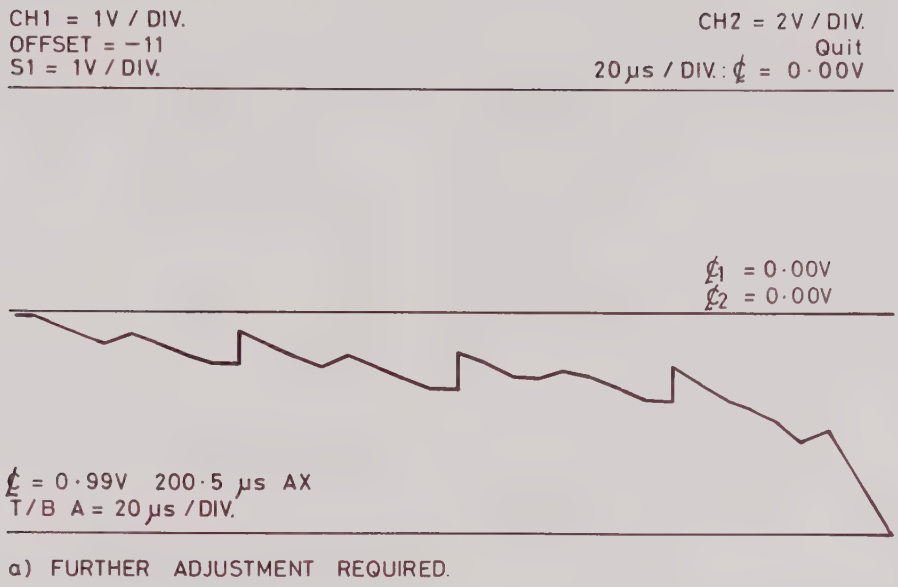
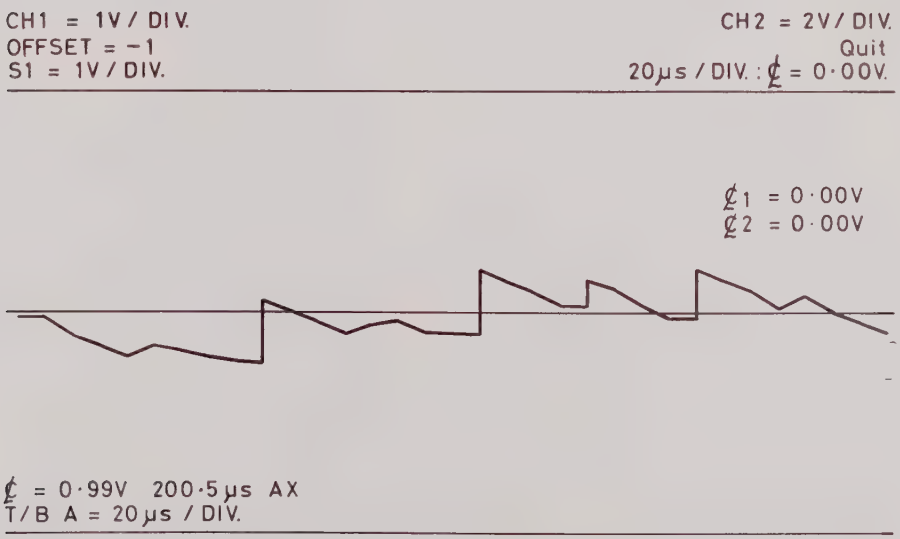


Fig. 5.2.17 CPU PCB



a) FURTHER ADJUSTMENT REQUIRED.

Fig. 5.3.1a DAC Self Adjustment Graphs



b) OPTIMUM ADJUSTMENT (START POINT NEARLY EQUAL TO END POINT).

Fig. 5.3.1b DAC Self Adjustment Graphs

graph, with 3 horizontal lines showing maximum limits and the nominal centre line. See Fig. 5.3.1 for examples.

Because of slight noise in the system (and the fact that the adjustment procedure is extremely sensitive and amplifies any noise present) the graph on the screen will change in detail from cycle to cycle. However, the basic shape should stay the same. The graph should start (at the left) at the centre line, and should in theory stay on that centre line across the screen. In practice, there will be an overall slope up or down towards the top or bottom limits. As RV2507 is adjusted the slope of the graph should change, so that at a particular position of RV2507 the graph seems to be close to the horizontal. When this step is reach "Quit" can be pressed to observe the graph in detail.

The optimum calibration adjustment is reached when the final point on the graph is on the centre line.

Adjustments to RV2507 have effects that "build up" across the screen, so it is best to make small adjustments and then wait for an entire cycle to observe the effects of the adjustment.

5.3.2.3 HORIZONTAL SOFTWARE CALIBRATION. (GENERAL MODE OPTIONS 51 and 52)

INTRODUCTION

These options are used when the timebase hardware is satisfactorily adjusted for calibration, to obtain full measurement accuracy.

The routines display the results of their calculation so that any final hardware adjustments can be made.

OPERATION

The operational procedure is extremely simple, requiring little external help, and no supplied signals.

The user selects option 51 (for timebase A calibration) or option 52 (for Timebase B calibration), and then obeys the various requests on the screen (e.g. select/B A: = CAL means that the timebase sweep calibration control must be set to "CAL"). The first timebase range to be calibrated will be 0.1ms/DIV (as requested e.g. "T/B B: = 0.1ms/DIV"). The routine will calibrate that range, and display the results on the screen in the form of a table (see Fig. 5.3.2).

In each position in the table there will be displayed a value between + 127 and −128, representing the calculated correction coefficient. If the calculation was unsuccessful, "MAX" or "MIN" will be displayed. Under these circumstances, the hardware should be adjusted as detailed in section 5.3.1.

Once the first timebase range is calibrated, all other ranges must be selected and calibrated, one by one (message "SELECT NEXT RANGE").

The ranges can be selected in any order. On all further ranges only one cursor is calibrated, and only one pair of results is displayed. From the results table displayed on the screen, some information can be obtained as to how accurately the hardware has been set up. If perfect, all displayed coefficients should be close to zero.

The procedure can be aborted at any time by pressing "QUIT".

CALIBRATION TABLE

(MAX = 127, MIN = −128)

T/B A = 0.1ms/DIV

	GAIN	OFFSET
C1	−3	+120
C2	−103	−17
C3	MAX	
C4	+63	20

Fig. 5.3.2 Horizontal Software Calibration Results

If there is a major hardware misadjustment, it is possible to get a "TIMEOUT ERROR".

This could mean that the delay system counter is not working, or that the timebase sweep is less than 10.5 DIVS (so that the cursor, positioned at 10.5 DIVS is not on the timebase ramp). See Sections 4.6 and 4.9 for details of the associated hardware.

5.3.2.4 VERTICAL SOFTWARE CALIBRATION (GENERAL MODE OPTIONS 55 and 56)

INTRODUCTION

These are used when the Vertical hardware is satisfactorily calibrated, to obtain full measurement accuracy.

The routines display the results of their calculations so that any final hardware adjustments can be made. See section 5.3.1.

OPERATION

To calibrate CH1, select option 55. To calibrate CH2, select option 56.

As the procedure is somewhat lengthy, the user is given the choice of calibrating a single range or of calibrating all the ranges. In either case, the user follows the instructions on the screen. The equipment required consists of a stable floating power supply range 6mV to 50volt and a DVM accurate to ±0.05%, or preferably an accurate oscilloscope calibrator, with the same range. The sequence is designed to suit such an oscilloscope calibrator, so that the minimum number of manual operations should be required.

The sequence if successful, is as follows:-

a) Select 2mV/DIV.

b) Input + 3cm signal (as requested on screen).

c) If this signal is accurately +6mV, then press "Y" otherwise press "N" and enter the actual value by the keypad.

d) Reverse this signal – this must be done without introducing any d.c. offsets. So the best method is to exchange the input leads to the oscilloscope or (in the case of oscilloscope calibrator) select " – "

if this is sufficiently accurate (better than ±0.05%).

e) At this stage an ADC correction coefficient will have been calculated and displayed on the screen.

f) Input a ≈ 7½cm signal (as requested on screen).

g) Reverse this signal.

h) At this stage Y shift gain and offset correction coefficients will have been calculated and displayed on the screen.

i) Select the next attenuator range.

j) Repeat from d).

Thus, on each attenuator setting, ADC and Y shift correction coefficients are calculated.

On one range only (50mV/Div. unless only one attenuator setting is being calibrated) the invert offset coefficient is calculated and displayed. (This causes no change to the procedure).

At any time, "QUIT" can be pressed to abort the routine in which case those coefficients already calculated will not be lost.

If any calculation fails, "MAX" or "MIN" is displayed on the screen, as appropriate, and the user has the option of re-attempting the calibration procedure (because the failure could have been due to a user mistake), from the point where it failed. At all times, the user is directed by messages on the screen. The results are shown in the form of a table, as in Fig. 5.3.3. In each position in the table there can be displayed a number between +127 and −128 representing the calculated correction coefficient. If the calculation fails, "MAX" or "MIN" is displayed, in which case the hardware should be adjusted as detailed in section 5.3.1.

CALIBRATION TABLE

CH1 = 5mV/Div.

	GAIN	OFFSET
ADC	−43	...
Y SHIFT	104	−20
INVERT	...	17

Fig. 5.3.3 Vertical Software Calibration Results

5.3.2.5 x10 PROBE SOFTWARE CALIBRATION . (GENERAL MODE OPTIONS 53 and 54)

INTRODUCTION

They are used when the vertical software calibration is satisfactory (options 55 and 56) to bring the accuracy of the x10 probes used, to within the specified accuracy of the instrument. The results of this calibration are only used if the x10 probe options are selected (Vertical Mode, options 11 and 12).

OPERATION

To calibrate the CH1 x10 probe, select option 53. To calbrate the CH2 x10 probe, select option 54.

The procedure is somewhat similar to that described in 5.3.2.4. The equipment required (apart from the x10 probe) is a floating power supply capable of 0.1 to 100volts and a ±0.05% DVM, or an oscilloscope calibrator covering the same range. The calibration is performed on four attenuator settings (10mV/Div., 100mV/Div., 1V/Div., and 10V/Div.). On each of these settings the user is requested to supply a + 10 Div signal, followed by a request to reverse that signal (again a low D.C. offset is required between the original signal and its inverse). This signal is readily available from an oscilloscope calibrator, but if a power supply is used, the actual voltage may not be exactly that requested. If not, then the exact voltage must be input via the keypad, when requested.

After each pair of input signals, the routine calculates the correction coefficient and displays the results on the screen and then requests the next attenuator range. If the calculation is unsuccessful, "MAX" or "MIN" is displayed, implying that either the input signal was wrong, or the probe accuracy was outside ±3%. The user has the option of repeating the procedure, or pressing "QUIT" to abort.

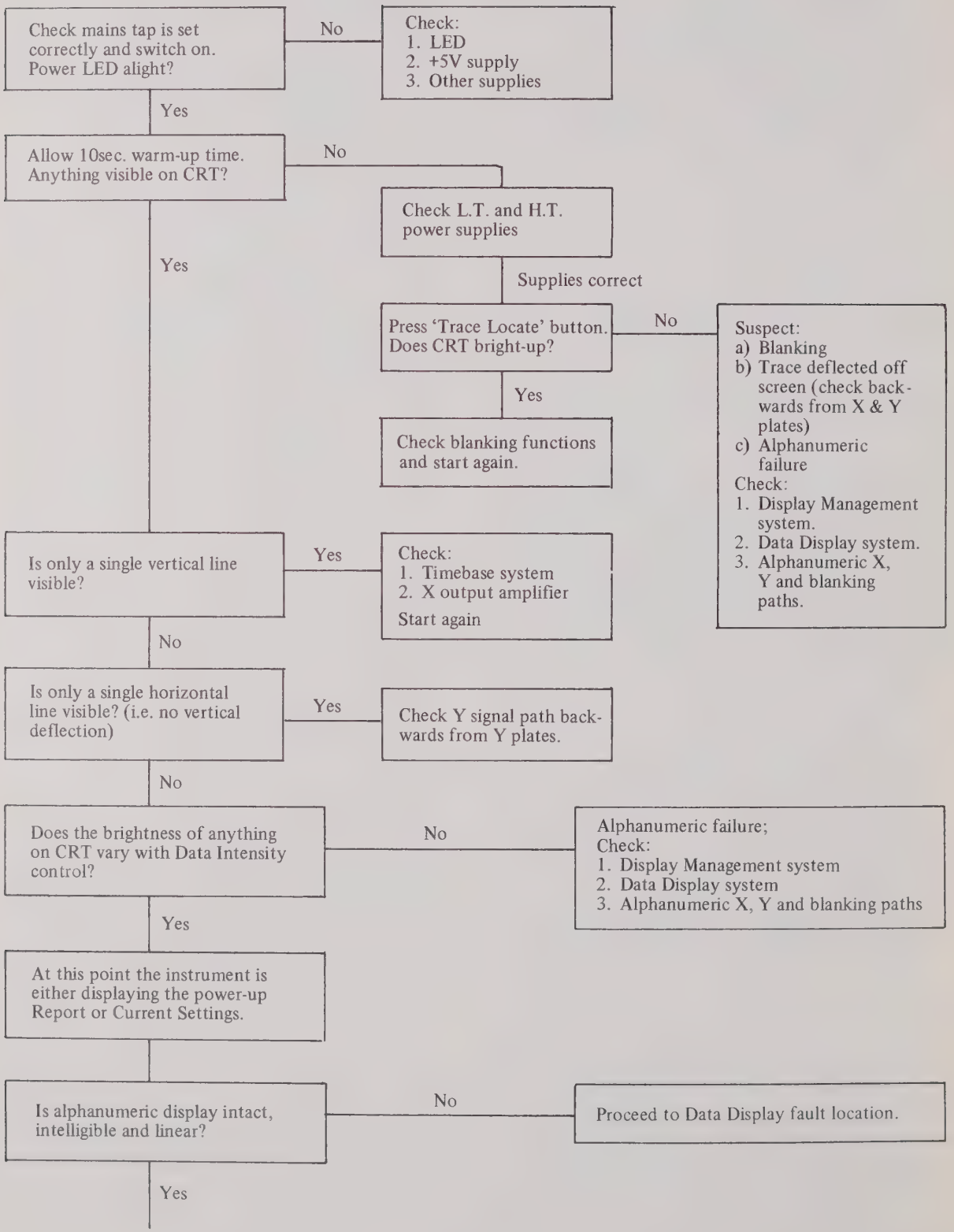
The number displayed on the screen is in the range +127 to −128 representing ±3% gain error in the probe.

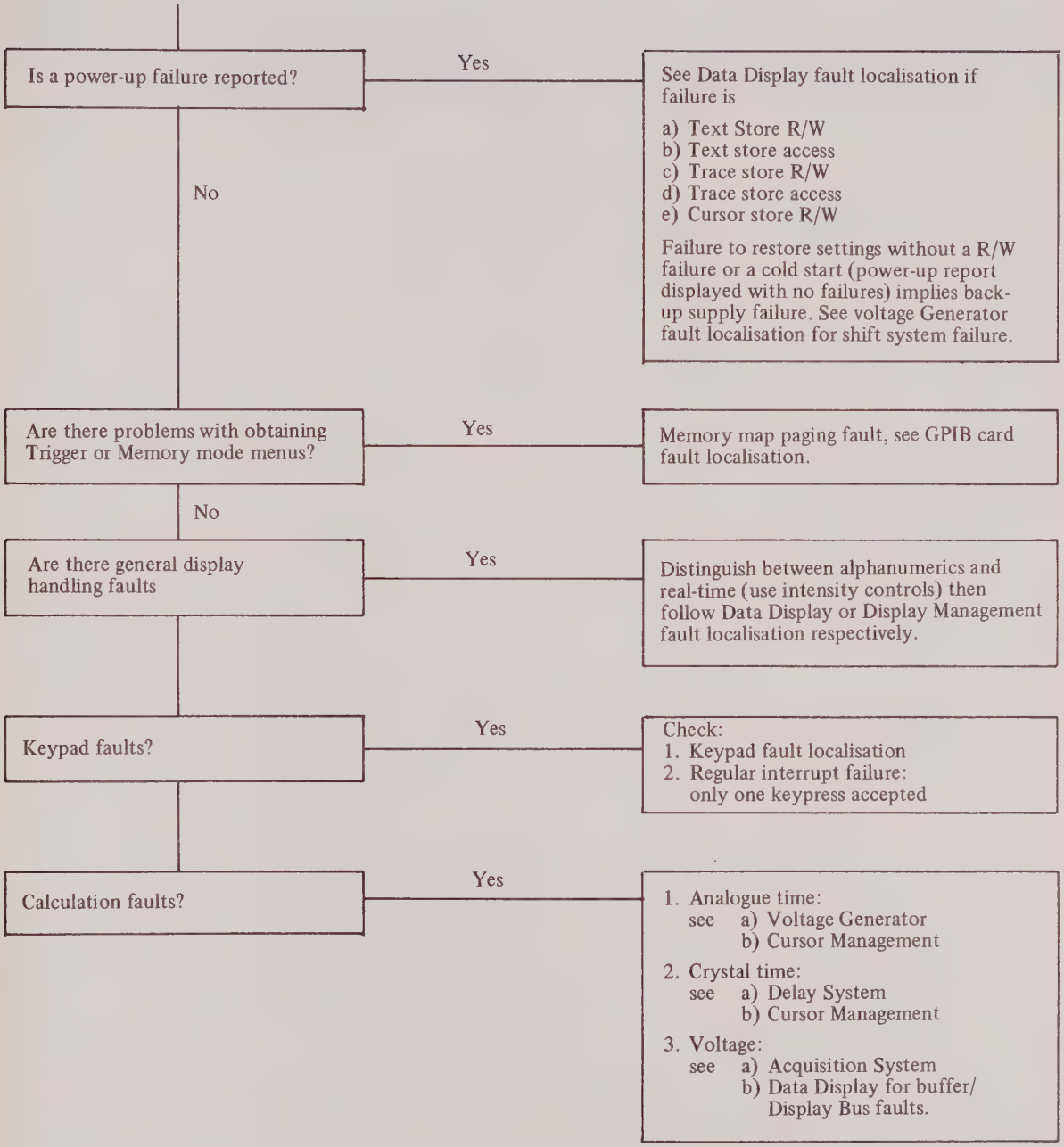
5.4 5110 FAULT LOCALISATION

5.4.1 OVERVIEW

The following flowchart should be used to localise the fault to a section covered in more detail in later sections. Obvious faults should be handled by moving directly to the appropriate flowchart or, if there is no flowchart, to the appropriate part of section 5.5.

5.4.1 OVERVIEW


Check mains tap is set correctly and switch on. Power LED alight?
No
Check:
1. LED
2. +5V supply
3. Other supplies
Yes
Allow 10sec. warm-up time. Anything visible on CRT?
No
Check L.T. and H.T. power supplies
Yes
Supplies correct
Press 'Trace Locate' button. Does CRT bright-up?
No
Suspect:
a) Blanking
b) Trace deflected off screen (check backwards from X & Y plates)
c) Alphanumeric failure
Check:
1. Display Management system.
2. Data Display system.
3. Alphanumeric X, Y and blanking paths.
Yes
Check blanking functions and start again.
Is only a single vertical line visible?
Yes
Check:
1. Timebase system
2. X output amplifier
Start again
No
Is only a single horizontal line visible? (i.e. no vertical deflection)
Yes
Check Y signal path backwards from Y plates.
No
Does the brightness of anything on CRT vary with Data Intensity control?
No
Alphanumeric failure;
Check:
1. Display Management system
2. Data Display system
3. Alphanumeric X, Y and blanking paths
Yes
At this point the instrument is either displaying the power-up Report or Current Settings.
Is alphanumeric display intact, intelligible and linear?
No
Proceed to Data Display fault location.
Yes

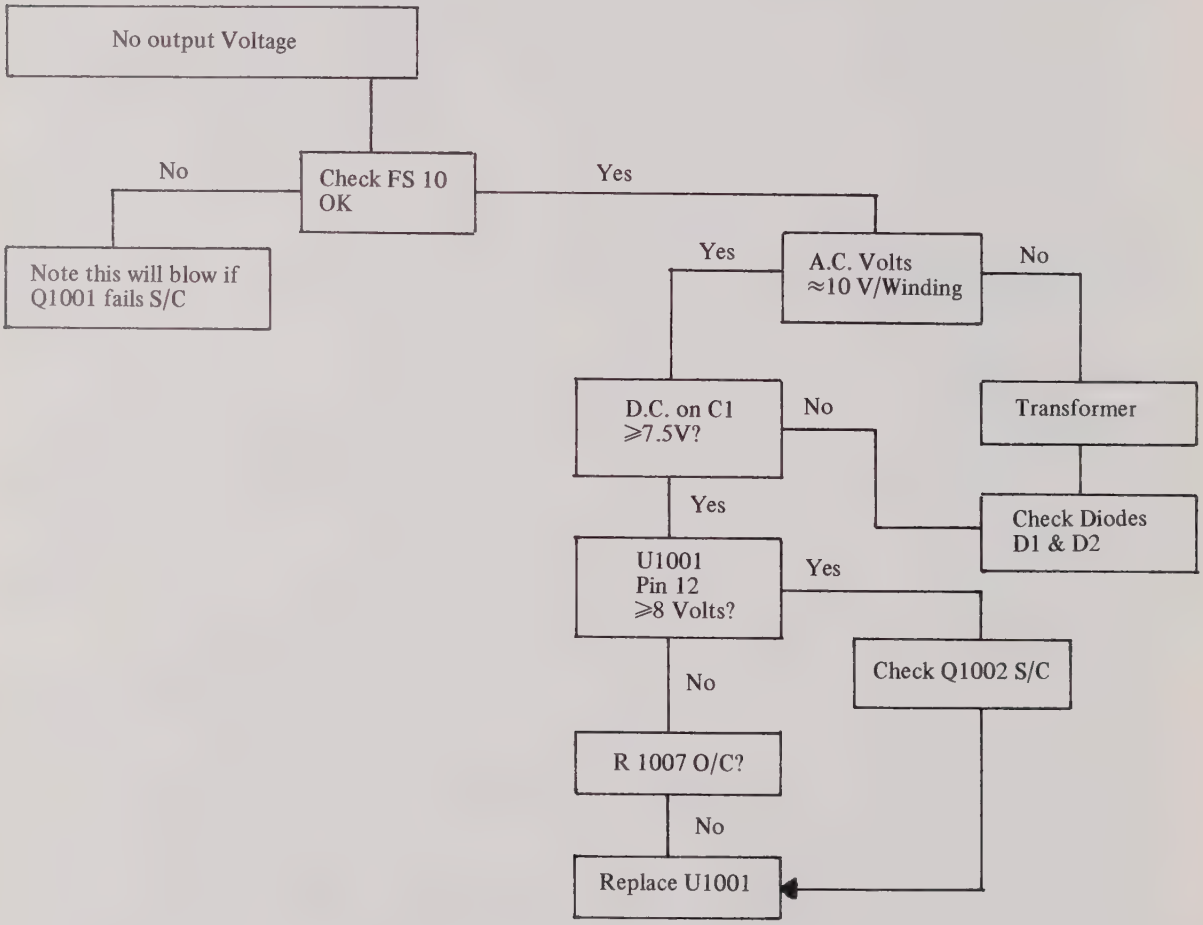

Is a power-up failure reported?
Yes
See Data Display fault localisation if failure is
a) Text Store R/W
b) Text store access
c) Trace store R/W
d) Trace store access
e) Cursor store R/W
Failure to restore settings without a R/W failure or a cold start (power-up report displayed with no failures) implies back-up supply failure. See voltage Generator fault localisation for shift system failure.
No
Are there problems with obtaining Trigger or Memory mode menus?
Yes
Memory map paging fault, see GPIB card fault localisation.
No
Are there general display handling faults
Yes
Distinguish between alphanumerics and real-time (use intensity controls) then follow Data Display or Display Management fault localisation respectively.
Keypad faults?
Yes
Check:
1. Keypad fault localisation
2. Regular interrupt failure: only one keypress accepted
Calculation faults?
Yes
1. Analogue time:
see a) Voltage Generator
b) Cursor Management
2. Crystal time:
see a) Delay System
b) Cursor Management
3. Voltage:
see a) Acquisition System
b) Data Display for buffer/ Display Bus faults.

5.4.2 POWER SUPPLY

Before any fault finding no component level is attempted, measurement at the power supply connectors, PLC or PLA should be made, as faults can often be traced to connections in the distribution network.

See Fig. 6.2.1 which should be helpful in diagnosis of the power supply is proved healthy.

+5 Volt Supply.



In normal use power supplies should not need to be adjusted having been set before leaving the factory.

Section 5.5.2 gives tolerance and measurement points for each supply.

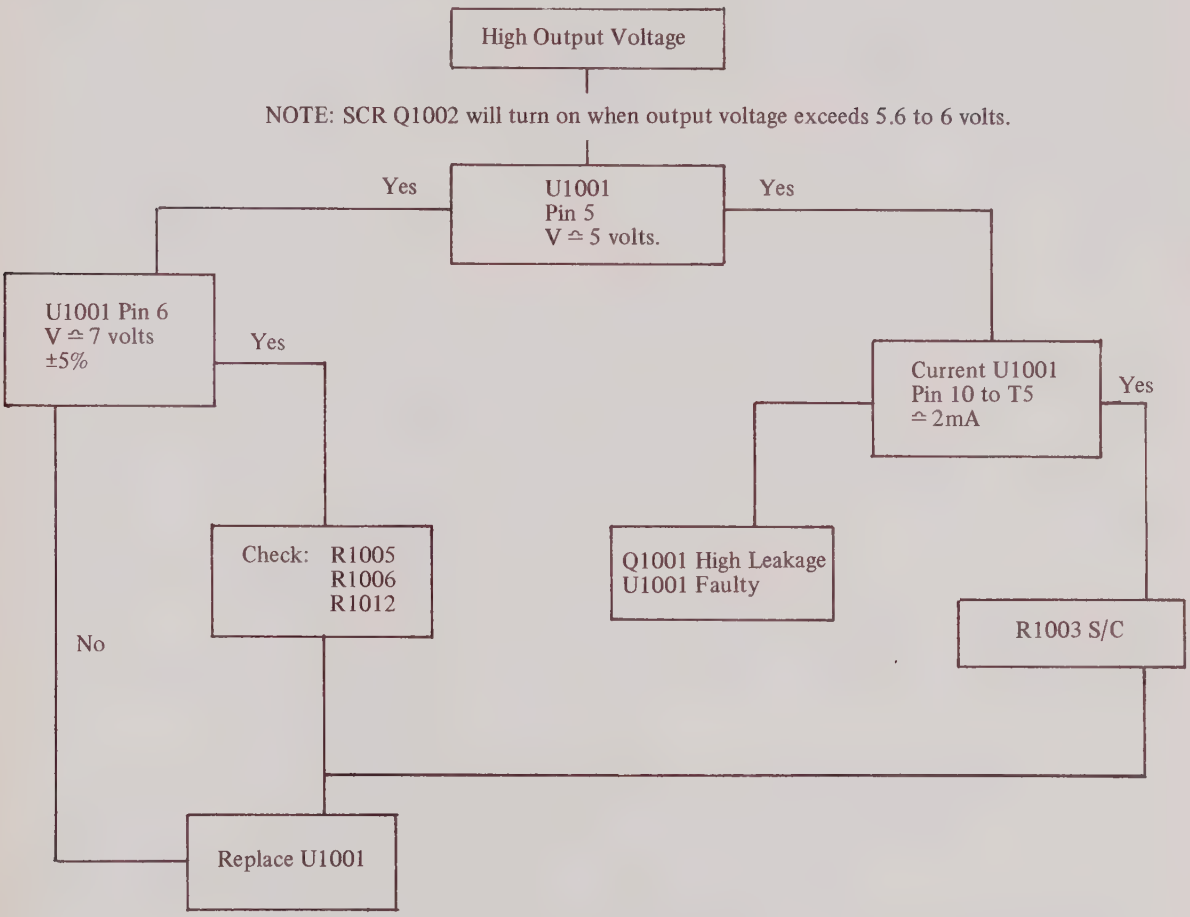
Should re-calibration of any supply be required, then removal of the false rear panels allows access through holes in the heat sink to adjustment potentiometers for the +5V −5V, +12V and −12 volt supplies. See Fig. 5.2.7.

CAUTION REMOVAL OF REAR PANEL EXPOSES MAINS INPUT VOLTAGE ON THERMAL SWITCH.

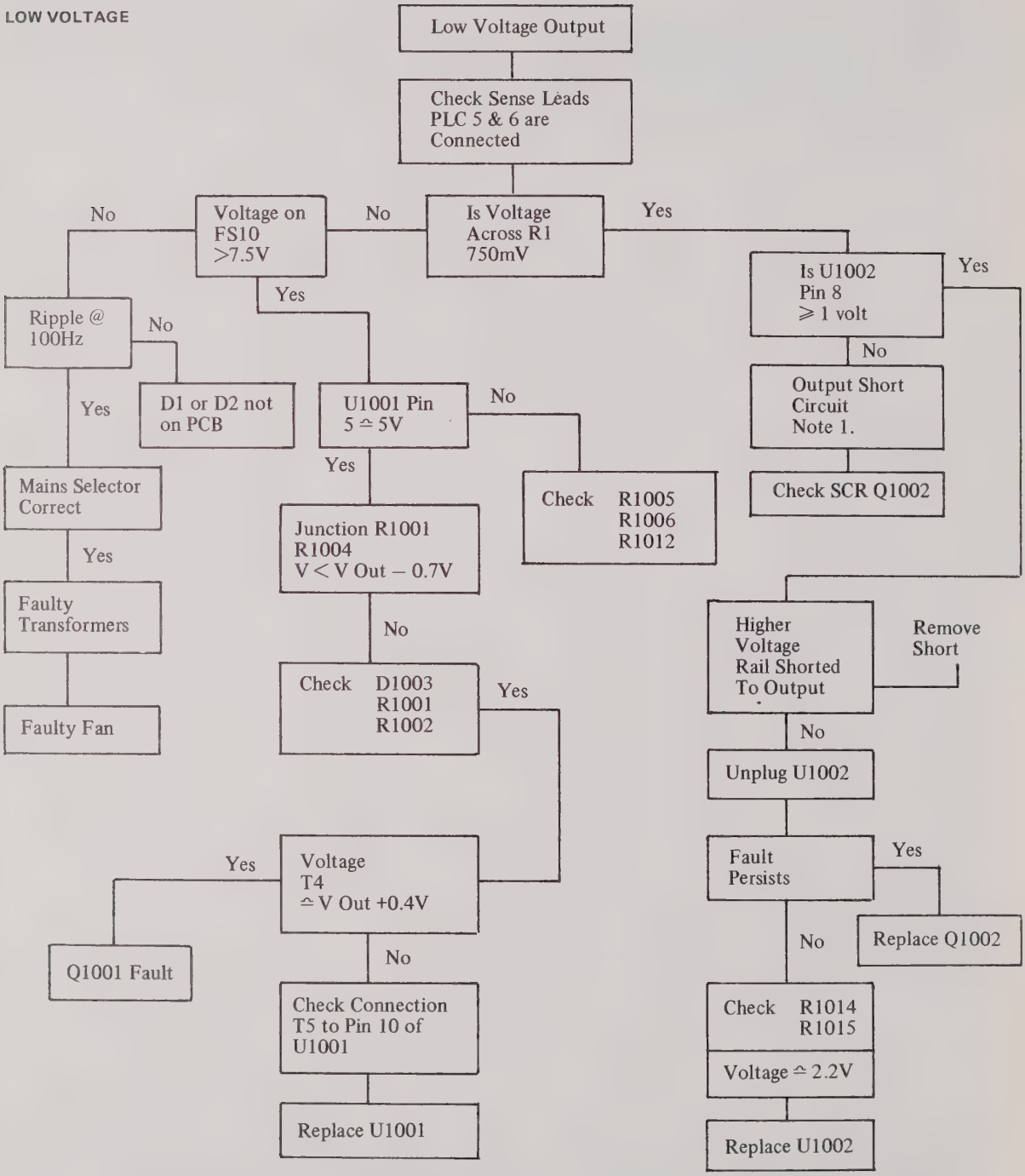
The +24V and +60 volt supplies are fixed. Any substantial variation found should be investigated as a potential fault condition.

Whenever the false rear panel is removed the opportunity should be taken to remove any accumulation of dust in this area, no attempt to oil the fan bearing should be made.

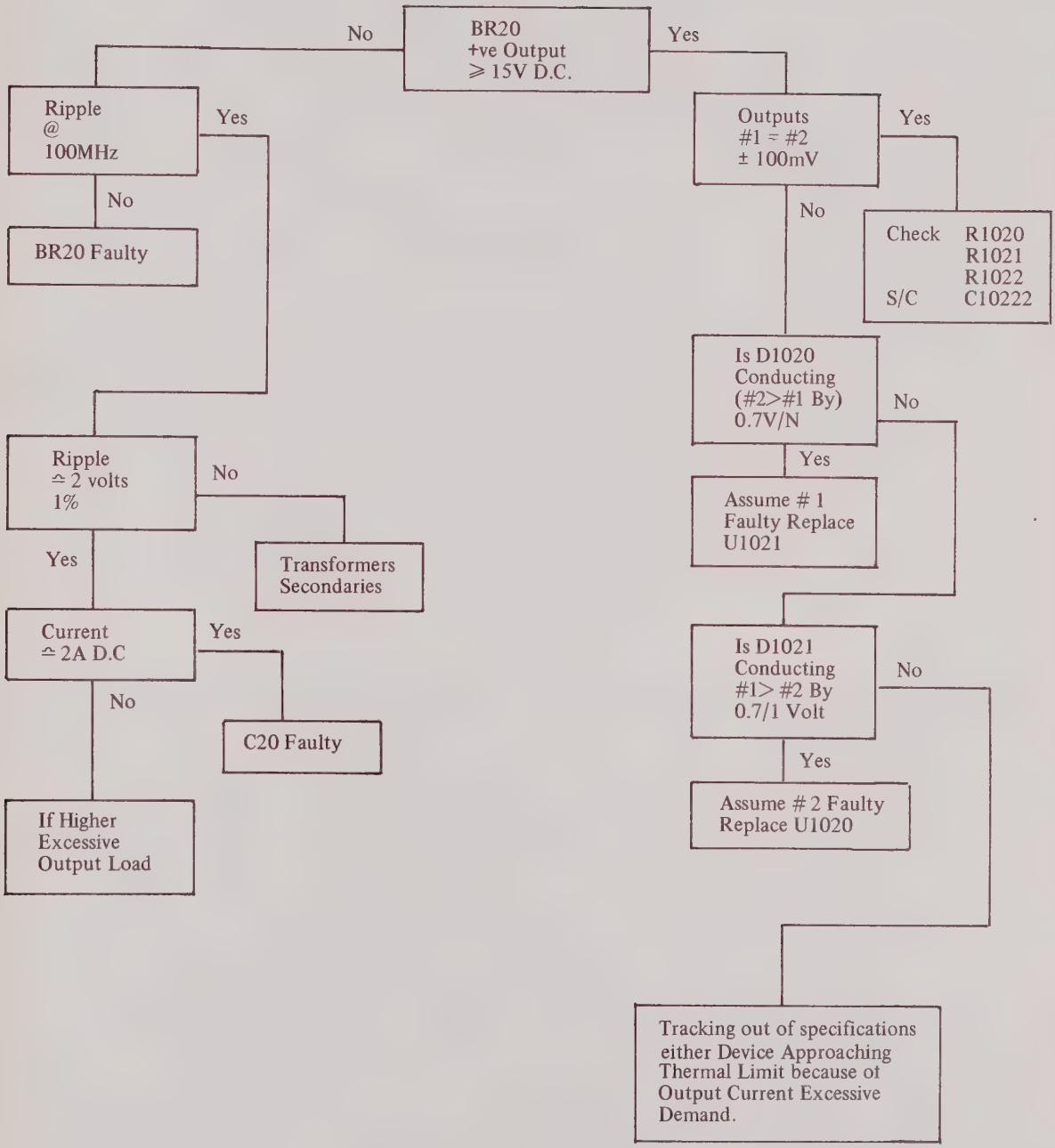
***NOTE 1**
Short Circuits remote from the power supply can cause high currents to flow in cableforms and the consequent output from the power supply need not be 0 volts, at the power supply output terminals.



LOW VOLTAGE


Low Voltage Output
Check Sense Leads PLC 5 & 6 are Connected
Is Voltage Across R1 750mV
No
Yes
Voltage on FS10 >7.5V
No
Yes
Ripple @ 100Hz
No
Yes
D1 or D2 not on PCB
Mains Selector Correct
Yes
Faulty Transformers
Faulty Fan
U1001 Pin 5 ≙ 5V
No
Yes
Check R1005 R1006 R1012
Junction R1001 R1004 V < V Out – 0.7V
No
Check D1003 R1001 R1002
Yes
Voltage T4 ≙ V Out +0.4V
Yes
Q1001 Fault
No
Check Connection T5 to Pin 10 of U1001
Replace U1001
Is U1002 Pin 8 ⩾ 1 volt
Yes
No
Output Short Circuit Note 1.
Check SCR Q1002
Higher Voltage Rail Shorted To Output
Remove Short
No
Unplug U1002
Fault Persists
Yes
No
Replace Q1002
Check R1014 R1015
Voltage ≙ 2.2V
Replace U1002

+12 VOLT SUPPLY

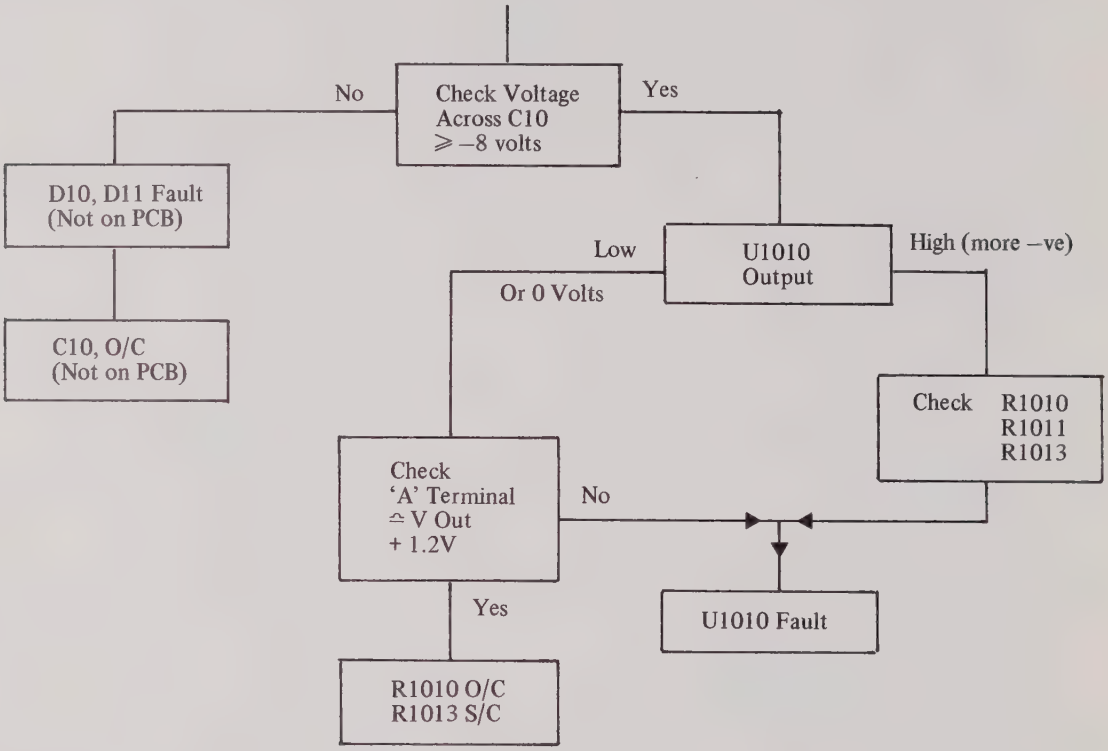


+12V SUPPLIES

Note that if a fault exists on either # 1 or # 2 supply then diodes D1020 or D1021 will conduct. This will tend to mask the fault as one device might well supply the necessary current without going into thermal limit.

–5 VOLT SUPPLY

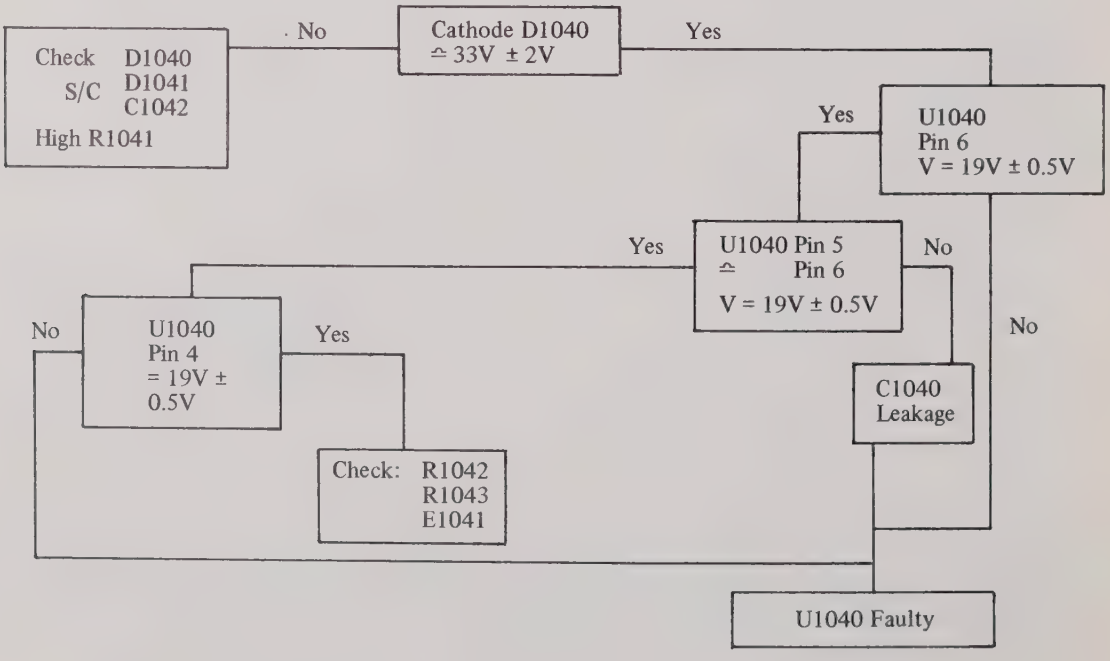
This supply will not give the correct output if D1 or D2 are faulty (+5V)



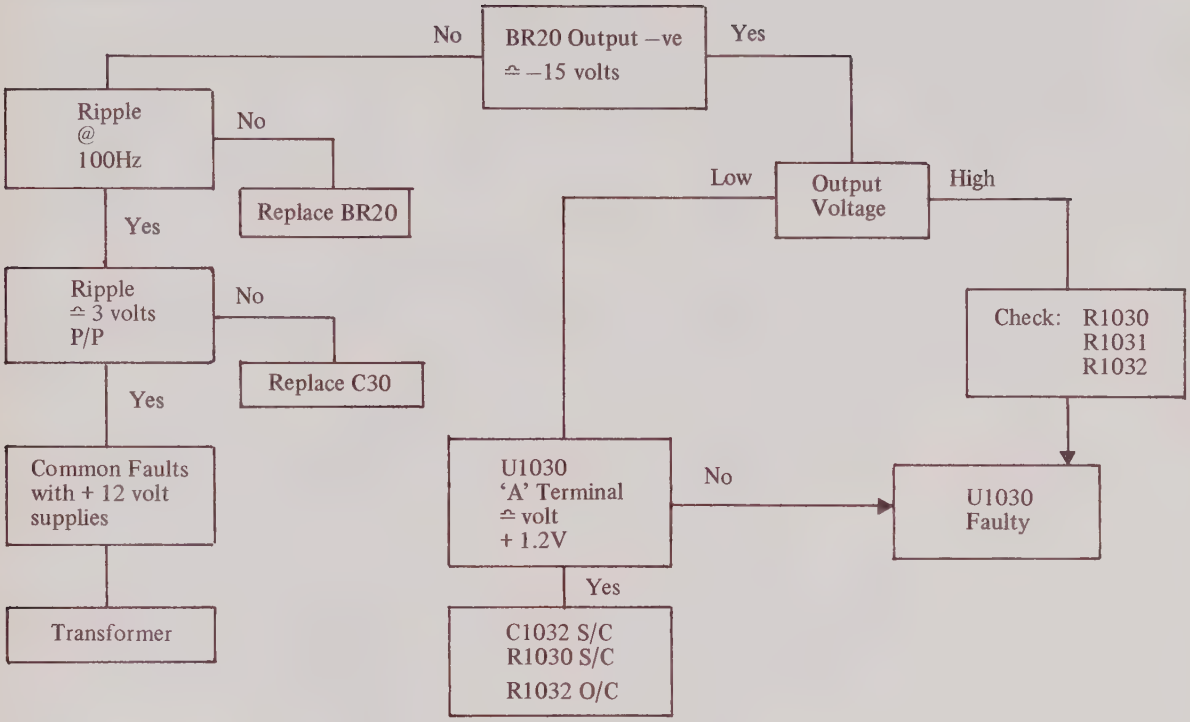
+24 VOLT SUPPLY

Note this supply will only give the correct voltage if the following conditions are met:-

1. + 60V supply is substantially working i.e. within ±10 volts.
2. + 12V # 2 is ± 1%



–12 VOLT SUPPLY



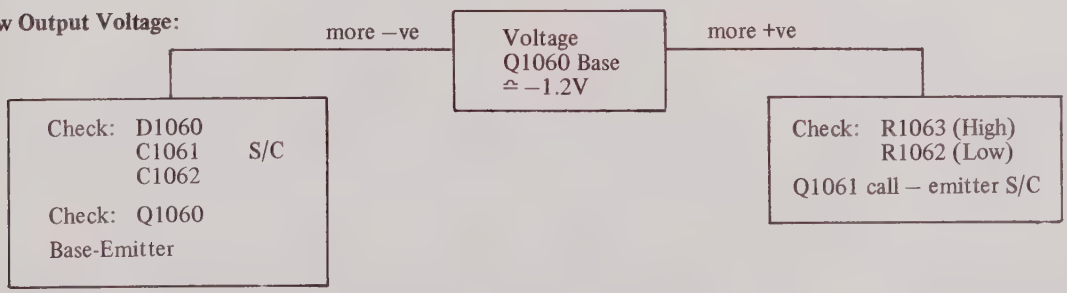
+60 VOLT (±120 VOLTS)

The + 5 volt and – 12 volt supplies must be operating correctly for this stabilizer to function:

No Output:

Check: FS 1050
D 1050 O/C
D 1056
D 1057

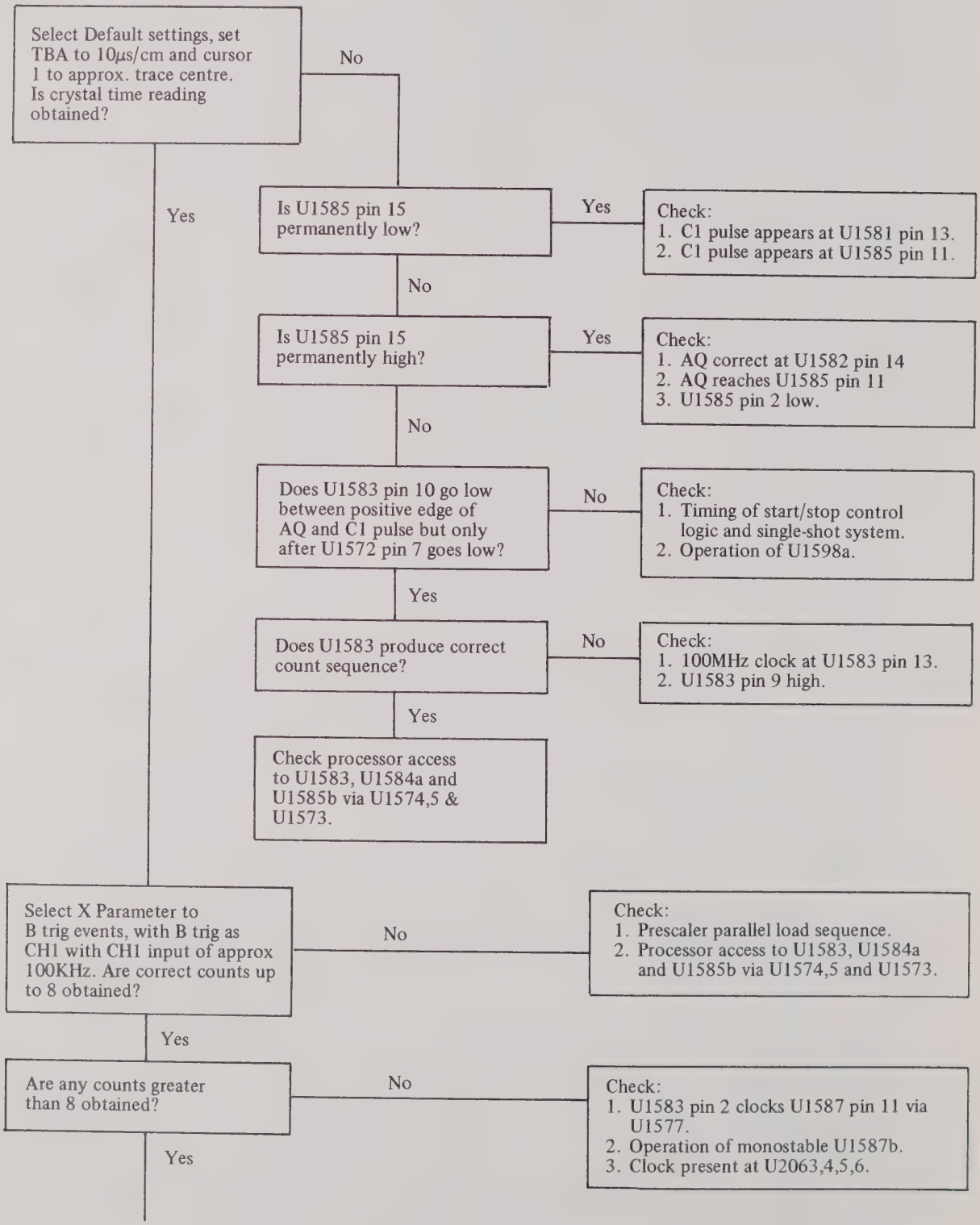
Low Output Voltage:



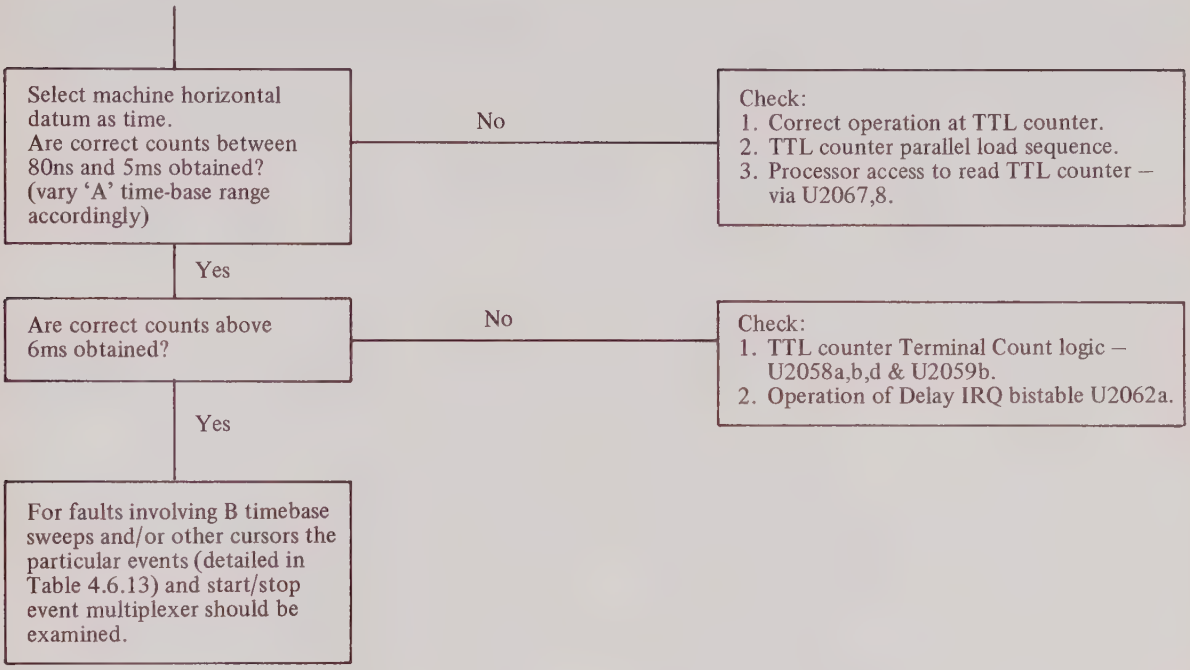
Uncontrolled or High Output:

Check: D1058 S/C
D1061 S/C
Q1060 C/e or C/b S/c
Q1061 b/e or c/e
D1062 o/c
R1062 High
R1063 Low

5.4.3 TIME/EVENT MEASUREMENT SYSTEM


Select Default settings, set TBA to 10μs/cm and cursor 1 to approx. trace centre. Is crystal time reading obtained?
No
Yes
Is U1585 pin 15 permanently low?
Yes
Check:
1. C1 pulse appears at U1581 pin 13.
2. C1 pulse appears at U1585 pin 11.
No
Is U1585 pin 15 permanently high?
Yes
Check:
1. AQ correct at U1582 pin 14
2. AQ reaches U1585 pin 11
3. U1585 pin 2 low.
No
Does U1583 pin 10 go low between positive edge of AQ and C1 pulse but only after U1572 pin 7 goes low?
No
Check:
1. Timing of start/stop control logic and single-shot system.
2. Operation of U1598a.
Yes
Does U1583 produce correct count sequence?
No
Check:
1. 100MHz clock at U1583 pin 13.
2. U1583 pin 9 high.
Yes
Check processor access to U1583, U1584a and U1585b via U1574,5 & U1573.
Select X Parameter to B trig events, with B trig as CH1 with CH1 input of approx 100KHz. Are correct counts up to 8 obtained?
No
Check:
1. Prescaler parallel load sequence.
2. Processor access to U1583, U1584a and U1585b via U1574,5 and U1573.
Yes
Are any counts greater than 8 obtained?
No
Check:
1. U1583 pin 2 clocks U1587 pin 11 via U1577.
2. Operation of monostable U1587b.
3. Clock present at U2063,4,5,6.
Yes

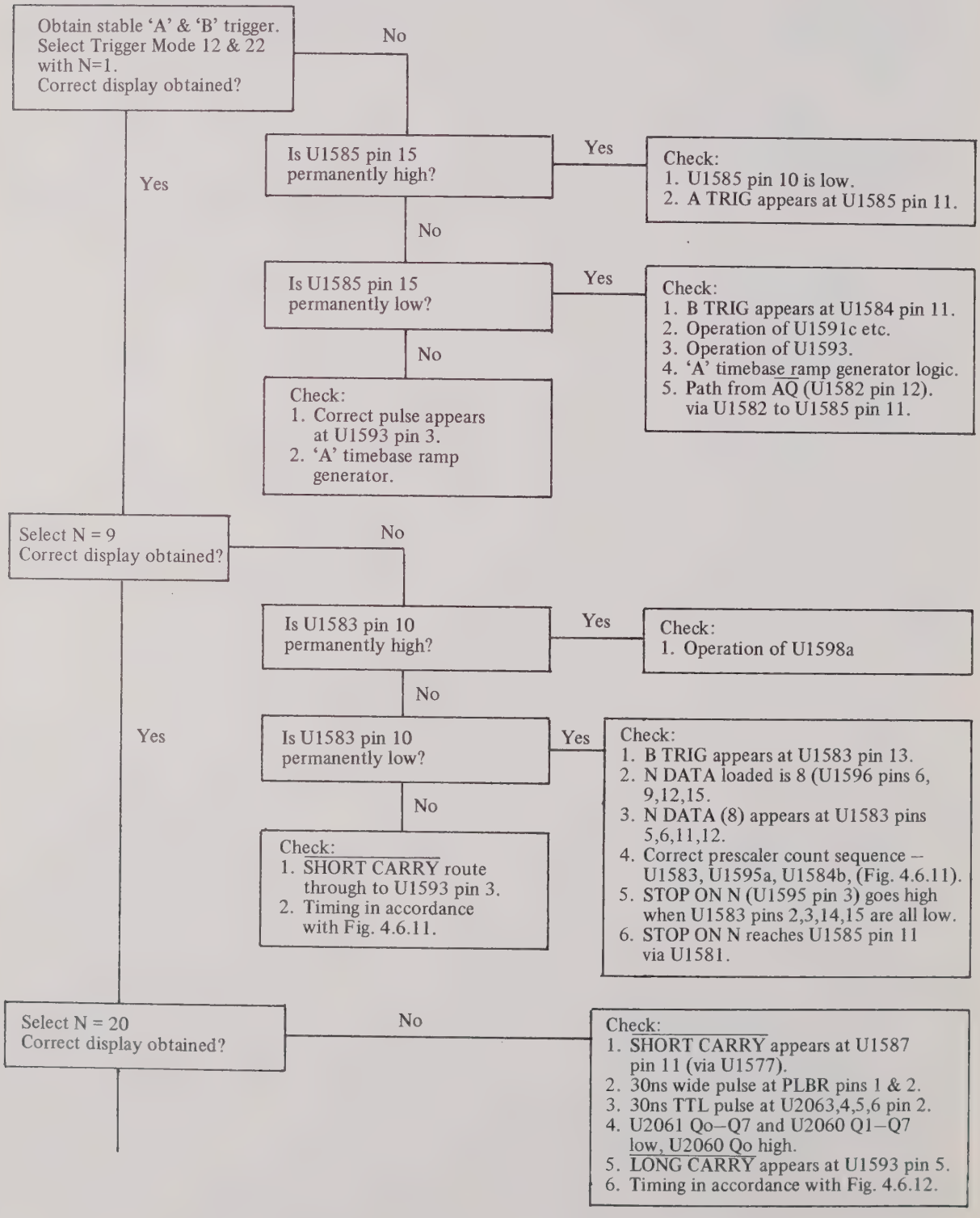
TIME/EVENT MEASUREMENT SYSTEM (Cont)

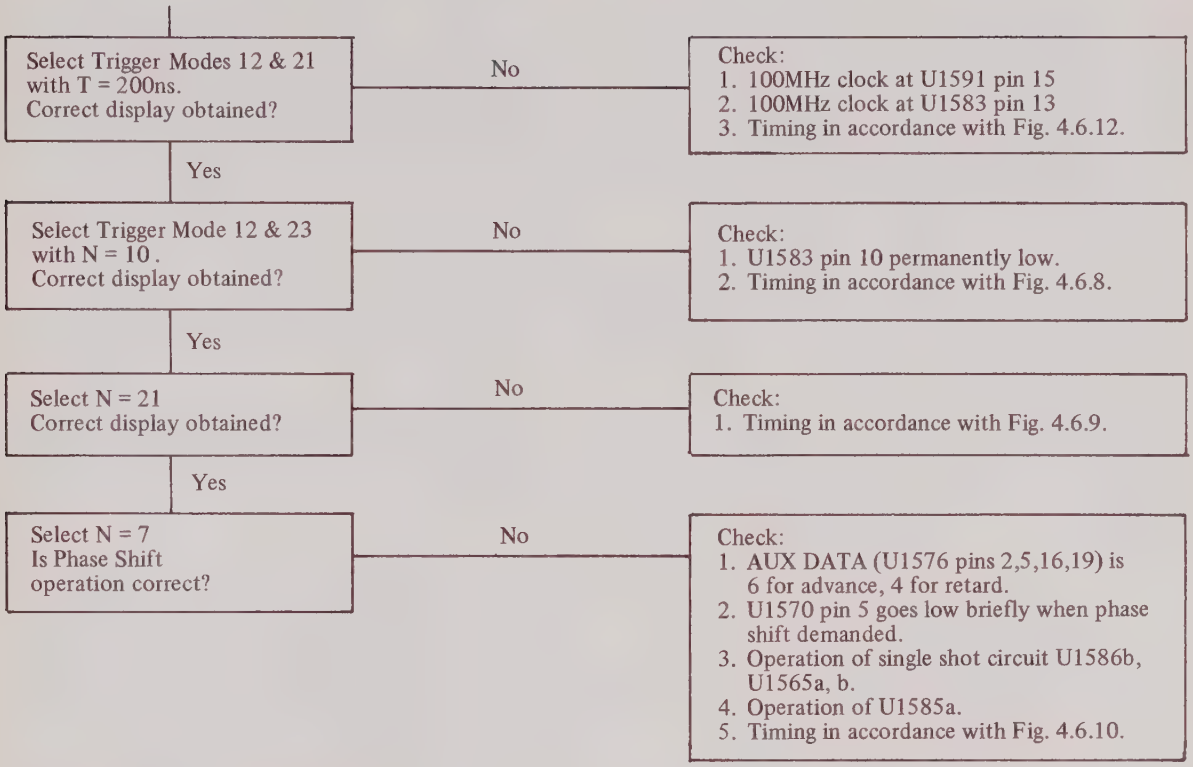

Select machine horizontal datum as time.
Are correct counts between 80ns and 5ms obtained? (vary 'A' time-base range accordingly)
No
Check:
1. Correct operation at TTL counter.
2. TTL counter parallel load sequence.
3. Processor access to read TTL counter – via U2067,8.
Yes
Are correct counts above 6ms obtained?
No
Check:
1. TTL counter Terminal Count logic – U2058a,b,d & U2059b.
2. Operation of Delay IRQ bistable U2062a.
Yes
For faults involving B timebase sweeps and/or other cursors the particular events (detailed in Table 4.6.13) and start/stop event multiplexer should be examined.

TRIGGER MODE FAULT LOCALISATION

In the following flow chart, operation of the Delay System control/counting system is emphasised for 'A' timebase trigger modes whilst the programmable nature of the 'B' trigger modes is covered without direct reference to counting details. For 'B' trigger mode faults the reader is advised to ascertain whether an equivalent (simpler) fault exists for 'A' timebase.

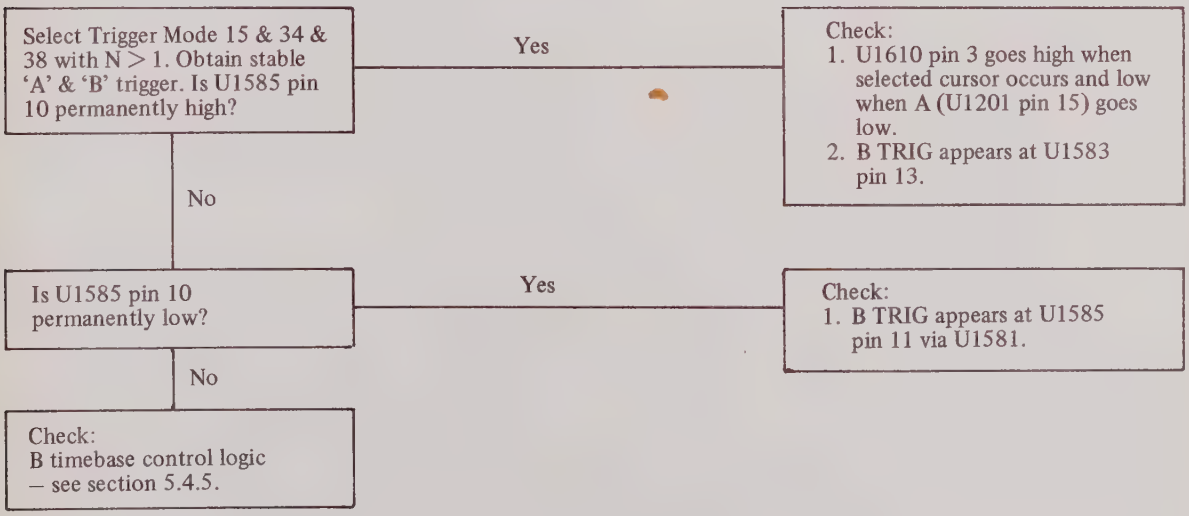
'A' TRIGGER MODE FAULT LOCALISATION


Obtain stable 'A' & 'B' trigger. Select Trigger Mode 12 & 22 with N=1. Correct display obtained?
No
Yes
Is U1585 pin 15 permanently high?
Yes
Check: 1. U1585 pin 10 is low. 2. A TRIG appears at U1585 pin 11.
No
Is U1585 pin 15 permanently low?
Yes
Check: 1. B TRIG appears at U1584 pin 11. 2. Operation of U1591c etc. 3. Operation of U1593. 4. 'A' timebase ramp generator logic. 5. Path from AQ (U1582 pin 12). via U1582 to U1585 pin 11.
No
Check: 1. Correct pulse appears at U1593 pin 3. 2. 'A' timebase ramp generator.
Select N = 9 Correct display obtained?
No
Yes
Is U1583 pin 10 permanently high?
Yes
Check: 1. Operation of U1598a
No
Is U1583 pin 10 permanently low?
Yes
Check: 1. B TRIG appears at U1583 pin 13. 2. N DATA loaded is 8 (U1596 pins 6, 9,12,15. 3. N DATA (8) appears at U1583 pins 5,6,11,12. 4. Correct prescaler count sequence – U1583, U1595a, U1584b, (Fig. 4.6.11). 5. STOP ON N (U1595 pin 3) goes high when U1583 pins 2,3,14,15 are all low. 6. STOP ON N reaches U1585 pin 11 via U1581.
No
Check: 1. SHORT CARRY route through to U1593 pin 3. 2. Timing in accordance with Fig. 4.6.11.
Select N = 20 Correct display obtained?
No
Check: 1. SHORT CARRY appears at U1587 pin 11 (via U1577). 2. 30ns wide pulse at PLBR pins 1 & 2. 3. 30ns TTL pulse at U2063,4,5,6 pin 2. 4. U2061 Qo–Q7 and U2060 Q1–Q7 low, U2060 Qo high. 5. LONG CARRY appears at U1593 pin 5. 6. Timing in accordance with Fig. 4.6.12.


Select Trigger Modes 12 & 21 with T = 200ns. Correct display obtained?
No
Check:
1. 100MHz clock at U1591 pin 15
2. 100MHz clock at U1583 pin 13
3. Timing in accordance with Fig. 4.6.12.
Yes
Select Trigger Mode 12 & 23 with N = 10. Correct display obtained?
No
Check:
1. U1583 pin 10 permanently low.
2. Timing in accordance with Fig. 4.6.8.
Yes
Select N = 21 Correct display obtained?
No
Check:
1. Timing in accordance with Fig. 4.6.9.
Yes
Select N = 7 Is Phase Shift operation correct?
No
Check:
1. AUX DATA (U1576 pins 2,5,16,19) is 6 for advance, 4 for retard.
2. U1570 pin 5 goes low briefly when phase shift demanded.
3. Operation of single shot circuit U1586b, U1565a, b.
4. Operation of U1585a.
5. Timing in accordance with Fig. 4.6.10.

'B' TRIGGER MODE FAULT LOCALISATION

The following flow chart is for Trigger Mode 15, 34 N> 1, this being one of the more complex modes. For other modes careful reference should be made to Table 4.6.14. for precise parameters with relevant descriptions appearing in section 4.6.2.


Select Trigger Mode 15 & 34 & 38 with N > 1. Obtain stable 'A' & 'B' trigger. Is U1585 pin 10 permanently high?
Yes
Check:
1. U1610 pin 3 goes high when selected cursor occurs and low when A (U1201 pin 15) goes low.
2. B TRIG appears at U1583 pin 13.
No
Is U1585 pin 10 permanently low?
Yes
Check:
1. B TRIG appears at U1585 pin 11 via U1581.
No
Check:
B timebase control logic – see section 5.4.5.

For faults in other modes (but not 'A' trigger modes) particular Start/stop/qualification events should be suspected – e.g. inputs to U1581, 2 and routing to U1585 pin 11 via U1581,2.

5.4.4 CURSOR GENERATION AND CONTROL

CURSOR GENERATORS

Each of the four generators are an identical circuit, only one will be described. Cursor 1, generated by U1631. For cursors 2,3 and 4 substitute U1641,51 and 61 respectively, with components 1640+, 50+ and 60+. Set the instrument as for the cursor fault finding chart listed below.

It should now be possible to individually engage each cursor and produce an on-screen bright up of approximately 1mm trace length. Also invoked should be a current cursor reading of voltage and time (X parameter). The cursor should be traversed across the full screen width to ensure this is the case for all ramp voltages.

Note: If a generator fails with output low then a bright up will be caused for the whole of a trace; and this will obscure any other cursor bright up, although these cursors are functional.

Waveform A should be present on all cursor outputs (pin 4).

Waveform B (selected ramp) should be present on pin 2 and 11 of all comparators.

There should be approx. 40mV D.C. across R32 at all times, junction with R33 more positive.

CURSOR FAULT FINDING CHART

To use the chart below, first set the oscilloscope to the following state:-

S5 MEMORY MODE
01 STORE 1 OFF
02 STORE 2 OFF

S8 VERTICAL MODE
01 CH1 ONLY

S9 TRIGGER MODE
01 NORMAL
11 A TRIGGER SOURCE: TRIGGER
13 CURSOR
31 A START

S7 HORIZONTAL MODE
01 A TIMEBASE ONLY

11 x 10 EXPANSION B1 OFF
06 ENABLE B1 OFF
07 ENABLE B3 OFF

'QUIT' TO MIXED MODE.

Set A Timebase to 10ms/cm.

B Timebase to 1ms/cm.

Select trigger source for A timebase and provide a repetitive signal.

To avoid any ambiguity on the first test, activate only one cursor at a time. Note that the short-form notation "*" has been used to indicate the node found in all paths, the following number refers to a specific cursor: e.g. *2 to cursor 2 etc. (see Fig. 4.7.1) for nodes and Fig. 5.4.1 for waveforms.

TEST 1. Activate each cursor in turn, de-activate all other cursors, and observe the waveforms indicated on the appropriate row of the figure below at the particular node shown each row. i.e. waveform 1 at node 6 for all cursors.

	NODE					
CURSOR	$\overline{*}$	$\overline{*}$	5	6	7	8
1	1	2	hi	1	2	hi
2	1	2	hi	1	2	hi
3	1	2	hi	1	2	hi
4	1	2	hi	1	2	hi

As the cursor management circuitry consists almost entirely of combinational logic, any failure identified at this stage can be pin-pointed easily be checking the selector gate enabling etc.

TEST 2. Permanently activate cursor 1, and select 06 ENABLE B1 ON. Change the HORIZONTAL MODE to 03 A alt. B. Each cursor should now be activated, to the exclusion of any others, except of course cursor 1 permanently enabled. As before in TEST 1, waveform are given at the appropriate NODE (ROW) tabulated against CURSOR (COLUMNS).

	NODE					
CURSOR	$\overline{*}$	$\overline{*}$	5	6	7	8
2	3	4	2	5	4	6
3	1	2	2	7	2	6
4	3	4	2	5	4	6

Note that on this configuration the cursors are paired, cursors 1 and 3 on A ramp, with bright up in A, and cursor 2 with cursor 4 on B. A failure to conform to the waveforms given should be noted, but if the whole table is completed the cause of faults often becomes very apparent.

TEST 3. Change the mode of operation to DUAL CHANNEL (press SHIFT for CH2). This should result in two phases, one for each Y channel, qualifiers received by U1612 becoming active. The cursors should now appear as shown below:-

C1 and C2 on CH1; C2 in B ramp.

C3 and C4 on CH2; C4 in B ramp.

The only node affected by the change of mode is tabulated below.

CURSOR	NODE 6	
2	10	N.B. all other nodes
3	11	remain as in
4	12	fig . . . . .

TEST 4. If the HORIZONTAL MODE: ENABLE B3 ON (07) is activated, B ramp will now start alternately from two different points in A ramp, one set by C1, the other by C3. Note that cursor 4 will only appear when C3 is active. Both node 6 and node 8 will produce different waveforms from TEST 2 (or 3) all other nodes remain the same.

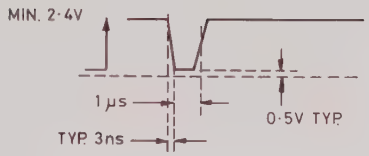
ALL CURSORS ACTIVE

CURSOR	NODE 6	NODE 8
1,2,3,4	13	14

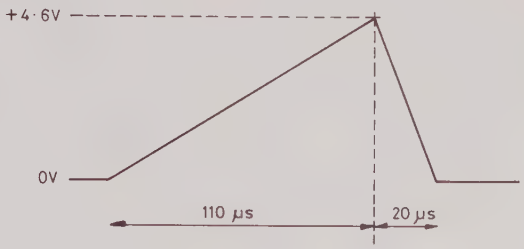
WAVEFORMS

All waveforms shown are at ecl logic levels, with ecl powered from +5V. This gives an ecl hi ≙+4V, ecl to ≙+3V.

WAVEFORM A.



B. SELECTED RAMP – TYPICAL A RAMP SHOWN



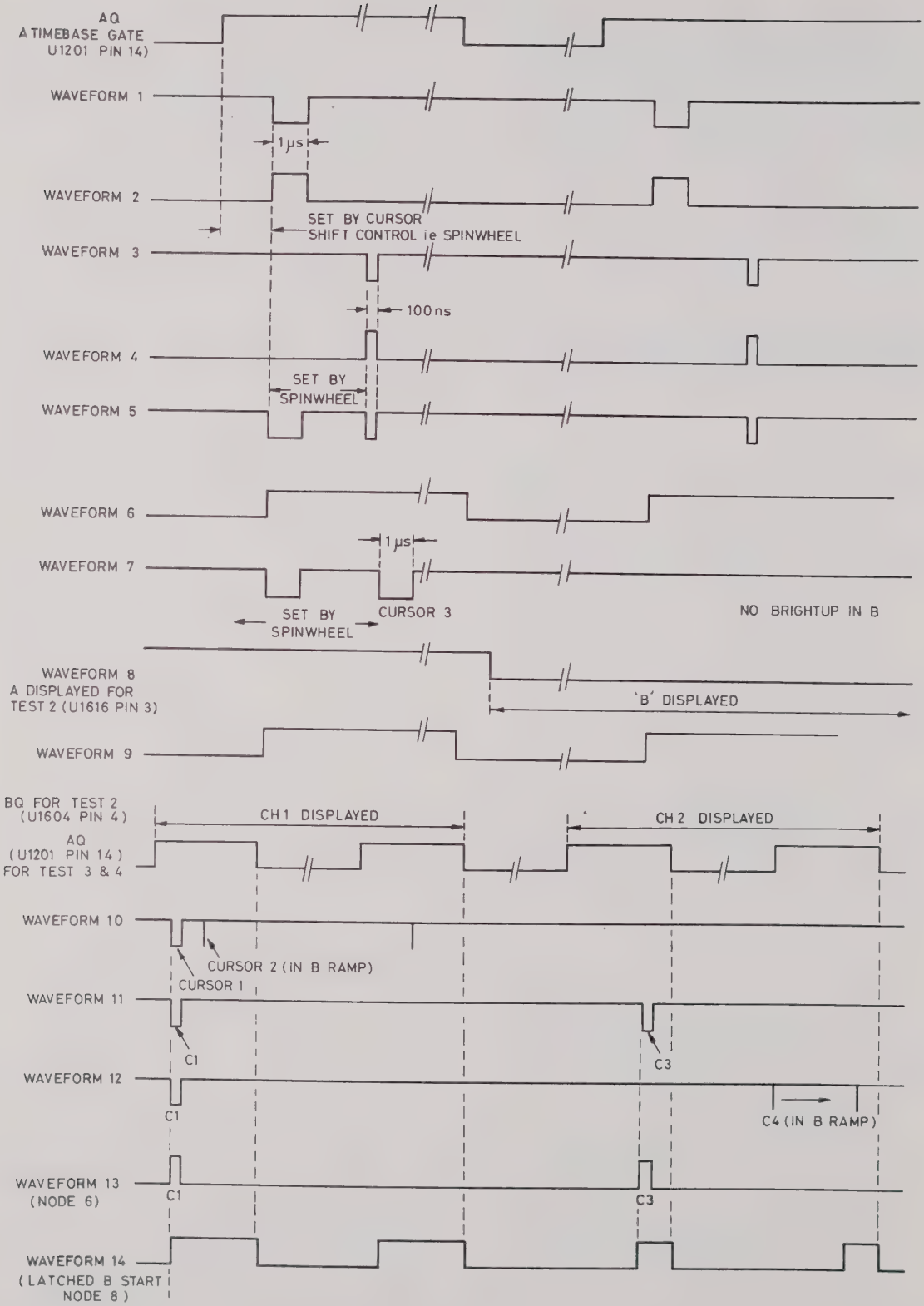
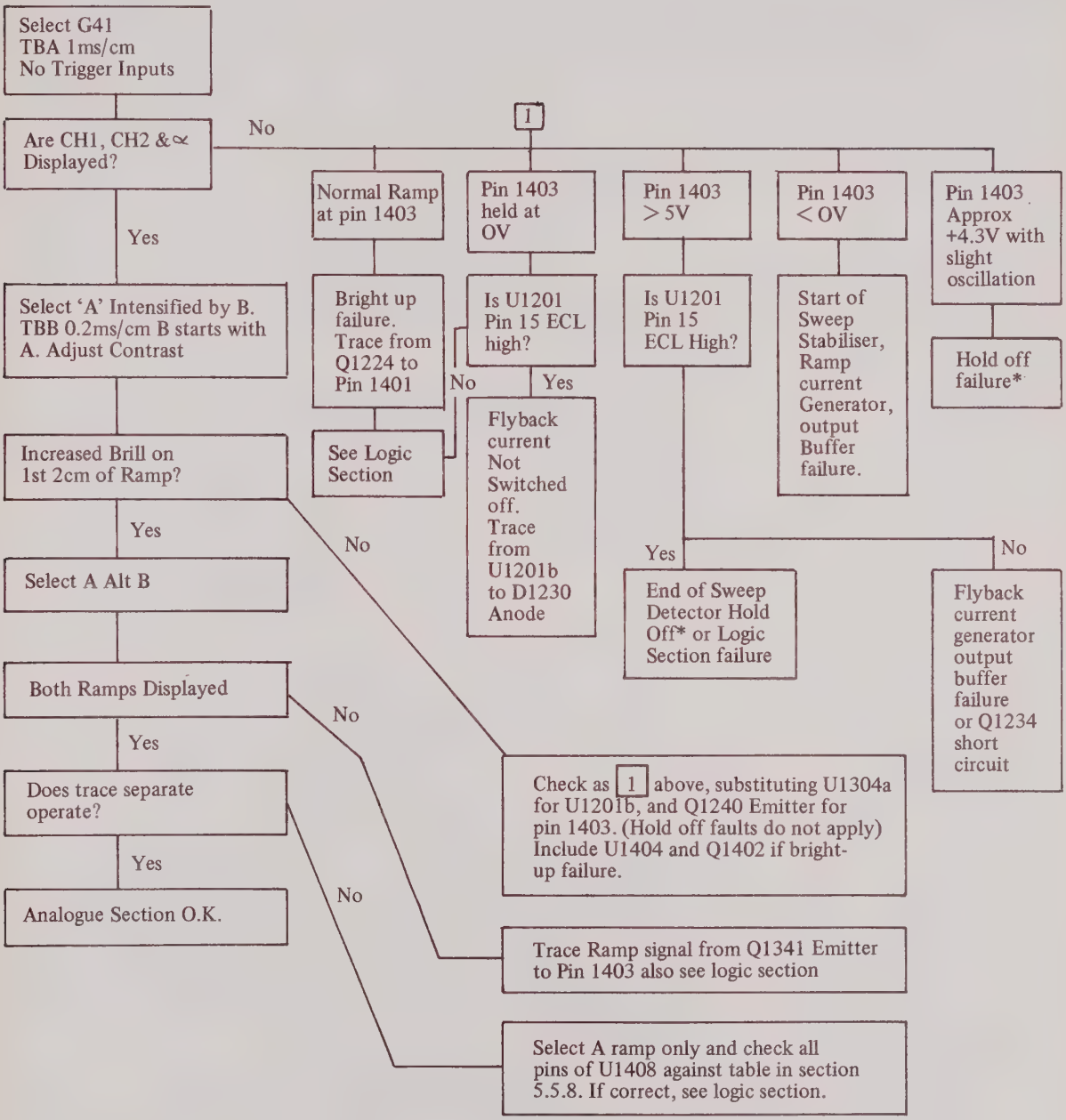


Fig. 5.4.1 Cursor Faultfinding, Tabulated Waveforms

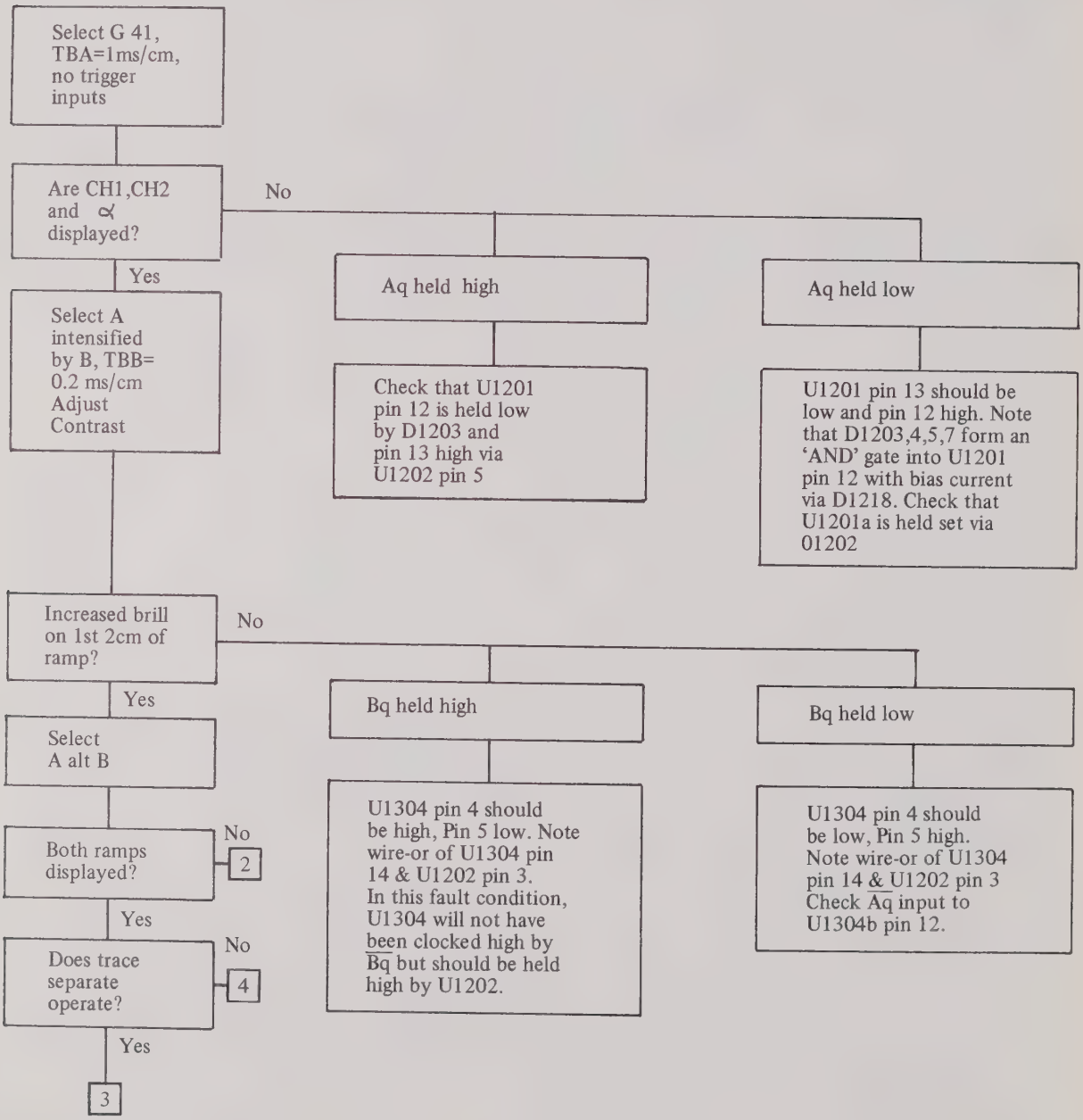
5.4.5 TIMEBASE ANALOGUE SECTION

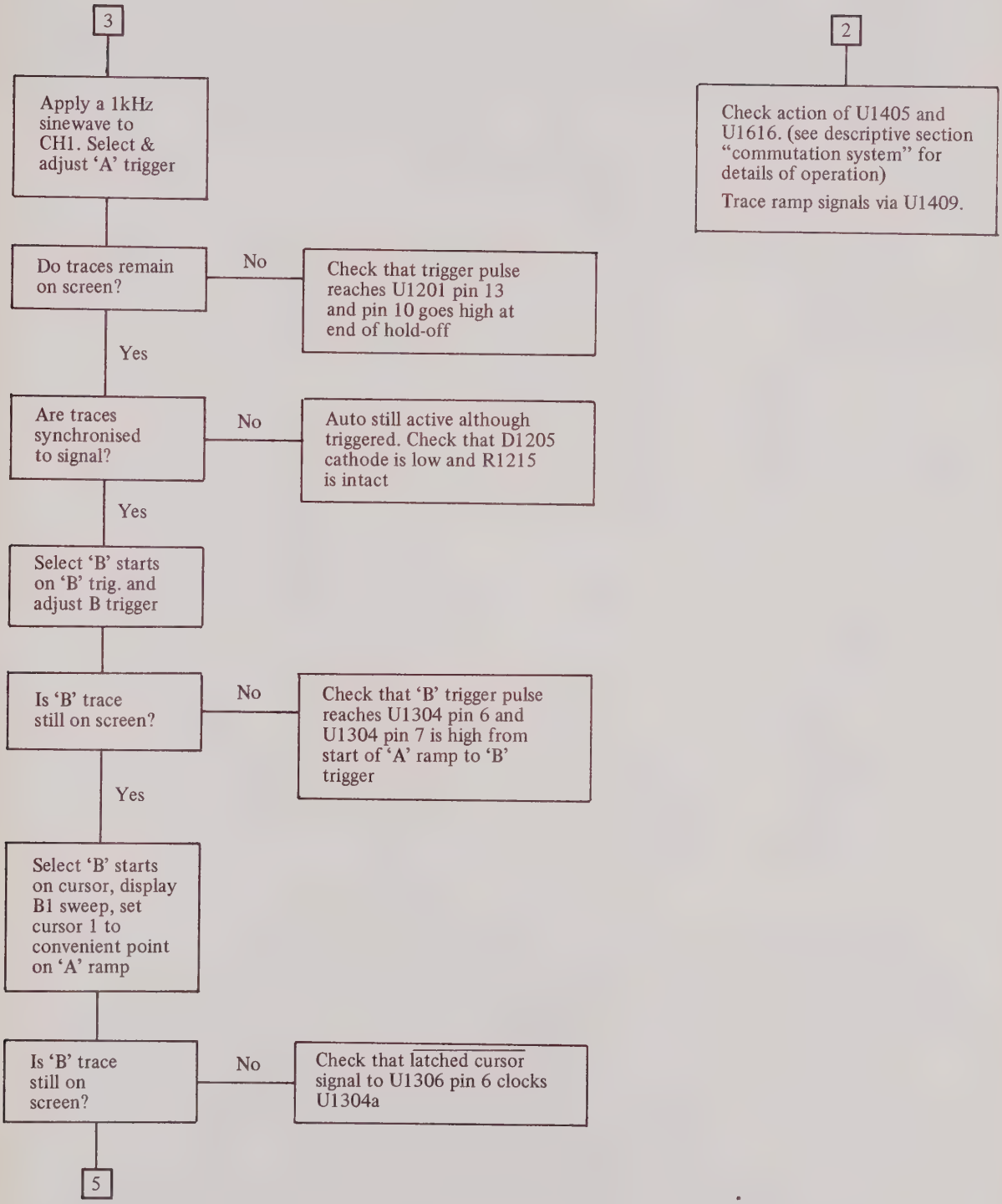

Select G41
TBA 1ms/cm
No Trigger Inputs
Are CH1, CH2 & ∝ Displayed?
No
Yes
1
Normal Ramp at pin 1403
Pin 1403 held at OV
Pin 1403 > 5V
Pin 1403 < OV
Pin 1403 Approx +4.3V with slight oscillation
Select 'A' Intensified by B. TBB 0.2ms/cm B starts with A. Adjust Contrast
Bright up failure. Trace from Q1224 to Pin 1401
Is U1201 Pin 15 ECL high?
Is U1201 Pin 15 ECL High?
Start of Sweep Stabiliser, Ramp current Generator, output Buffer failure.
Hold off failure*
No
Yes
Flyback current Not Switched off. Trace from U1201b to D1230 Anode
See Logic Section
Increased Brill on 1st 2cm of Ramp?
Yes
No
Select A Alt B
Yes
No
End of Sweep Detector Hold Off* or Logic Section failure
Flyback current generator output buffer failure or Q1234 short circuit
Both Ramps Displayed
Yes
No
Does trace separate operate?
Yes
No
Analogue Section O.K.
Check as 1 above, substituting U1304a for U1201b, and Q1240 Emitter for pin 1403. (Hold off faults do not apply) Include U1404 and Q1402 if bright-up failure.
Trace Ramp signal from Q1341 Emitter to Pin 1403 also see logic section
Select A ramp only and check all pins of U1408 against table in section 5.5.8. If correct, see logic section.

*Hold off failure in Auto Trig mode applies both set and reset to U1201b at End of sweep, forcing Q and $\overline{Q}$ high. Symptoms depend upon relative VBes of Q1222 and Q1224.

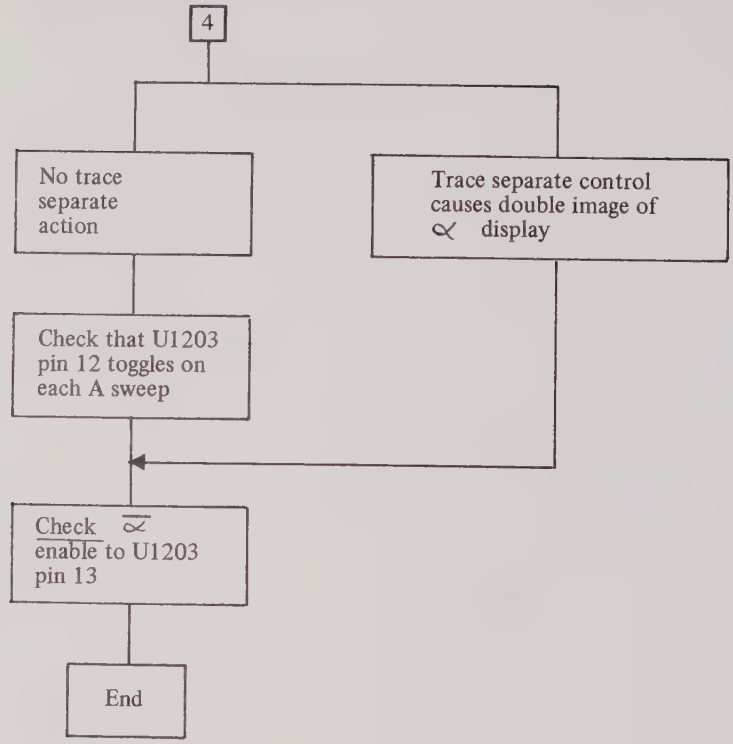
TIMEBASE, LOGIC SECTION

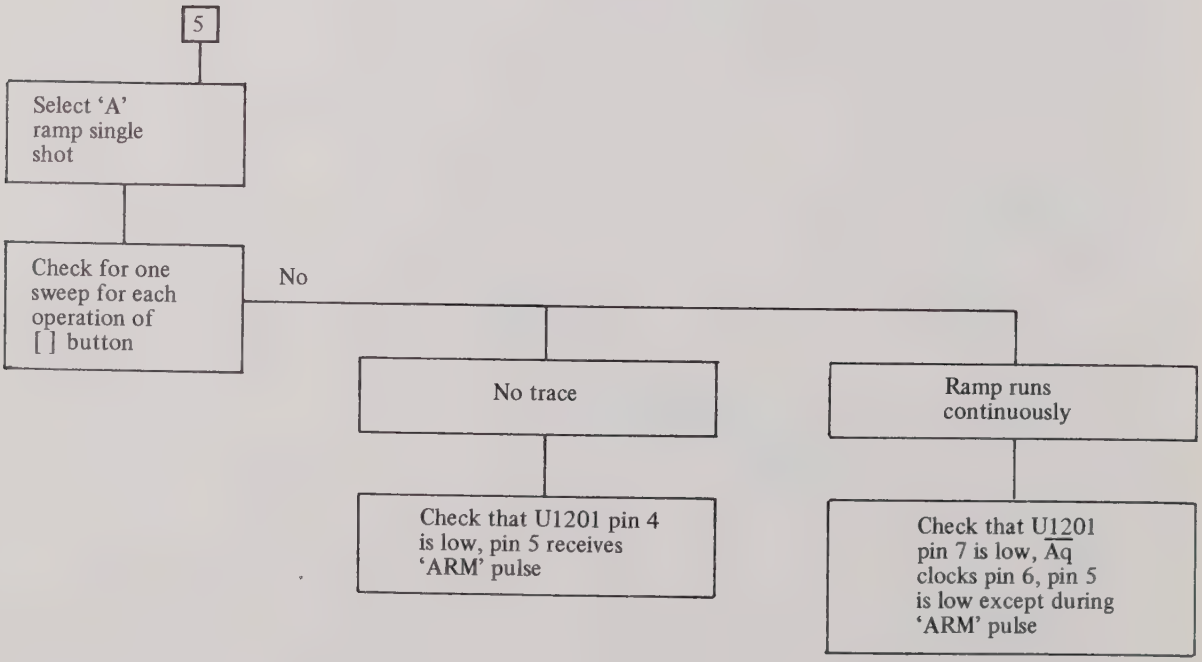
Check analogue sections first. Enter left hand column of logic section at the same level as leaving analogue section. Check port outputs against Fig. 4.9.3 of description section.


Select G 41, TBA=1ms/cm, no trigger inputs
Are CH1,CH2 and ∝ displayed?
No
Yes
Aq held high
Aq held low
Check that U1201 pin 12 is held low by D1203 and pin 13 high via U1202 pin 5
U1201 pin 13 should be low and pin 12 high. Note that D1203,4,5,7 form an 'AND' gate into U1201 pin 12 with bias current via D1218. Check that U1201a is held set via 01202
Select A intensified by B, TBB= 0.2 ms/cm Adjust Contrast
Increased brill on 1st 2cm of ramp?
No
Yes
Bq held high
Bq held low
Select A alt B
U1304 pin 4 should be high, Pin 5 low. Note wire-or of U1304 pin 14 & U1202 pin 3. In this fault condition, U1304 will not have been clocked high by $\overline{Bq}$ but should be held high by U1202.
U1304 pin 4 should be low, Pin 5 high. Note wire-or of U1304 pin 14 & U1202 pin 3 Check $\overline{Aq}$ input to U1304b pin 12.
Both ramps displayed?
No
2
Yes
Does trace separate operate?
No
4
Yes
3


3
Apply a 1kHz sinewave to CH1. Select & adjust 'A' trigger
Do traces remain on screen?
No
Check that trigger pulse reaches U1201 pin 13 and pin 10 goes high at end of hold-off
Yes
Are traces synchronised to signal?
No
Auto still active although triggered. Check that D1205 cathode is low and R1215 is intact
Yes
Select 'B' starts on 'B' trig. and adjust B trigger
Is 'B' trace still on screen?
No
Check that 'B' trigger pulse reaches U1304 pin 6 and U1304 pin 7 is high from start of 'A' ramp to 'B' trigger
Yes
Select 'B' starts on cursor, display B1 sweep, set cursor 1 to convenient point on 'A' ramp
Is 'B' trace still on screen?
No
Check that latched cursor signal to U1306 pin 6 clocks U1304a
5
2
Check action of U1405 and U1616. (see descriptive section "commutation system" for details of operation)
Trace ramp signals via U1409.

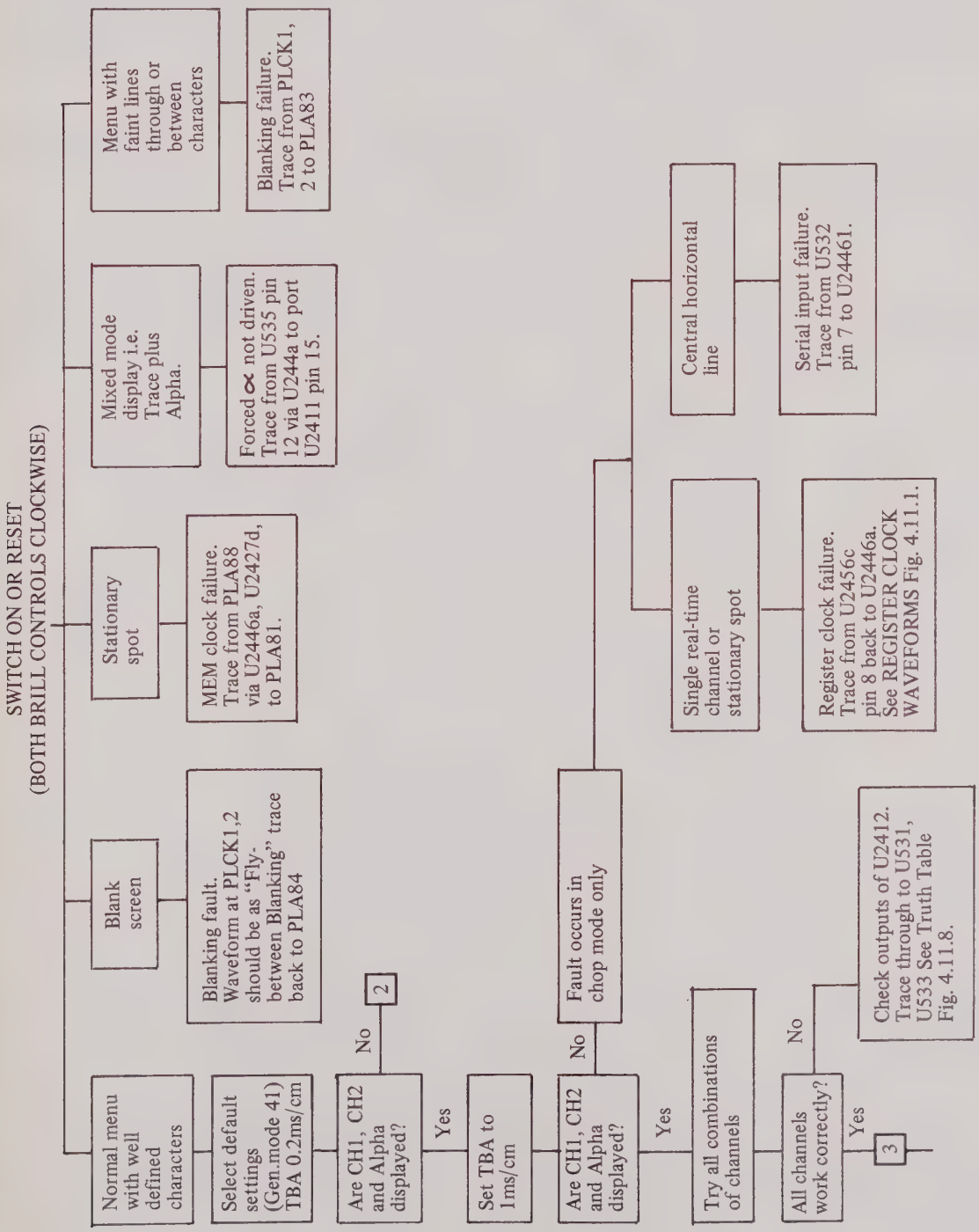
TIMEBASE LOGIC SECTION (CONT.)


4
No trace separate action
Trace separate control causes double image of ∝ display
Check that U1203 pin 12 toggles on each A sweep
Check ∝ enable to U1203 pin 13
End

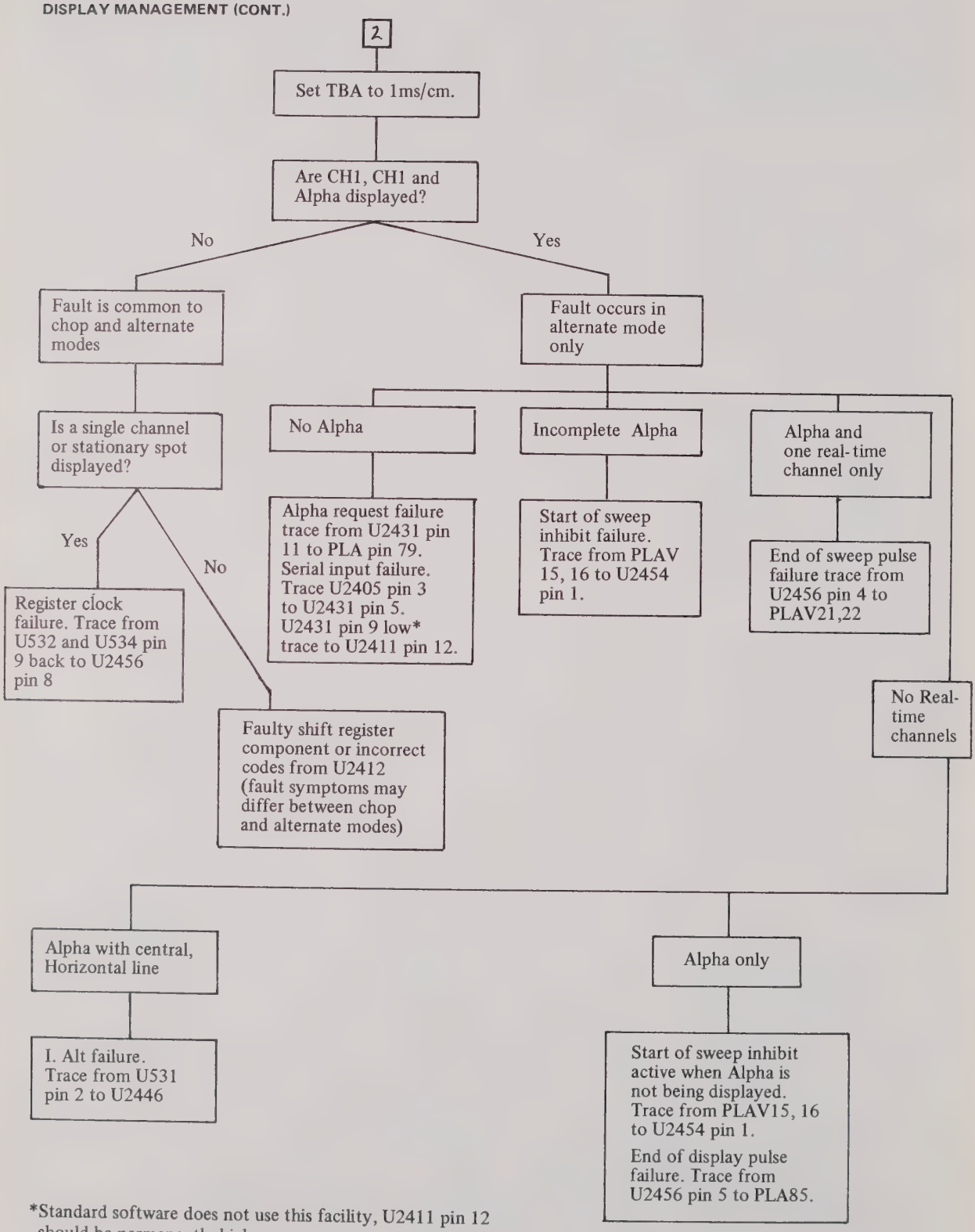

5
Select 'A' ramp single shot
Check for one sweep for each operation of [ ] button
No
No trace
Ramp runs continuously
Check that U1201 pin 4 is low, pin 5 receives 'ARM' pulse
Check that U1201 pin 7 is low, Āq clocks pin 6, pin 5 is low except during 'ARM' pulse

5.4.6 DISPLAY MANAGEMENT

The accompanying flowchart details a suggested sequence for tracing faults in the display management system. Before attempting detailed logic tracing, check that the +5V supply is within limits (±0.25V), and that the outputs of ports U2411 and U2412 correspond with the mode selected (see fig. 4.11.8 of descriptive sections) since illegal output codes may produce misleading systems. Note that the display management contains a mixture of TTL, C MOS and ECL logic devices, see section 5.5.1 for voltage levels at interfaces.

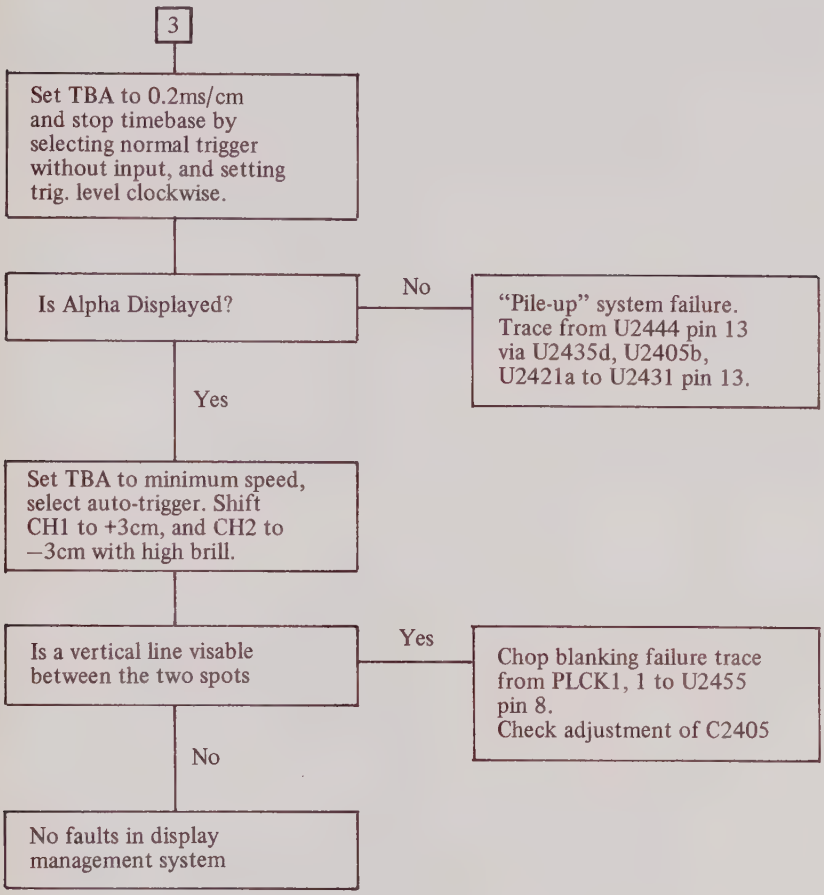

SWITCH ON OR RESET
(BOTH BRILL CONTROLS CLOCKWISE)
Normal menu with well defined characters
Blank screen
Stationary spot
Mixed mode display i.e. Trace plus Alpha.
Menu with faint lines through or between characters
Select default settings (Gen..mode 41) TBA 0.2ms/cm
Blanking fault. Waveform at PLCK1,2 should be as "Fly-between Blanking" trace back to PLA84
MEM clock failure. Trace from PLA88 via U2446a, U2427d, to PLA81.
Forced ∝ not driven. Trace from U535 pin 12 via U244a to port U2411 pin 15.
Blanking failure. Trace from PLCK1, 2 to PLA83
Are CH1, CH2 and Alpha displayed?
No
2
Yes
Set TBA to 1ms/cm
Are CH1, CH2 and Alpha displayed?
No
Fault occurs in chop mode only
Yes
Try all combinations of channels
Single real-time channel or stationary spot
Central horizontal line
Register clock failure. Trace from U2456c pin 8 back to U2446a. See REGISTER CLOCK WAVEFORMS Fig. 4.11.1.
Serial input failure. Trace from U532 pin 7 to U24461.
All channels work correctly?
No
Yes
3
Check outputs of U2412. Trace through to U531, U533 See Truth Table Fig. 4.11.8.

DISPLAY MANAGEMENT (CONT.)


2
Set TBA to 1ms/cm.
Are CH1, CH1 and Alpha displayed?
No
Yes
Fault is common to chop and alternate modes
Fault occurs in alternate mode only
Is a single channel or stationary spot displayed?
No Alpha
Incomplete Alpha
Alpha and one real-time channel only
Yes
No
Alpha request failure trace from U2431 pin 11 to PLA pin 79. Serial input failure. Trace U2405 pin 3 to U2431 pin 5. U2431 pin 9 low* trace to U2411 pin 12.
Start of sweep inhibit failure. Trace from PLAV 15, 16 to U2454 pin 1.
End of sweep pulse failure trace from U2456 pin 4 to PLAV21,22
Register clock failure. Trace from U532 and U534 pin 9 back to U2456 pin 8
Faulty shift register component or incorrect codes from U2412 (fault symptoms may differ between chop and alternate modes)
No Real-time channels
Alpha with central, Horizontal line
Alpha only
I. Alt failure. Trace from U531 pin 2 to U2446
Start of sweep inhibit active when Alpha is not being displayed. Trace from PLAV15, 16 to U2454 pin 1.
End of display pulse failure. Trace from U2456 pin 5 to PLA85.

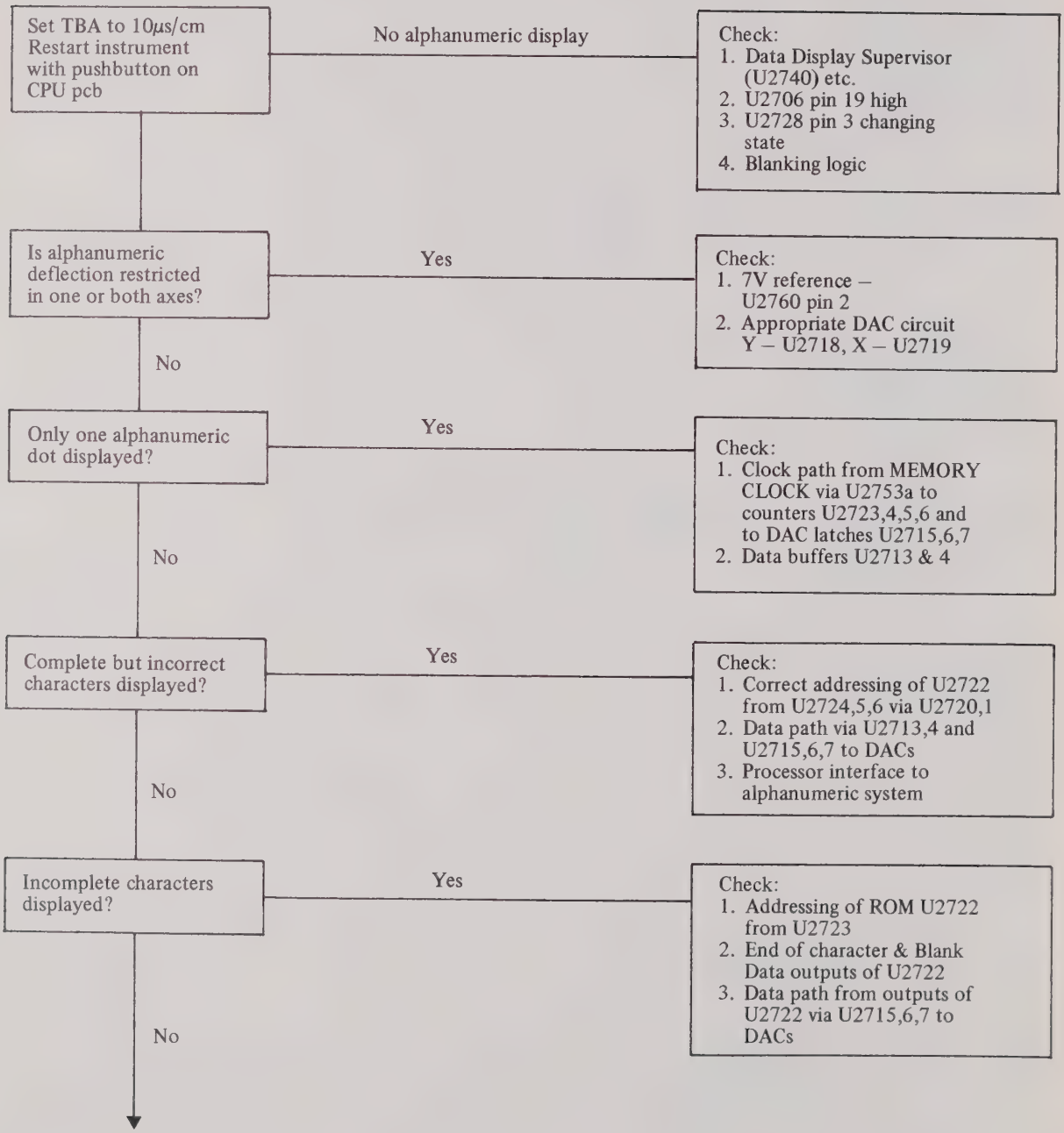
*Standard software does not use this facility, U2411 pin 12 should be permanently high.

DISPLAY MANAGEMENT (CONT.)

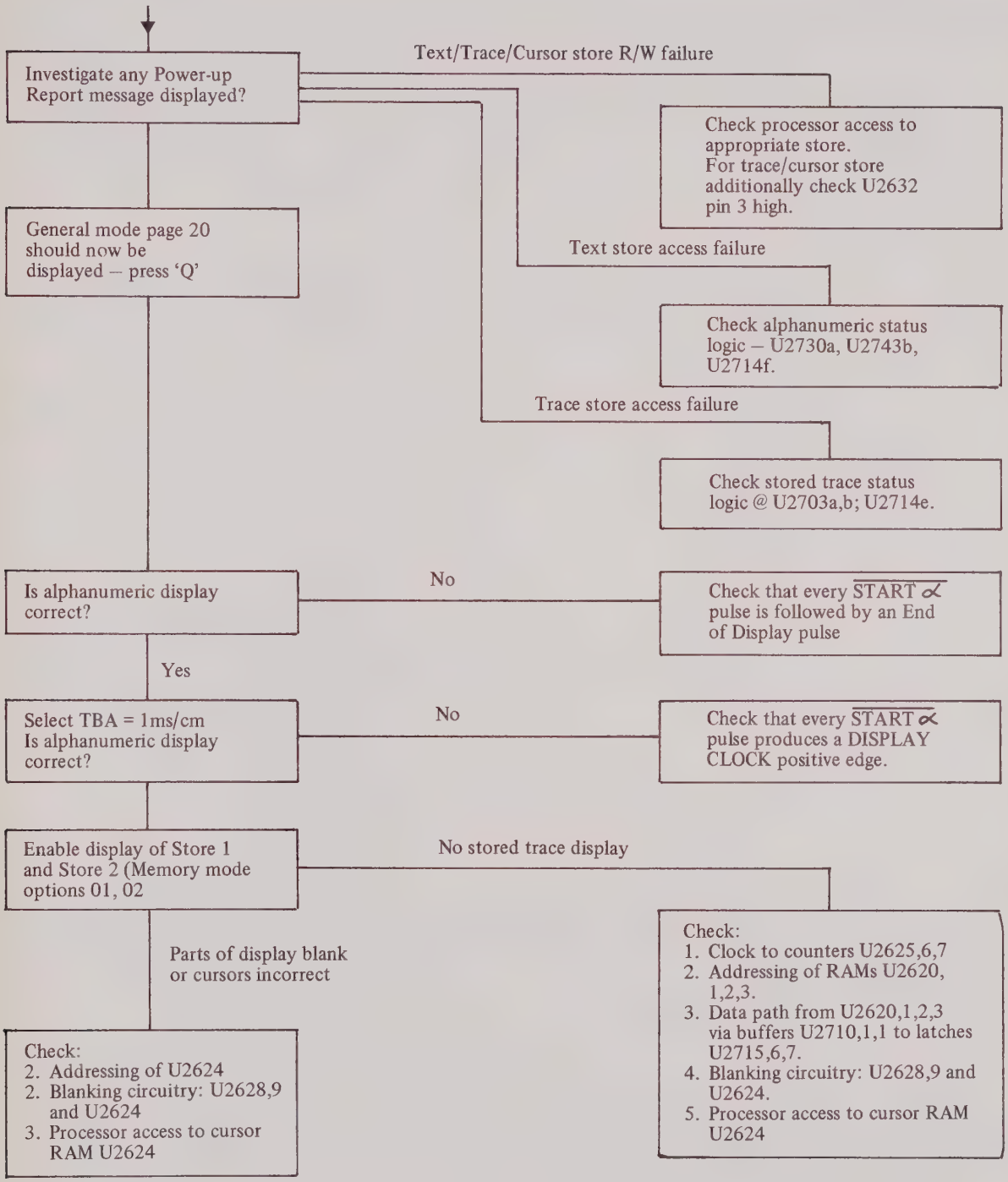

3
Set TBA to 0.2ms/cm and stop timebase by selecting normal trigger without input, and setting trig. level clockwise.
Is Alpha Displayed?
No
"Pile-up" system failure. Trace from U2444 pin 13 via U2435d, U2405b, U2421a to U2431 pin 13.
Yes
Set TBA to minimum speed, select auto-trigger. Shift CH1 to +3cm, and CH2 to −3cm with high brill.
Is a vertical line visable between the two spots
Yes
Chop blanking failure trace from PLCK1, 1 to U2455 pin 8. Check adjustment of C2405
No
No faults in display management system

5.4.7 DATA DISPLAY

Note: In the following the alphanumeric portion of the display should be identified by the alphanumeric intensity control.

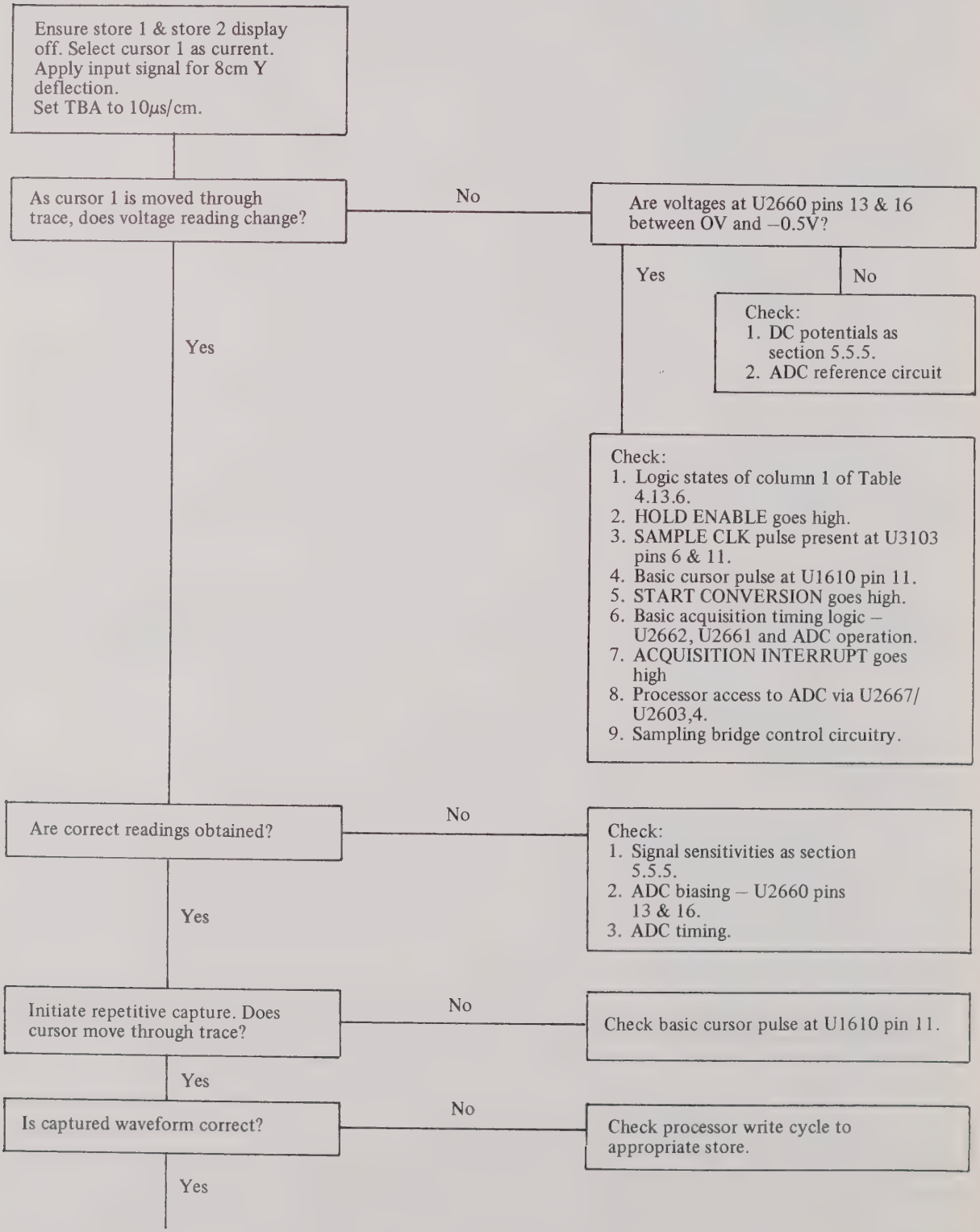

Set TBA to 10μs/cm
Restart instrument with pushbutton on CPU pcb
No alphanumeric display
Check:
1. Data Display Supervisor (U2740) etc.
2. U2706 pin 19 high
3. U2728 pin 3 changing state
4. Blanking logic
Is alphanumeric deflection restricted in one or both axes?
Yes
Check:
1. 7V reference – U2760 pin 2
2. Appropriate DAC circuit Y – U2718, X – U2719
No
Only one alphanumeric dot displayed?
Yes
Check:
1. Clock path from MEMORY CLOCK via U2753a to counters U2723,4,5,6 and to DAC latches U2715,6,7
2. Data buffers U2713 & 4
No
Complete but incorrect characters displayed?
Yes
Check:
1. Correct addressing of U2722 from U2724,5,6 via U2720,1
2. Data path via U2713,4 and U2715,6,7 to DACs
3. Processor interface to alphanumeric system
No
Incomplete characters displayed?
Yes
Check:
1. Addressing of ROM U2722 from U2723
2. End of character & Blank Data outputs of U2722
3. Data path from outputs of U2722 via U2715,6,7 to DACs
No

DATA DISPLAY (CONT)

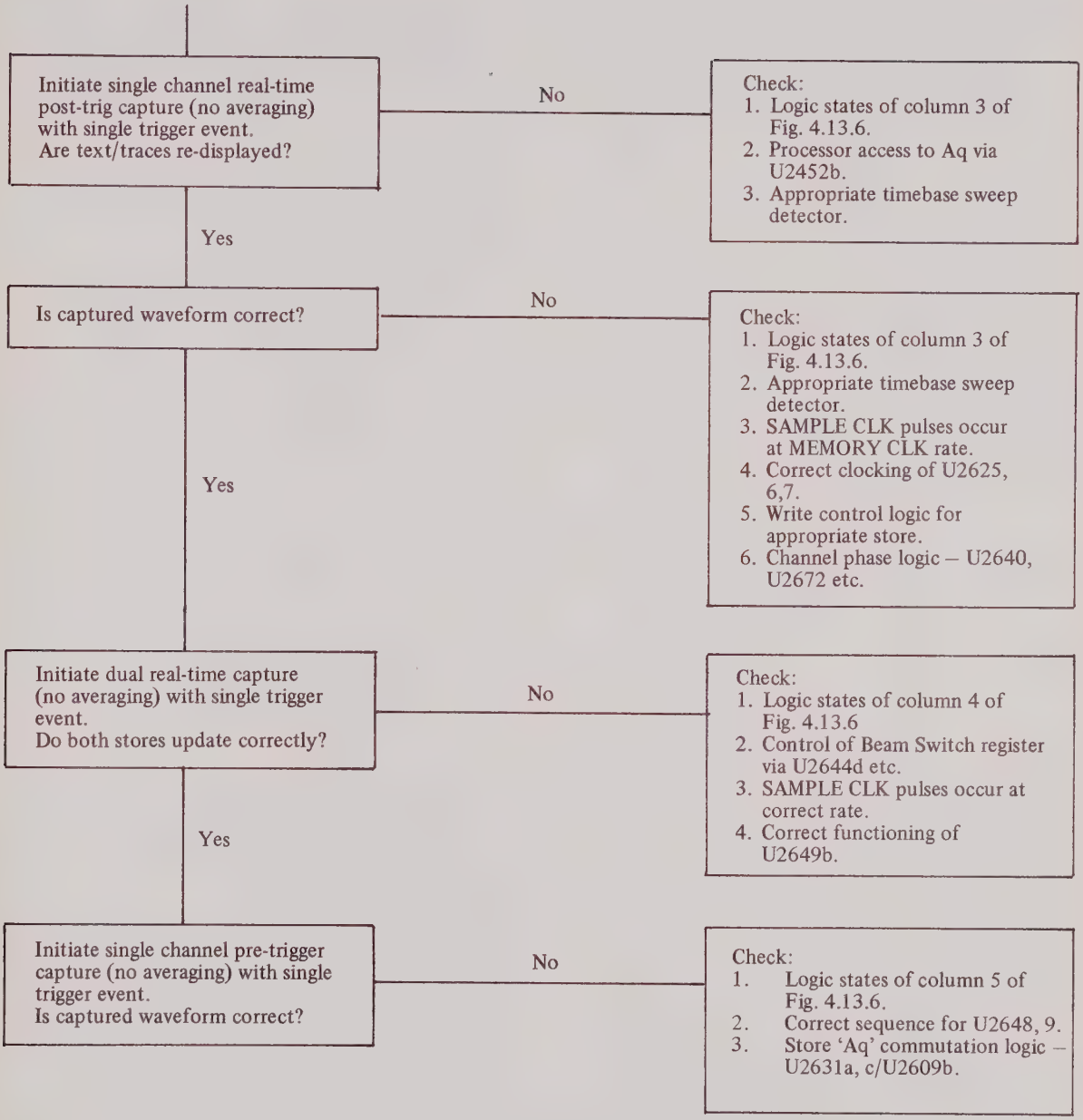

Investigate any Power-up Report message displayed?
Text/Trace/Cursor store R/W failure
Check processor access to appropriate store. For trace/cursor store additionally check U2632 pin 3 high.
General mode page 20 should now be displayed – press 'Q'
Text store access failure
Check alphanumeric status logic – U2730a, U2743b, U2714f.
Trace store access failure
Check stored trace status logic @ U2703a,b; U2714e.
Is alphanumeric display correct?
No
Check that every START ∝ pulse is followed by an End of Display pulse
Yes
Select TBA = 1ms/cm Is alphanumeric display correct?
No
Check that every START ∝ pulse produces a DISPLAY CLOCK positive edge.
Enable display of Store 1 and Store 2 (Memory mode options 01, 02
No stored trace display
Parts of display blank or cursors incorrect
Check:
2. Addressing of U2624
2. Blanking circuitry: U2628,9 and U2624
3. Processor access to cursor RAM U2624
Check:
1. Clock to counters U2625,6,7
2. Addressing of RAMs U2620, 1,2,3.
3. Data path from U2620,1,2,3 via buffers U2710,1,1 to latches U2715,6,7.
4. Blanking circuitry: U2628,9 and U2624.
5. Processor access to cursor RAM U2624

5.4.8. DATA ACQUISITION

Note: In capture modes averaging can be employed merely to allow longer periods of activity for examination.


Ensure store 1 & store 2 display off. Select cursor 1 as current. Apply input signal for 8cm Y deflection. Set TBA to 10μs/cm.
As cursor 1 is moved through trace, does voltage reading change?
No
Are voltages at U2660 pins 13 & 16 between OV and −0.5V?
Yes
No
Check:
1. DC potentials as section 5.5.5.
2. ADC reference circuit
Yes
Check:
1. Logic states of column 1 of Table 4.13.6.
2. HOLD ENABLE goes high.
3. SAMPLE CLK pulse present at U3103 pins 6 & 11.
4. Basic cursor pulse at U1610 pin 11.
5. START CONVERSION goes high.
6. Basic acquisition timing logic – U2662, U2661 and ADC operation.
7. ACQUISITION INTERRUPT goes high
8. Processor access to ADC via U2667/ U2603,4.
9. Sampling bridge control circuitry.
Are correct readings obtained?
No
Check:
1. Signal sensitivities as section 5.5.5.
2. ADC biasing – U2660 pins 13 & 16.
3. ADC timing.
Yes
Initiate repetitive capture. Does cursor move through trace?
No
Check basic cursor pulse at U1610 pin 11.
Yes
Is captured waveform correct?
No
Check processor write cycle to appropriate store.
Yes

DATA ACQUISITION (CONT)


Initiate single channel real-time post-trig capture (no averaging) with single trigger event. Are text/traces re-displayed?
No
Check:
1. Logic states of column 3 of Fig. 4.13.6.
2. Processor access to Aq via U2452b.
3. Appropriate timebase sweep detector.
Yes
Is captured waveform correct?
No
Check:
1. Logic states of column 3 of Fig. 4.13.6.
2. Appropriate timebase sweep detector.
3. SAMPLE CLK pulses occur at MEMORY CLK rate.
4. Correct clocking of U2625, 6,7.
5. Write control logic for appropriate store.
6. Channel phase logic – U2640, U2672 etc.
Yes
Initiate dual real-time capture (no averaging) with single trigger event. Do both stores update correctly?
No
Check:
1. Logic states of column 4 of Fig. 4.13.6
2. Control of Beam Switch register via U2644d etc.
3. SAMPLE CLK pulses occur at correct rate.
4. Correct functioning of U2649b.
Yes
Initiate single channel pre-trigger capture (no averaging) with single trigger event. Is captured waveform correct?
No
Check:
1. Logic states of column 5 of Fig. 4.13.6.
2. Correct sequence for U2648, 9.
3. Store 'Aq' commutation logic – U2631a, c/U2609b.

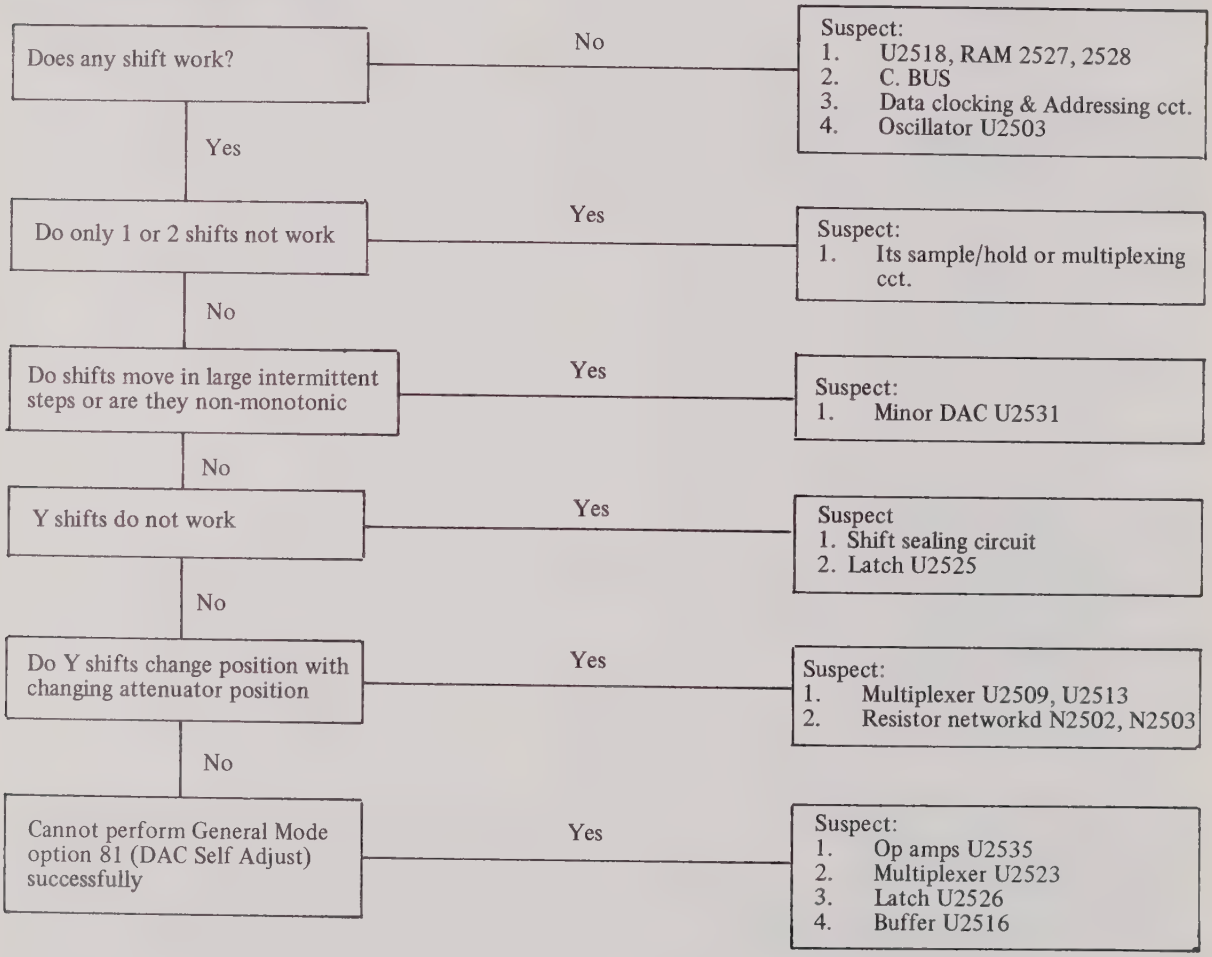
RELATIONSHIP BETWEEN ACQUISITION MODES AND TRUTH TABLE 4.13.6

a) In the absence of a capture sequence (Memory Mode 19) and Data Input Display off (Calculation Mode 14), and provided the current cursor is assigned to a 'real-time' trace (i.e. CH1 or CH2) then column 1 of Table 4.13.6 applies.

b) For the same conditions as a) but with Data Input Display on (Calculation Mode 14), the processor alternates between columns 1 and 2 of Table 4.13.6.

c) Columns 3–7 follow the descriptions heading each column.

5.4.9 VOLTAGE GENERATOR



5.4.10 CPU

The interaction of hardware and software can cause difficulty when faultfinding microprocessor based systems. The power-up software in the instrument has some self checking procedures designed to inform the user of major malfunction. The messages are listed below, with pointers to likely causes.

Faced with a failure that prevents successful entry into the power-up routine, or display of the results of the self diagnosis, then other responses should be examined.

Note: Although the processor checks the data integrity of NVRAM by checksum it is possible to enter a non recoverable condition by partial corruption of variables held in NVRAM this will probably cause garbage to be displayed on the current settings page. In this case, turn the machine off and short test point P1 to GND for at least 1 second. If, after turn-on from this condition front panel indicators for shift allocation and cursor activation behave as expected, then attention should be directed towards the mechanisms by which alphanumeric data is displayed and by which the display is controlled.

In particular C-bus should be examined for correct working, preferably with respect to the timebase board.

Also of particular interest as a guide to the correct behaviour of the microprocessor is the IRQ line (pin 3). Should it be shorted low then all normal operation of the instrument will cease. In normal operation, without change to front panel controls this line transiently goes low every 25ms.

If the spinwheel is now activated in association with the change of some parameter such as X or Y shift, then the IRQ line should be seen to increase dramatically in activity, and the time spent low after regular interrupt also significantly increase. A fault directly associated with the microprocessor on immediate date/address/control buses is most unlikely if the above sequence can be induced. If the microprocessor is still suspect then Fig. 5.4.2 should be consulted. This gives the state of all pins for normal operation. If the fault has not been identified at this stage, then the instrument should be returned for repair as recourse to an emmulator system is by far the quickest way to eliminate working elements and isolate a fault. Note that the system used must be compatible with the 6809 processor used, and in particular supply a clock on pin 39 at X4 E out frequency. It must, further, allow 'E' stretching by MREADY (watch dynamic rams) and not preempt any of the address space.

Possible Power-up errors

1. ROM error – fatal error # n.

   At power-on on the processor performs checksum calculations on each rom and an error will substitute a number for n above as follows:

n	Address range	ROM in error
0	S28ØØ – S3FFF	GPIB paged rom U2951 A13 Hi
1	S2ØØØ – S3FFF	GPIB paged rom U2951 A13 Lo
2	S4ØØØ – S5FFF	CPU U2006
3	S6ØØØ – S7FFF	CPU U2005
4	S8ØØØ – S9FFF	CPU U2004
5	SAØØØ – SBFFF	CPU U2003
6	SCØØØ – SDFFF	CPU U2002
7	SEØØØ – SFFFF	CPU U2001

Note that as the checksums and the checksum routine are contained in the top rom # 7 is unlikely!

2. NVRAM failed R/W test

   Fatal error as the processor uses this ram for scratchpad, system stack, current machine settings etc.
   May be caused by incorrect setting of POWER FAILURE detect circuitry which does not re-enable NVRAM at RESET. If this is the case, pressing S2001 after power-up will clear this fault.

   When this message is displayed, the processor is continually attempting the read-write test, allowing empiracle fault finding.

3. NVRAM corrupted all defaults used

   Probable causes

   a) Back-up battery failure.
   b) Mis-setting of POWER-FAIL detect circuitry.

4. Reselection of stored settings failed

   Probable causes

   a) Recalling an uninitialised machine state.
   b) Recalling a machine state corrupted or incorrectly transferred from GPIBus.
   c) Switching off while the instrument is changing a menu setting.

5. Text store
   Store 1
   Store 2
   Cursor Store
   } failed R/W test

   Non-fatal as the instrument will function with reduced ability.

6. Machine states corrupted
   As 3) but check GPIB back-up battery.

7. GPIB store failed R/W test
   Paged ram of GPIB board, check

   a) bus faults
   b) paging faults.

8. Shift system interrupt failure
   No interrupt from Vgen scratchpad to allow processor access. May occur after switch-on as fault occurs. It

is only flagged once per switch-on and will be ignored thereafter, allowing operation of the rest of the instrument.

9. Test store access failure.
See data display for fault finding.
Will cause the system to hang if trace display selected.

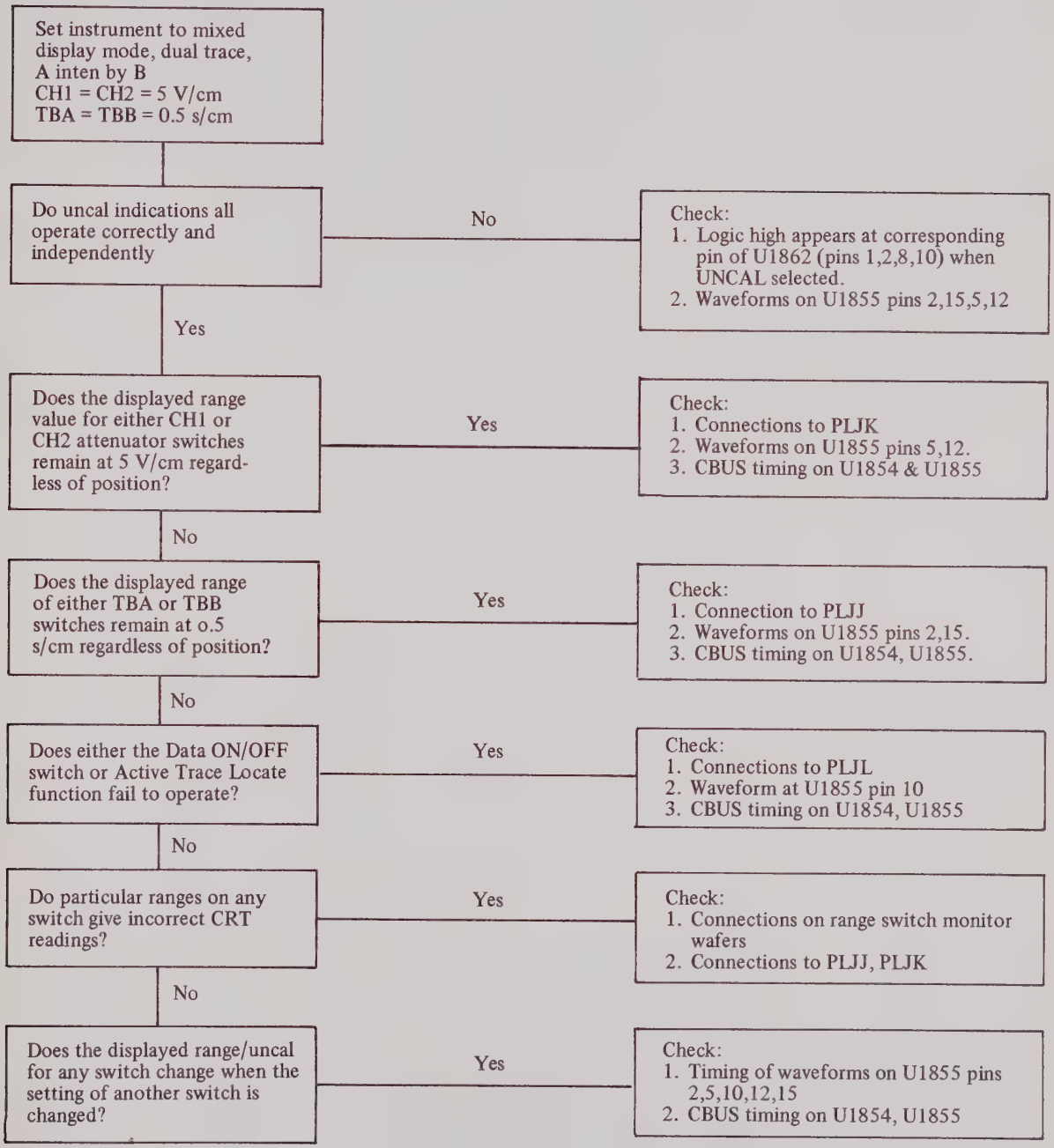
10. Trace store access failure
See data display for fault finding.
Will cause the system to hang when reading ADC (current cursor voltage) or if cursor is on a store.

11. Real-time Interrupt failure
Fault on this board, check action of U2011b and programmable clock divider chain.
Keypad cannot be debounced and so only first key press will be recognised.

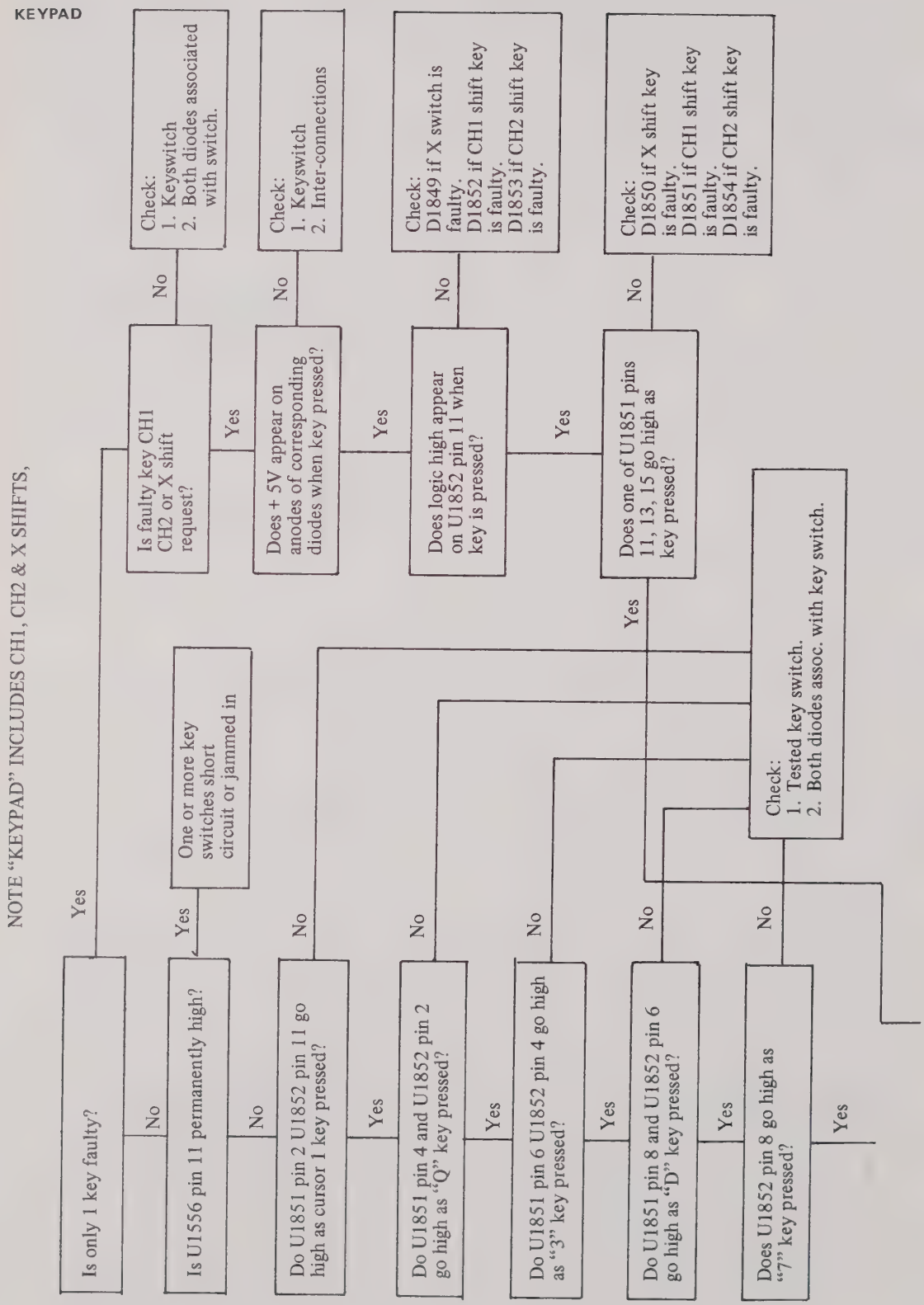
1.	OV GND		
2.	HIGH		
3.	HIGH reg. ↓ 25ms + other activity		
4.	HIGH		
5.	LOW ↑ FOR $\overline{IRQ}$		
6.	LOW		
7.	+5V		
8.	Ao		
9.	”		
10.	”		
12.	”		
13.	”		
14.	”		
15.	”	μP ADDRESS BUS:	HIGHLY ACTIVE BETWEEN LOGIC HIGH OR LOW, CHANGING EACH 1μs CYCLE
16.	”		
17.	”		
18.	”		
19.	”		
20.	”		
21.	”		
22.	”		
23.	A15		
24.	D7		
25.	”		
26.	”		
27.	”	μP DATA BUS:	HIGHLY ACTIVE PULLED HIGH
28.	”		
29.	”		
30.	”		
31.	Do		
32.	R/$\overline{W}$	HIGH MORE THAN LOW	
33.	HIGH		
34.	IRREGULAR 1μs SQUAREWAVE		
35.	IRREGULAR: PHASED WITH 34		
36.	HIGH	C BUS ACCESS CAUSES LOW TRANSITION	
37.	HIGH		
38.	4MHz SINEWAVE		
39.	4MHz SINEWAVE		
40.	HIGH		

KEY { ↓ HIGH to low transition. ↑ Low to high transition
HIGH = logic high > 2.4 volt
LOW = logic low < 0.6 volt

5.4.11 CONTROL DATA BUS


Set instrument to mixed display mode, dual trace, A inten by B
CH1 = CH2 = 5 V/cm
TBA = TBB = 0.5 s/cm
Do uncal indications all operate correctly and independently
No
Check:
1. Logic high appears at corresponding pin of U1862 (pins 1,2,8,10) when UNCAL selected.
2. Waveforms on U1855 pins 2,15,5,12
Yes
Does the displayed range value for either CH1 or CH2 attenuator switches remain at 5 V/cm regardless of position?
Yes
Check:
1. Connections to PLJK
2. Waveforms on U1855 pins 5,12.
3. CBUS timing on U1854 & U1855
No
Does the displayed range of either TBA or TBB switches remain at o.5 s/cm regardless of position?
Yes
Check:
1. Connection to PLJJ
2. Waveforms on U1855 pins 2,15.
3. CBUS timing on U1854, U1855.
No
Does either the Data ON/OFF switch or Active Trace Locate function fail to operate?
Yes
Check:
1. Connections to PLJL
2. Waveform at U1855 pin 10
3. CBUS timing on U1854, U1855
No
Do particular ranges on any switch give incorrect CRT readings?
Yes
Check:
1. Connections on range switch monitor wafers
2. Connections to PLJJ, PLJK
No
Does the displayed range/uncal for any switch change when the setting of another switch is changed?
Yes
Check:
1. Timing of waveforms on U1855 pins 2,5,10,12,15
2. CBUS timing on U1854, U1855

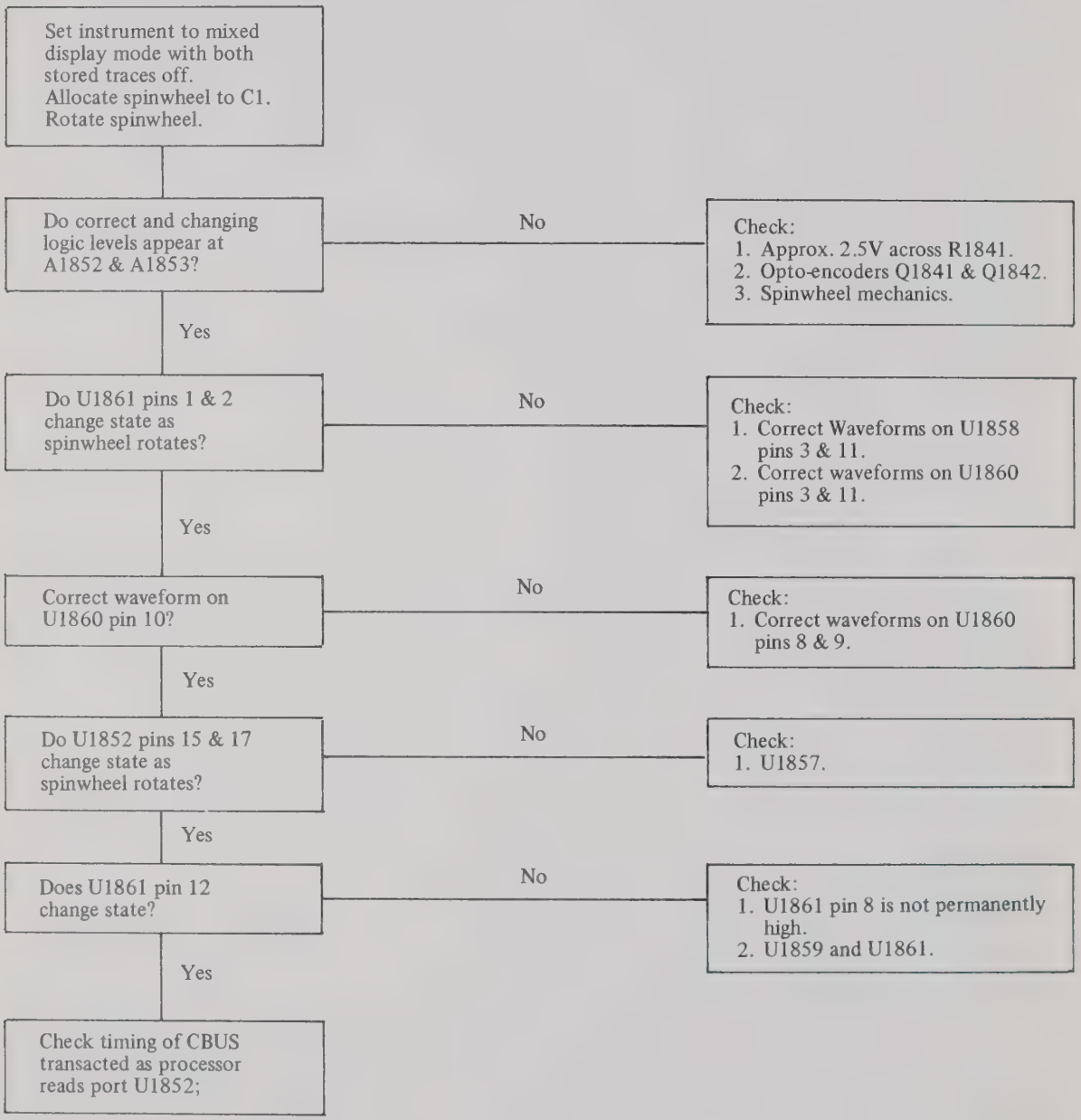
KEYPAD


NOTE "KEYPAD" INCLUDES CH1, CH2 & X SHIFTS,
Is only 1 key faulty?
Yes
No
Is faulty key CH1 CH2 or X shift request?
Yes
No
Check:
1. Keyswitch
2. Both diodes associated with switch.
Is U1556 pin 11 permanently high?
Yes
No
One or more key switches short circuit or jammed in
Does + 5V appear on anodes of corresponding diodes when key pressed?
Yes
No
Check:
1. Keyswitch
2. Inter-connections
Do U1851 pin 2 U1852 pin 11 go high as cursor 1 key pressed?
Yes
No
Does logic high appear on U1852 pin 11 when key is pressed?
Yes
No
Check:
D1849 if X switch is faulty.
D1852 if CH1 shift key is faulty.
D1853 if CH2 shift key is faulty.
Do U1851 pin 4 and U1852 pin 2 go high as "Q" key pressed?
Yes
No
Does one of U1851 pins 11, 13, 15 go high as key pressed?
Yes
No
Check:
D1850 if X shift key is faulty.
D1851 if CH1 shift key is faulty.
D1854 if CH2 shift key is faulty.
Do U1851 pin 6 U1852 pin 4 go high as "3" key pressed?
Yes
No
Do U1851 pin 8 and U1852 pin 6 go high as "D" key pressed?
Yes
No
Check:
1. Tested key switch.
2. Both diodes assoc. with key switch.
Does U1852 pin 8 go high as "7" key pressed?
Yes
No

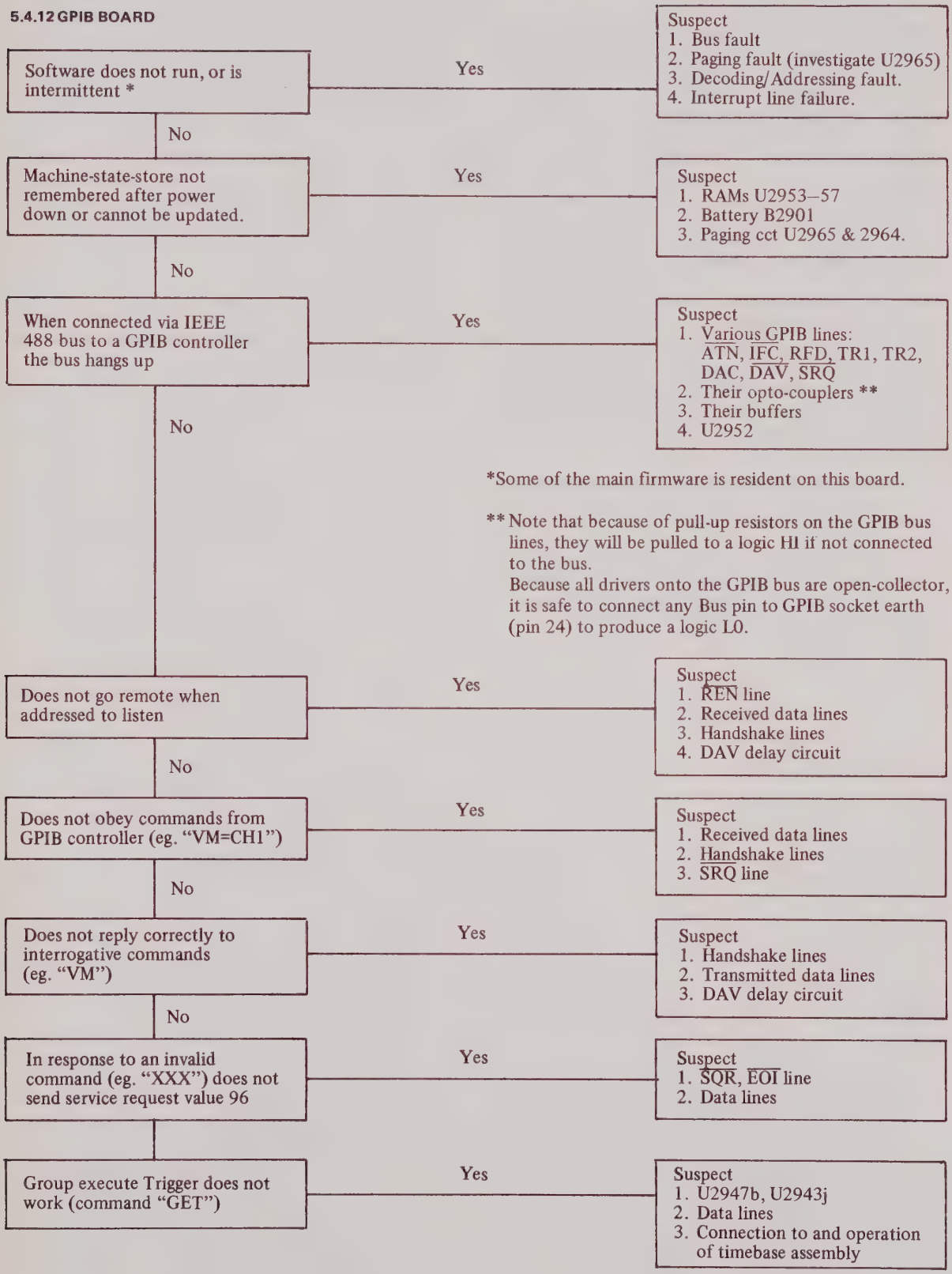
KEYPAD

Does U1856 pin 11 go high as any key pressed?
No
Check 1. U1853
Yes
Does U1851 pin 17 change state as any key pressed?
Stays Low
Check:
1. U1856.
Stays high
Check:
1. Waveforms at U1859 pins 8 & 10.
2. Waveforms at U1856 pin 10.
Yes
Does U1860 pin 4 change state as any key pressed?
Stays Low
Check:
1. CBUS timing on U1855.
Stays high
Yes
Check CBUS timing on U1851 and U1852
Check:
1. Waveform at U1858 pin 4.

SPINWHEEL CONTROL AND INTERFACE


Set instrument to mixed display mode with both stored traces off.
Allocate spinwheel to C1.
Rotate spinwheel.
Do correct and changing logic levels appear at A1852 & A1853?
No
Check:
1. Approx. 2.5V across R1841.
2. Opto-encoders Q1841 & Q1842.
3. Spinwheel mechanics.
Yes
Do U1861 pins 1 & 2 change state as spinwheel rotates?
No
Check:
1. Correct Waveforms on U1858 pins 3 & 11.
2. Correct waveforms on U1860 pins 3 & 11.
Yes
Correct waveform on U1860 pin 10?
No
Check:
1. Correct waveforms on U1860 pins 8 & 9.
Yes
Do U1852 pins 15 & 17 change state as spinwheel rotates?
No
Check:
1. U1857.
Yes
Does U1861 pin 12 change state?
No
Check:
1. U1861 pin 8 is not permanently high.
2. U1859 and U1861.
Yes
Check timing of CBUS transacted as processor reads port U1852;

5.4.12 GPIB BOARD



*Some of the main firmware is resident on this board.

** Note that because of pull-up resistors on the GPIB bus lines, they will be pulled to a logic HI if not connected to the bus.
Because all drivers onto the GPIB bus are open-collector, it is safe to connect any Bus pin to GPIB socket earth (pin 24) to produce a logic LO.

5.5 CIRCUIT VOLTAGES

The following sections offer a general guide to circuit voltages and signal sensitivities as an aid to fault-finding.

The D.C. voltages shown are measured using a 1MΩ minimum input impedance digital voltmeter between the measured point and 0V unless otherwise stated. A 1kΩ resistor is inserted in series with the positive lead to prevent instability.

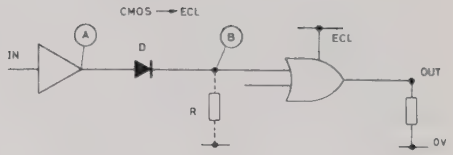
5.5.1 LOGIC SIGNALS

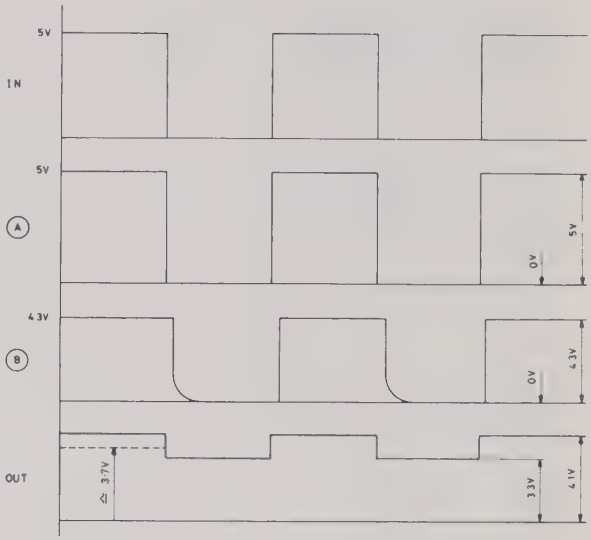
A mixture of logic technologies is used on the instrument and hence logic signal swings can change significantly whilst tracing any particular function. Observers should be aware of both the input and output criteria of each logic family.

ECL in the instrument is powered from the +5 volt rail with the exception of the sample head drive (Y output board) and the acquisition interface to it (−5 volt). CMOS is always powered from the +5 volt supply and normally the most negative voltage encountered is ground. There are two exceptions to this.

1. Timebase board analogue gates have logic swing of 0 to +5V but can pass analogue signals of up to −10V.
2. Voltage generator multiplexer circuits use analogue gates with +5 to −5V logic swings U2506,2508 derived from a level translator, U2505.

Several strategies have been adopted to allow interfaces between the families





	LSTTL	NMOS	CMOS	ECL(+5)	(−5)
NOMINAL IMPEDANCE	2K	100K	1M	50K	50K
I/P THRESHOLD	HIGH 2	2.0	3.5	3.9	−1.1
	LOW 0.8	0.6	1.5	3.5	−1.5
O/P VOLTAGE	3	2.6	5.0	4.1	−0.9
	0.3	0.4	0.0	3.3	−1.7
SIMPLE GATE PROP	10ns #3	N/A	50–150ns #1	4ns #2. #4	4ns

#1. Variations are dependent upon output loading and where capacitance is large, this may be exceeded. Transition time through analogue gates is in the order of 10ns.

#2. This is dependent upon pull down resistor value for ↓ transistion.

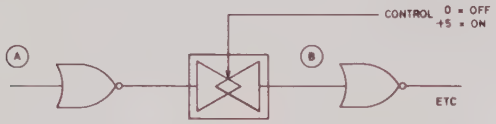
#3. No open collector TTL is used although pull-up resistors sometimes are.

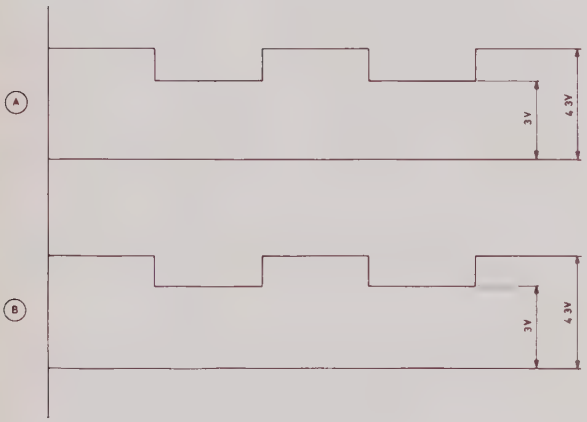
#4. ECL is sometimes terminated to a +3V voltage derived from the +5 volt supply via resistors.

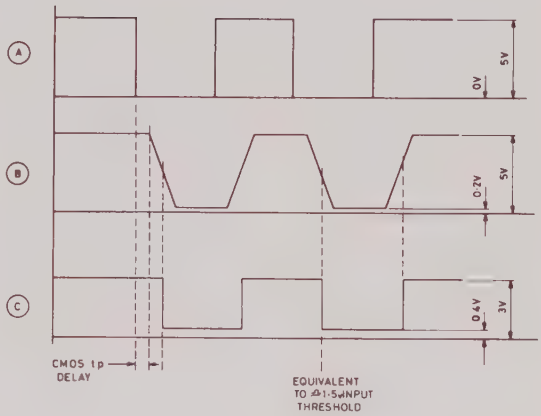
Fig. 5.5.1 Logic Input/Output Characteristics

diode included so that ECL input high is not infringed. R sometimes used for fast CMOS signal.

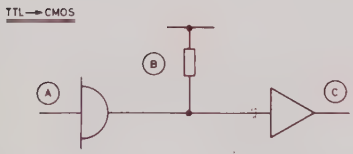
Note that where analogue gates are used in conjunction with ECL to produce complex functions then the gate only acts in a transition mode i.e. there is no amplitude change.

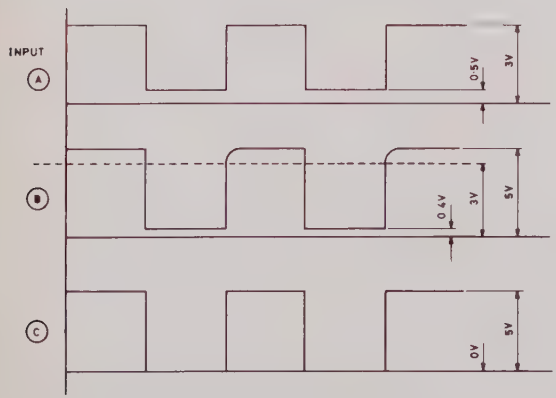


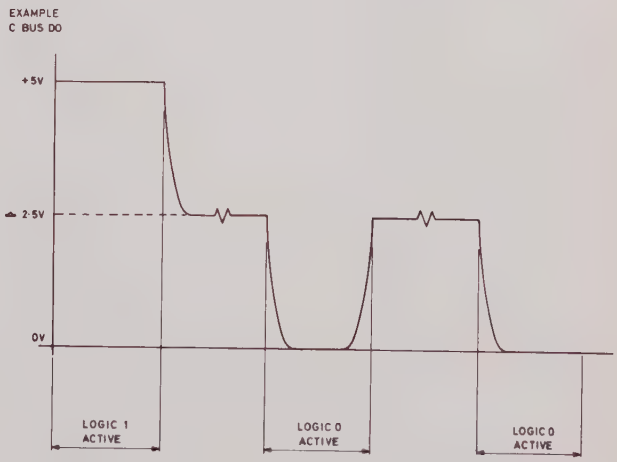


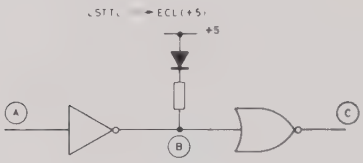


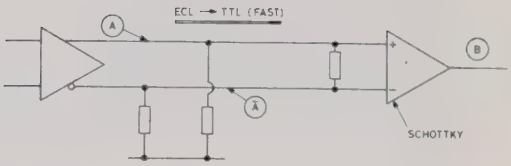
Some bused signals are configured with an inactive state where nether a logic 1 or 0 condition is used i.e.

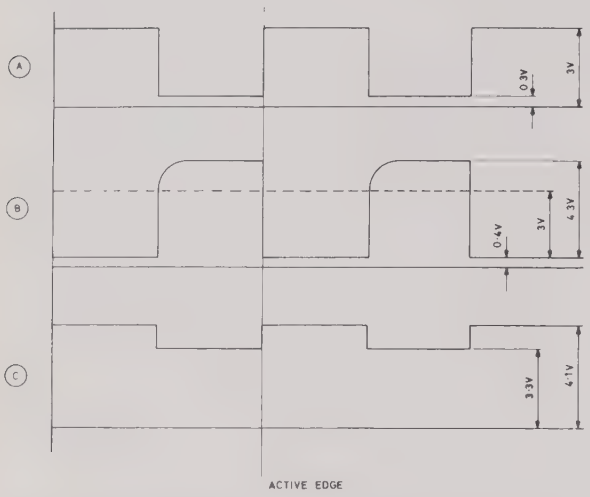


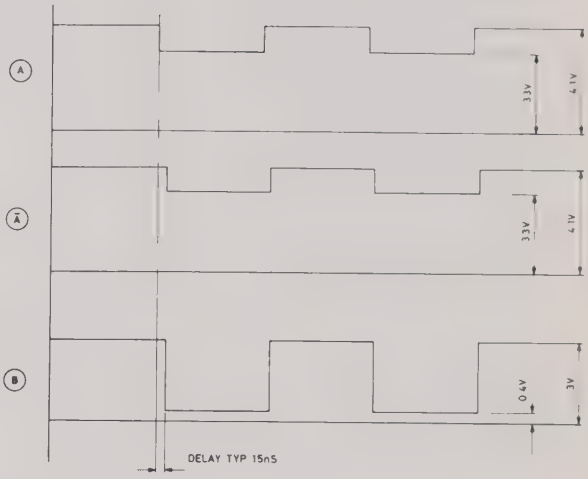






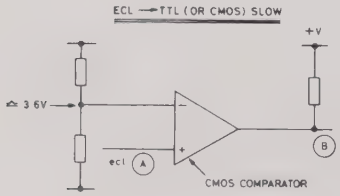


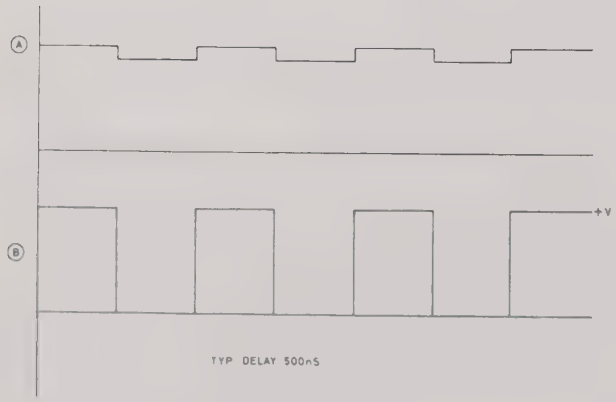




This is usually arranged so that the ↓ LS transition is active.

N.B. Often signal is transmitted as a twisted pair with characteristic impedance, and termination.





OUTPUT						
NOMINAL	VOLTAGE IN		SET VOLTAGE		APPROX MEASUREMENT	
	MIN *1	RIPPLE P/P Volts	HIGH	LOW	LOAD CURRENT	POINT
+5V	7.6V	500mV	5.05V	4.95V	6.5* Amp	Backplane 52 wrt 50
−5V	7.2	1 Volt	−5.05V	−4.95V	500 mA	X–Output PLW 5 wrt 3
+12V #2	15V	1 Volt	12.15V	11.85V	1 Amp	Backplane 71 wrt 50
+12V #1			12.25V	11.75V	1.3 Amp	X Amp PLY 4 wrt PLW 4
−12V	15V	1Volt	12.15V	11.85V	1.2 Amp	X Amp PLW 6 wrt PLW 4
+12V	30V	25mV	25.1V	23.1V *2	15 mA	X Amp PLY 3 wrt PLW 4
+60V			64V	56.5V *3	2.5 mA	X Amp PLY 7 wrt PLW 4

* No Options Fitted.
*1 This is the instantaneous min voltage at the main smoothing capacitor.
*2 Assumes +12 Volt #2 set ± 1%
*3 Assumes −12 Volt set ± 1%

Fig. 5.5.2 Power Supply Voltages

5.5.3 Y PRE-AMPLIFIER D.C. OPERATING POTENTIALS

The voltages shown in the table below are measured using a 1MΩ minimum input impedance digital voltmeter between the Measured Point and OV unless otherwise stated. A 1KΩ resistor is inserted in the positive lead to prevent instability. On the oscilloscope under test, CH1 and CH2 Sensitivity controls are set to 20mV/cm with their inputs grounded. CH1 is selected and the trace positioned on screen center.

MEASURED POINT		VOLTAGE
Q102 Emitter	–	−4V
Q103 Base	–	+0.72V
Q103 Emitter	–	OV
U105 Pin 6	–	−3.86V
U101 Pin 2, Pin 6	–	OV
U102 Pin 1 & 7	–	−0.8V
Q104, Q105 Emitter	–	+3.2V
Q104, Q105 Collector	–	−5.4V
U103 Pin 3, Pin 5	–	−6.2V
U103 Pin 13,12,9,10	–	−1.03V
U104 Pin 8, 11	–	+2V
U104 Pin 3,4,5,13	–	−6.65V
U107 Pin 1 [Trace]	–	−2V
U107 Pin 5 [Normal]	–	−2.24V
U107 Pin 1 [Trace]	–	−2.24V
U107 Pin 5 [Inverted]	–	−2V
U107 Pin 9 (Var Gain = Cal)	–	−7.2V
U107 Pin 9 (Var Gain = Uncal)	–	−10.8V
Unit 107 Pin 2 (Trace Normal)	–	−6.6V
U107 pin 2 (Trace inverted)	–	−4.5V
U420 pin 1,5,6,9	–	−2V
U420 pin 3	–	−7.2V
Q420, Q421 emitters	–	−3.5V

SIGNAL LEVELS IN Y PRE-AMP

Voltages are measured using a 10:1 probe on a general purpose oscilloscope which is A.C. coupled. The oscilloscope under test has its CH1 and CH2 sensitivity controls set to 20 mV/cm and is A.C. coupled. A 160 mV pk-pk squarewave is injected into CH1 with CH1 only selected and the trace centred.

Measured Point		pk-pk Voltage
Q103 emitter	–	40mV
Q105 collector	–	70mV
pin 8 of U104	–	160mV
pin 10 of U420	–	125mV
Q420 collector	–	160mV

A 160mV pk-pk squarewave is injected into CH2 with CH2 only selected.

Measured Point		pk-pk Voltage
Q303 emitter	–	40mV
Q305 collector	–	70mV
pin 8 of U304	–	160mV
pin 10 of U450	–	125mV
Q450 collector	–	160mV

5.5.4 Y AMPLIFIER POTENTIALS AND SIGNAL LEVELS

The Y amplifier (both pre-amp and output sections) potentials and signal levels were measured after the following procedure:-

Select General Mode 41
Select Y1 only, 0.5V/cm
Timebase A 0.2ms/cm
Alphanumerics switched off
Apply 1KHz sinewave to CH1 and adjust to 6cm p-p

NODE	Mean Level	Signal
Q507 emitter	+8.9V	–
base	+8.2V	–
collector	+5.8V	–
Q508 base	+8.9V	–
collector	+11.7V	–
Q503/4 emitter	+4.5V	–
base	+3.8V	–
collector	–0.5V	100mV/cm differential
U502 PIN 15	–3.5V	–
1	–2.0V	–
4,14	–0.5V	100mV/cm differential
2,12	+3.0V	50mV/cm differential
8,9	+3.9V	–
6,11 (=DELAY LINE)	+5.6V	56mV/cm
Q505 collector	0V	22mV/cm
Q506 collector	+0.3	–
Q3001/Q3002		
emitter	+4.9V	–
base	+4.2V	–
collector	–0.3V	600mV/cm differential
Q3007/Q3008		
emitter	–4.9V	146mV/cm differential
base	–5.5V	150mV/cm differential
collector	–11.5V	–
R3034/R3035 junction	–11.65V	–
Q3003/Q3004		
emitter	–5.7V	–
base	–4.9V	146mV/cm differential
collector	+2.7V	600mV/cm differential
PINS 3013/3014	+6.4V	(module virtual earths, 7V–1Vbe)
Y PLATES	+31 to +32 see calibration section	4.6V/cm differential

5.5.5 Y OUTPUT & SAMPLING AMPLIFIER NORMAL OPERATING POTENTIALS AND SIGNAL SENSITIVITIES

Conditions:-
Vertical: CH1 only, Data off, mixed display, trace centred.
Horizontal: TBA only (10μs/cm), Auto trigger.

Location		D.C. Potential	Signal Sensitivity
Delay Line output	Pins 3003,3004	+5.6V	25mV/cm
Q3001,3002	Collectors	–1.8V	
Q3007,3008	Emitters	–4.8V	45mV/cm
Q3003,3004	Collectors	+2.3V	280mV/cm
Output Module	Pins 71,74	+6.0V	
" "	Pins 75,76	+33V	2.5V/cm
U3170	Pins 2,3	–2.9V	
"	Pin 6	–3.8V	40mV/cm
Q3153 3154	Emitters	–3.4V	

Location		D.C. Potential	Signal Sensitivity
" "	Collectors	+8.35V	
Q3151,3152	Collectors	+0.7V	
Q3150	Emitter	OV	120mV/cm
Q3194	Base	+0.7V	
Voltage across R3145,3148		1V	

5.5.6 D.C. OPERATING POTENTIALS IN TRIGGER AMPLIFIER

A Channel Measured Point		Voltage
Q703 base	–	0V
Q705 base	–	0.7V
Q706 base	–	–1V
Q705,Q706 collectors	–	+2.4V
Q715 emitter (X-Y selected)	–	+1.6V
Q715 emitter (T-Y selected)	–	+4V
Q709,Q710 collectors	–	–0.2V
Q711,Q712 collectors	–	+3.3V
U701 pin 5 (+ve trigger)	–	+3.5V
U701 pin 5 (–ve trigger)	–	+4.2V
U701 pin 10 (+ve trigger)	–	+2V
U701 pin 10 (–ve trigger)	–	+3.5V

B Channel Measured Point		Voltage
Q803 base	–	0v
Q805 base	–	–0.74V
Q806 base	–	–1V
Q805,Q806 collectors	–	+3.8V
Q809 collector	–	–0.8V
Q811,Q812 collectors	–	+3.5V
U801 pin 5 (+ve trigger)	–	+4.2V
U801 pin 5 (–ve trigger)	–	+3.5V
U801 pin 10 (+ve trigger)	–	+3.5V
U801 pin 10 (–ve trigger)	–	+2V

SIGNAL LEVELS IN TRIGGER AMPLIFIER

The voltages are measured using a 10:1 probe on a general purpose oscilloscope which is A.C. coupled.
Set the oscilloscope under test as follows:-

CH1 sensitivity	– 20mV/cm, A.C. coupled
A trigger source	– CH1
A trigger slope	– positive
A trigger coupling	– A.C.

Inject an 80mV pk-pk squarewave at 1kHz from a calibrator and centre the trace. Adjust the A trigger level control to give the greatest deflection on Q709 collector.

Measured point		pk-pk Voltage
Q703 emitter	–	75mV
Q706,Q705 collector	–	180mV
Q709,Q710 collector	–	880mV
Q712 collector	–	2.75V
U701 pin 2 (level control adjusted to give stable waveform)	–	0.8V

Next set the oscilloscope under test as follows:-

B trigger source	– CH1
B trigger slope	– positive
B trigger coupling	– A.C.

Adjust the B trigger level control to give the greatest deflection on Q809 collector

Measured point		pk-pk Voltage
Q803 emitter	–	75mV
Q806,Q805 collector	–	160mV
Q809,Q810 collector	–	880mV
Q812 collector	–	2.75V
U801 pin 2 (level control adjusted to give stable waveform)	–	0.8V

Inject a 200mV pk-pk squarewave into the A-EXT Trigger socket. Select external A trigger source.

Measured point		pk-pk Voltage
Q703 emitter	–	75mV

Change input to 2V pk-pk and select ÷10 Ext A Trigger source.

Measured point		pk-pk Voltage
Q703 emitter	–	75mV

Inject a 200mV pk-pk squarewave into the B-EXT Trigger socket. Select external B trigger source.

Measured point		pk-pk Voltage
Q803 emitter	–	75mV

Change input to 2V pk-pk and select ÷10 Ext B Trigger source.

Measured point		pk-pk Voltage
Q803 emitter	–	75mV

TIME-CAL SIGNAL LEVELS

Select General Mode 88 Time-cal ON. Use option 89 to set period to 1ms.

Measured point		pk-pk Voltage
U690 pin 15	–	0.9V
pin 616	–	0.9V

5.5.7 TUBEBASE PCB POTENTIALS AND SIGNAL LEVELS

Conditions. Alternate mode, timebase not running (normal trig with no signal), alpha switched off, stores off. Brill controls at minimum.

NODE	VOLTAGE
Q930 emitter	+82.7V
base	+82V
collector	+76.7V
Q931 base	+76V
collector	+9.8V
Q933 base	0V
collector	–11.2V
Q901–Q904 bases	ECL logic levels
Q920–Q923 bases	ECL logic levels
BRIGHT-UP INPUT	+3.0V
Q934 base	+2.4V
collector	+0.6V
R928/929	+11.5 (pulses to +0.3V during cursors)

5.5.8 TIMEBASE: POTENTIALS AND SIGNAL LEVELS

The potential and normal levels in the analogue section of the timebase were measured after the following setting-up procedure:

Select General Mode 41 to obtain default control settings. Select 'A' INT 'B', 'B' STARTS WITH 'A'. 'A' ramp 50μs/cm. 'B' ramp 20μs/cm. 'A' and 'B' variables in CAL position, minimum hold off no signal inputs. The data refers to 'A' ramp, but, unless otherwise stated, similar values apply to the corresponding points in 'B' ramp.

See Table on following page

5.5.9 X AMP POTENTIALS AND SIGNAL LEVELS

NODE	SIGNAL OR D.C. LEVEL
D1909 cathode	+7.5 ±5%. Controls virtual earth potentials at Q1909 and Q1912 bases.
Q1901,1902 collectors	Complementary ∝ enable, logic levels +7.0 and +8.0V.
PLAB3	∝ analogue input. D.C. bias +2.3V, signal sensitivity 100mV/cm
PLZ1,2	∝ enable, complementary ECL levels.
P1902	Ramp input. Positive ramp from 0 to 4.3V, sensitivity 0.36V/cm without X expansion.
R1926/28	X plates. Mean D.C. level +30.5V Signal sensitivity 8.7V/cm differential.
Q1907/8 collectors	Mean D.C. level +63V, signal as R1926/28.
U1902 pin 6	X shift. Range 0 to 4.2V.
Q1921 base	+2.2V
Q1920 base	5V CMOS level.

VOLT DROP ACROSS:		
R1969	0.1V	Indicates current from –12V rail
R1956	0.8V	" " " +12V rail
R1957	0.5V	" " " +24V rail
R1934	1.8V	" " " +120V rail

The following measurements were made with no ramp running (normal trigger with no signal). 'A' ramp only, and X shift to extreme left.

Q1918 collector	–4.9V	X expansion	OFF
	+3.6V	"	ON
Q1918 base	–7.3V	"	OFF
	–11.6V	"	ON
Q1919 collector	+3.7V	"	OFF
	+2.4V	"	ON
Q1919 base	–11.5V	"	OFF
	–7.2V	"	ON

5.5.10 VOLTAGE GENERATOR POTENTIALS

1. U2529 pin 2: 7V ± 5%
2. U2531 pin 14 & 15: OV ± 0.5V
3. Shift outputs PLAK pins 3,5,7,9 have operating range ± 4.1V.
4. Across C2517: 5V ± 5%
5. Across C2547: 5V ± 5%
6. U2505 outputs swing between ±5V nominal.

FUNCTION	NODE	VOLTAGE	REMARKS
Ramp Output Buffer	U1222 Pin 13	0 to +4.3V	'A' ramp. Q1340 em. = 'B' ramp
	Q1237 Pin 7	+1.5 to +5.8	As 'A' ramp.
	Q1237 Pin 4	−9.3V	
	U1202 Pin 5	0 to 3.6V	As 'A' ramp. U1202 is used in analogue mode as "end of sweep" threshold detector.
Ramp Current Generator	PLV Pin 3	+16.6V	+24.3V in extreme UNCAL position
	" " 4	+16.6V	+22V in extreme UNCAL position
	" " 7	+16.5V	+22V in extreme UNCAL position
	" " 9	+24V	
Flyback Current Generator	Q1230 emitter	(SWITCH) −8V −6.8V	Q1235 is cut off in UNCAL pos. in phase with Aq
	" base	−7.5V	
	" collector	+1.5 to +5.8	As 'A' ramp
	D1229 anode	−11.7V	
Hold-off System (applies to 'A' ramp only)	D1231 anode	−1 to +2.3V	As 'A' ramp. Waveform distortion does not
	Q1229 emitter	−0.6 to +2V	As 'A' ramp. affect performance
	" collector		Hold off ramp. see fig. 4.9.5 of descriptive section. bottom of ramp +3.6V, top depends on timebase speed, from +4V to +12V (Q1228 saturates at low ramp speeds)
	Q1224 collector	(SWITCH) +2 to +4.2V	HOLD OFF, ECL compatible
Hold-off System	PLS Pin 5	−11.4V	0V in maximum hold-off position.
Auto Trig	PLS Pin 8	+3.7V	−0.4V when triggered, a clamped to 0V by Q1246 when in NORMAL TRIG mode.
Bright-up	U1404 Pin 1	−3.8V	(MAX. CONTRAST, −9.8 MIN. CONTRAST OR "A ONLY" −2.9V in X-Y mode)
	" " 2	−2.9V	−9.8V in X-Y mode
	" " 5	−9.8V	−2.9V in X-Y mode
	Q1402 base	−2.2V	
	Q1401 base	(SWITCH) 0 to +1.3V	
Trace Separate	U1408 Pin 1	−3.3V	
	" " 2	−5.6V	
	" " 3	−6.4V	
	" " 4	−5,9V	
	" " 5	−0.4V	
	" " 6	±0.6V	Trace separate range
	" " 7,10	−0.42V	
	" " 8,11	+4.0V	
	" " 9	0V	

5.5.11 GPIB BOARD POTENTIALS

1. Across C2909: 5V ± 5%
2. Across C2905: 5V ± 5%
3. Across C2908: 9.6V ± 1.5V
4. U2932 pin 5: −5V ± 5%
5. Across battery B2901, with instrument power off: 3.6V ± 5%.

5.5.12 C.P.U. BOARD

Voltage across battery, with instrument turned off should be 3.6V ± 5%.

5.6 PROCESSOR HARDWARE INTERFACE

Included below are two tables that together give a guide to the software control of all hardware functions.

5.6.1 PORT INDEX

Gives a tabulation of software port no., address, location and circuit reference.

D.M.	=	Display Management
T/B	=	Timebase
uP	=	Microprocessor
KPD	=	Keypad Assembly
V.G.	=	Voltage Generator
DD	=	Data Display
ACQ	=	Acquisition & Store
IEEE	=	IEEE

Where connector is a number only this refers to the back-plane connector, non-component side.

5.6.2 MASTER INDEX

Lists all ports with the function of each line described.

5.6.1 PORT INDEX

PORT No.	IC No. CCT REF	R/W	ADDRESS (HEX)	CONNECT	BOARD	FUNCTION
01	2412	W	$OD71	63	DM	Y Beam Switch Control
02	2411	W	$OD70	62	DM	Controls, Buzzer
	2452	W	$OD70	62	DM	Reset Sweep Detectors
03	2452	R	$OCO5	42	DM	Ramp Detectors
	2714	R	$OCO5	42	DD	RAM Access
04	1410	W	$OCF2	AD	T/B	Trigger Amp Controls
05	1411	W	$OCF3	AD	T/B	Timebase modes
06	1620	W	$OC76	BY4	T/B	Cursor Ramp Selector
07	1624	W	$OC75	BY10	T/B	Cursor Qualifiers
08	1625	W	$OFOO	AD1	T/B	Cursor Bright-up Sample
09	1570	W	$OC73	BY6	T/B	Delay System (D.S.) Clock
10	1571	W	$OC75	BY8	T/B	(D.S.) Start, Stop Event
11	1572	W	$OC76	BY9	T/B	(D.S.) Modes
12	1576	W	$OC74	BY7	T/B	(D.S.) Prescaler Load Data
13	1573	R	$OCO3	BY2	T/B	(D.S.) Prescaler States
14	2060	W	$0801		uP	(D.S.) TTL Load Data LSE
15	2061	W	$O8OO		uP	(D.S.) TTL Load Data MSB
16	2067	R	$O8O3		uP	(D.S.) TTL Data
17	2068	R	$O8O2		uP	(D.S.) TTL Data
18						UNUSED
19	2049	W	$O8O4		uP	(D.S.) TTL Section Control
20	2050	R	$OC8O		uP	IRQ Source Port
21	2052	W	$OCFO		uP	Programmable Clock
22	1578	W	$OC72	BY5	T/B	A & B Trigger Selector
23	1566	W	$OC7O	BY1	T/B	Word Acquisition Clock
24	1855	W	$OD73	BG9	KPD	Control Addressing
25	1854	R	$OC04	BG11	KPD	Read Selected Control
26	1852	R	$OC86	B96	KPD	Read Keypad Rows
27	1851	R	$OC87	BG8	KPD	Read Keypad Columns
28	1802	W	$OD77	BG3	KPD	Shift Allocation LEDS
29	1801	W	$OD76	BG4	KPD	"Active" Cursor LEDS
30	2526	W	$OD72	64	V.G.	Access, Comparator Control
31	2516	R	$OC83	47	V.G.	Comparator
32	2401	W	$OCF7	61	DM	Y Invert, Penlift
33	2402	R	$OCO6	43	DM	Channel Overloads, Switches
34	2525	W	$OD74	74	V.G.	Shift Scaling

PORT INDEX (CONT)

PORT No.	IC NO. CCT REF	R/W	ADDRESS (HEX)	CONNECT	BOARD	FUNCTION
35	2706	W	SOCF4	58	D.D.	Page Selector
36	2606	W	SOD75	75	ACQ.	Store Selector
37	2607	W	SOCF5	59	ACQ.	uB 0.6, Mode Controls
38	2608	W	SOCF6	60	ACQ.	uB 7–13; ACQ. Request
39	2667	R	SO8O7	44	ACQ.	Single Shot Data
40	2616	R	SOC81	45	ACQ.	Word Latch Data
41	2767	W	SOCF1	55	D.D.	Plotter Controls
42	2965	W	SOBxx	*95	IEEE	Page RAM/ROM Selector

5.6.2 MASTER INDEX

LINE No.	PORT No.	DATA	FUNCTION
3		D_0	DUAL CH.HIGH IN DUAL Y MODE (INC. DUAL & TV).
4		D_1	2Ø HIGH IF ANY 2 OF Y1 Y2 OR T.V. SELECTED (LOW FOR ALL 3)
5		D_2	3Ø HIGH FOR CH1 CH2 TV.
6		D_3	CHOP/$\overline{\text{ALT}}$.MAIN CHOP/ALT CONTROL TO DISPLAY MANAGEMENT
7	01	D_4	T.V. SELECT
8		D_5	L }
9		D_6	M } MODE CONTROL LINES
10		D_7	N }
11		D_0	FORCE HIGH FOR PERMANENT MODE.(MUST BE IN ALT. MODE)
12		D_1	∝ ENABLE LOW DISABLES IF IN ALT MODE.NO EFFECT IN CHOP
13		D_2	RESET 'A' SWEEP DETECTOR } ACTIVE HIGH, DYNAMIC PORTS
14	02	D_3	" 'B' " " } SEE 24, 25 LINES
15		D_4	CHOP STROBE SELECT 1=2MHz, 0=PROG
16		D_5	BUZZER
17		D_6	REAL TIME BLANKING
18		D_7	∝ BLANKING
19		D_0	μP ACCESS TO STORED TRACE RAM –0=ACCESS ALLOWED
20		D_1	AQ, A RAMP GATE FROM TIMEBASE
21		D_2	
22		D_3	
34	03	D_4	IEEE $\overline{\text{INSERTED}}$
24		D_5	'A' SWEEP DETECT } (RESET BY LINES 13,14)
25		D_6	'B' SWEEP DETECT } 1=THERE HAS BEEN A COMPLETE SWEEP.
26		D_7	μP ACCESS TO CHAR.RAM –0=ACCESS ALLOWED
27		D_0	$\overline{\text{SINGLE SHOT}}$ ($\overline{\text{SS}}$). SINGLE SHOT MODE FOR 'A' RAMP
28		D_1	ARM SS. ARMS SS IF 29. FIRES SS IMMEDIATELY IF 29.
29		D_2	INHIBIT AUTO. TRIG.
30	04	D_3	TRIG. VIEW SIGNAL INHIBIT
31		D_4	$\overline{\text{ENABLE}}$: FORCE B TO START WITH A.
32		D_5	CONFIGURE Y FOR REALTIME ACQUISITION.
33		D_6	
34		D_7	

MASTER INDEX (CONT)

LINE No.	PORT No.	DATA	FUNCTION
35		D_0	RESET B. DISABLES B RAMP.
36		D_1	B STARTS AFTER DELAY. 1 FOR GATED B START
37		D_2	X10 GAIN (EXPANDED); LOW FOR X10
38	05	D_3	A INTENS. B.
39		D_4	A ALT. B
40		D_5	B ONLY
41		D_6	A ONLY
42		D_7	SELECT EXT X TO X AMP A TRIG. SOURCE (X-Y MODE)
43		D_0	CURSOR 1 ON A RAMP
44		D_1	CURSOR 2 ON A RAMP
45		D_2	CURSOR 3 ON A RAMP
46	06	D_3	CURSOR 4 ON A RAMP
47		D_4	CURSOR 1 ON B
48		D_5	CURSOR 2 ON B
49		D_6	CURSOR 3 ON B
50		D_7	CURSOR 4 ON b
51		D_0	ALT/$\overline{\text{CHOP}}$ 0=SINGLE SAMPLE ACQUISITION
52		D_1	DUAL B START. 1=C1 ALT C3 TO B START LATCH
53		D_2	$\overline{\text{ENABLE}}$ DELAY COUNTER B START
54	07	D_3	DUAL CHANNEL. 1 = ENABLE CURSOR CHANNEL QUALIFIERS
55		D_4	$\overline{\text{ENABLE}}$ C1 B START } IF BOTH $\overline{\text{ENABLE}}$, THEN
56		D_5	$\overline{\text{ENABLE}}$ C3 B START } LINE 52 MUST = 0
57		D_6	
58		D_7	$\overline{\text{ENABLE}}$ AQ. TO START B RAMP
59		D_0	$\overline{\text{ENABLE}}$ C4 BRIGHT-UP
60		D_1	$\overline{\text{ENABLE}}$ C3 BRIGHT-UP INDIVIDUAL BRIGHT-UP ON/OFF
61		D_2	$\overline{\text{ENABLE}}$ C2 BRIGHT-UP DOES NOT AFFECT ANY OTHER
62	08	D_3	$\overline{\text{ENABLE}}$ C1 BRIGHT-UP FUNCTION.
63		D_4	$\overline{\text{ENABLE}}$ C4 SAMPLE
64		D_5	ENABLE C3 SAMPLE INDIVIDUAL SAMPLE ENABLE.
65		D_6	$\overline{\text{ENABLE}}$ C2 SAMPLE ONLY ONE CURSOR NORMALLY
66		D_7	ENABLE C1 SAMPLE ENABLED

MASTER INDEX (CONT)

LINE No.	PORT No.	DATA	FUNCTION
67		D_0	$\overline{\text{SELECT}}$ Ao — TRIG SOURCE
68		D_1	$\overline{\text{SELECT}}$ Bo — TRIG SOURCE; COUNTER CLOCK SOURCE
69		D_2	$\overline{\text{SELECT}}$ 100MHz — COUNTER CLOCK SOURCE
70	09	D_3	SELECT MODE 3
71		D_4	$\overline{\text{SELECT}}$ MODE 3
72		D_5	$\overline{\text{PHASE SHIFT}}$ ↓ FOR 1 UNIT OF PHASE SHIFT
73		D_6	ASYNC. START FREE RUN COUNTER FOR ÷ N MODE
74		D_7	ASYNC. STOP
75		D_0	$\overline{A}$ — DELAY COUNTER — START EVENT SELECTOR,
76		D_1	$\overline{B}$ — DELAY COUNTER — START EVENT SELECTOR,
77		D_2	$\overline{C}$ — DELAY COUNTER — START EVENT SELECTOR,
78	10	D_3	$\overline{D}$ — DELAY COUNTER — START EVENT SELECTOR,
79		D_4	$\overline{A}$ — DELAY COUNTER — STOP EVENT SELECTOR.
80		D_5	$\overline{B}$ — DELAY COUNTER — STOP EVENT SELECTOR.
81		D_6	$\overline{C}$ — DELAY COUNTER — STOP EVENT SELECTOR.
82		D_7	$\overline{D}$ — DELAY COUNTER — STOP EVENT SELECTOR.
83		D_0	$\overline{\text{A TRIG SOURCE TO B.T.B,}}$
84		D_1	
85		D_2	INHIBIT SINGLE SHOT COUNT. LOW TO SELECT SS COUNT MODE
86	11	D_3	ARM SINGLE SHOT COUNT. NEGATIVE EDGE TO ARM SS COUNT.
87		D_4	FORCE S1. 1 TO PARALLEL LOAD PRE-SCALER.
88		D_5	MODE $1/\overline{2}$ HIGH FOR N=2–16, LOW FOR N ⩾ 17.
89		D_6	$\overline{\text{ENABLE}}$ Bo QUALIFIER — QUALIFY COUNTER START EVENT
90		D_7	$\overline{\text{ENABLE}}$ Ao QUALIFIER — "GHOST AQ/BQ"
91		D_0	DO — MAIN — PARALLEL LOAD DATA FOR PRE-SCALER
92		D_1	$\overline{D1}$ — MAIN — PARALLEL LOAD DATA FOR PRE-SCALER
93		D_2	$\overline{D2}$ — MAIN — PARALLEL LOAD DATA FOR PRE-SCALER
94	12	D_3	$\overline{D3}$ — MAIN — PARALLEL LOAD DATA FOR PRE-SCALER
95		D_4	DO — AUX FOR PHASE SHIFT (LOAD AS FOR N + 1)
96		D_5	$\overline{D1}$ — AUX FOR PHASE SHIFT (LOAD AS FOR N + 1)
97		D_6	$\overline{D2}$ — AUX FOR PHASE SHIFT (LOAD AS FOR N + 1)
98		D_7	$\overline{D3}$ — AUX FOR PHASE SHIFT (LOAD AS FOR N + 1)

MASTER INDEX (CONT)

LINE No.	PORT No.	DATA		FUNCTION
99		D_0	$\overline{D0}$	
100		D_1	$\overline{D1}$	READ DATA FROM PRE-SCALER (DELAY COUNTER)
101		D_2	$\overline{D2}$	
102		D_3	$\overline{D3}$	
103	13	D_4	SINGLE SHOT SET (=COUNTER HAS NOT STARTED SINCE LAST ARM)	
104		D_5	COUNTER RUNNING.	
105		D_6		
106		D_7		
107		D_0	D3	
108		D_1	4	
109		D_2	5	
110	14	D_3	6	TTL SECTION, LSB.
111		D_4	7	
112		D_5	8	
113		D_6	9	
114		D_7	10	
				PARALLEL LOAD DATA FOR DELAY COUNTER (TTL SECTION)
115		D_0	D11	
116		D_1	12	
117		D_2	13	
118		D_3	14	
119	15	D_4	15	
120		D_5	16	TTL SECTION, LSB.
121		D_6	17	
122		D_7	18	
123		D_0	D3	
124		D_1	4	
125		D_2	5	
126	16	D_3	6	READ DELAY COUNTER (TTL SECTION)
127		D_4	7	
128		D_5	8	
129		D_6	9	
130		D_7	10	

MASTER INDEX (CONT)

LINE No.	PORT No.	DATA	FUNCTION	
131		D_0	D11	
132		D_1	12	
133		D_2	13	
134	17	D_3	14	READ DELAY COUNTER (CONT'D)
135		D_4	15	TTL SECTION MSB
136		D_5	16	
137		D_6	17	
138		D_7	18	
139		D_0		
140		D_1		
141		D_2		
142	18	D_3		NOT CONNECTED
143		D_4		
144		D_5		
145		D_6		
146		D_7		
147		D_0	FORCE L.C. WHEN $\overline{148}$	
148		D_1	$\overline{\text{ENABLE}}$ L.C. IMPULSE LO	
149		D_2	$\overline{\text{DISABLE}}$ L.C. PULSE LO	
150		D_3	$\overline{\text{CLEAR COUNTER IRQ}}$; DISABLE ~~IRQ~~ IF HELD LO	
151	19	D_4		
152		D_5		
153		D_6		
154		D_7		
155		D_0	DELAY COUNTER	
156		D_1	V-GEN	
157		D_2	SHIFT	
158	20	D_3	IEEE	IRQ SOURCE PORT
159		D_4	KEYPAD	
160		D_5	25ms REGULAR	
161		D_6	END OF CAPTURE	
162		D_7		

MASTER INDEX (CONT)

LINE No.	PORT No.	DATA	FUNCTION
163	21	D_0	PROGRAMMABLE CLOCK DIVIDER DATA
164		D_1	
165		D_2	
166		D_3	
167		D_4	A
168		D_5	B — PROGRAMMABLE CLOCK DECADE SELECTOR
169		D_6	C
170		D_7	$\overline{\text{ENABLE}}$ PROGRAMMABLE CLOCK
171	22	D_0	$\overline{\text{A TRIG DIRECT}}$
172		D_1	$\overline{\text{A TRIG DELAYED}}$ (N=1)
173		D_2	$\overline{\text{A TRIG DELAYED}}$ (N 1)
174		D_3	$\overline{\text{A TRIG IEEE}}$
175		D_4	$\overline{\text{B TRIG DIRECT}}$
176		D_5	$\overline{\text{STOPWATCH MODE}}$
177		D_6	$\overline{\text{B TRIG DELAYED}}$
178		D_7	'B' TRIG.= TIME CAL $\overline{\text{ENABLE}}$
179	23	D_0	$\overline{\text{ENABLE}}$ CURRENT CURSOR SYNC.
180		D_1	$\overline{\text{ENABLE}}$ CURRENT SURSOR ASYNC. — SEE "WORD TRIGGER" FOR DETAILS
181		D_2	$\overline{\text{ENABLE}}$ TRIGGER WORD SAMPLING
182		D_3	$\overline{\text{ENABLE}}$ BLOCK CLOCK
183		D_4	$\overline{\text{ENABLE}}$ SAMPLE AFTER DELAY
184		D_5	CLEAR S1
185		D_6	
186		D_7	
187	24	D_0	TIMEBASE A — ADDRESS LINES TO FRONT PANEL CONTROL, WHICH ARE THEN READ ON PORT 25
188		D_1	TIMEBASE B
189		D_2	CH1 ATTENUATOR
190		D_3	CH2 ATTENUATOR
191		D_4	SINGLE LINE CONTROLS
192		D_5	
193		D_6	
194		D_7	$\overline{\text{MASK KEYPAD IRQ}}$. RESET OR MASK FOR LINE 159

MASTER INDEX (CONT)

LINE No.	PORT No.	DATA	FUNCTION
195	25	D_0	READ FRONT PANEL CONTROL STATUS
196		D_1	
197		D_2	
198		D_3	
199		D_4	
200		D_5	
201		D_6	
202		D_7	
203	26	D_0	KEYPAD ROWS
204		D_1	
205		D_2	
206		D_3	
207		D_4	
208		D_5	
209		D_6	SPINWHEEL OUTPUT
210		D_7	
211	27	D_0	KEYPAD COLUMNS
212		D_1	
213		D_2	
214		D_3	
215		D_4	
216		D_5	
217		D_6	
218		D_7	KEYPAD IRQ, (BY-PASSES MASK)
219	28	D_0	C1 — CURSOR POSITION — SHIFT LEDS
220		D_1	C2 — CURSOR POSITION — SHIFT LEDS
221		D_2	C3 — SHIFT LEDS
222		D_3	C4 — SHIFT LEDS (0 = LED ON)
223		D_4	CH1 — SHIFT LEDS
224		D_5	CH2 — SHIFT — SHIFT LEDS
225		D_6	X
226		D_7	

MASTER INDEX (CONT)

LINE No.	PORT No.	DATA	FUNCTION
227	29	D_0	C1
228		D_1	C2
229		D_2	C3 — "ACTIVE CURSOR" LEDS. 0 = LED ON
230		D_3	C4
231		D_4	
232		D_5	
233		D_6	
234		D_7	
235	30	D_0	VOLTAGE GENERATOR EXTERNAL ACCESS REQUEST
236		D_1	
237		D_2	
238		D_3	SELECT COMPARATOR SOURCES
239		D_4	(VOLTAGE GENERATOR)
240		D_5	
241		D_6	
242		D_7	
243	31	D_0	
244		D_1	
245		D_2	
246		D_3	
247		D_4	
248		D_5	
249		D_6	
250		D_7	READ COMPARATOR (SEE LINES 236–240)
251	32	D_0	
252		D_1	RESET Y CHANNEL OVERLOAD DETECTORS ↓
253		D_2	INVERT CH1
254		D_3	INVERT CH2
255		D_4	CONFIGURE Y FOR DUAL REALTIME ACQUISITION
256		D_5	PENLIFT 1 = CLOSE RELAY CONTACTS
257		D_6	
258		D_7	

MASTER INDEX (CONT)

LINE No.	PORT No.	DATA	FUNCTION
259		D_0	READ CH1 OVERLOAD (Ø= OVERLOAD)
260		D_1	READ CH2 OVERLOAD (Ø= OVERLOAD)
261		D_2	READ CH1 GND ("1" = GROUNDED)
262		D_3	READ CH2 GND
263	33	D_4	READ CH1 AC/$\overline{DC}$
264		D_5	READ CH2 AC/$\overline{DC}$
265		D_6	
266		D_7	
267		D_0	SHIFT SCALING
268		D_1	
269		D_2	
270		D_3	
271	34	D_4	
272		D_5	
273		D_6	
274		D_7	
275		D_0	DISPLAY PAGE 1 OF NUMERICS
276		D_1	DISPLAY PAGE 2 OF NUMERICS
277		D_2	DISPLAY STORE 1 TRACE
278	35	D_3	DISPLAY STORE 2 TRACE
279		D_4	CHOP/$\overline{ALT}$ TIE TO LINE 6
280		D_5	$\overline{ENABLE}$ DOT JOINING (HARDWARE OVERRIDE IN CHOP)
281		D_6	ENABLE TRACE REPLAY (LOW FOR ALL ACQN. MODES) μB3
282		D_7	μB14 ON ACQUISITION
283		D_0	$\overline{PRE\text{-}TRIG\ ACQUISITION}$
284		D_1	UNCONDITIONAL AQ ENABLE (⎍ TO START PRE-TRIG ACQ) (⎍306 FIRST)
285		D_2	μB15 — ACQN. STORE SELECTORS — CH1 → STORE — DO NOT SELECT
286		D_3	μB16 — ACQN. STORE SELECTORS — CH2 → STORE — 285–287
287	36	D_4	μB17 — ACQN. STORE SELECTORS — CH1 → STORE — OR
288		D_5	μB18 — ACQN. STORE SELECTORS — CH2 → STORE — 286–288
289		D_6	ENABLE POD DELAY
290		D_7	RESET STORE ADDRESS COUNTER

MASTER INDEX (CONT)

LINE No.	PORT No.	DATA	FUNCTION
291	37	D_0	μB0
292		D_1	μB1 — ACQUISITION MODE CONTROLS
293		D_2	μB2
294		D_3	μB10
295		D_4	μB5
296		D_5	μB4
297		D_6	μB6
298		D_7	μB19
299	38	D_0	μB7
300		D_1	μB8
301		D_2	μB9
302		D_3	ENABLE READ CLOCK
303		D_4	μB12
304		D_5	μB11
305		D_6	μB13
306		D_7	ACQUISITION REQUEST ⌐ ENABLE CAPTURE (TRACE OR SINGLE)
307	39	D_0	ANALOGUE TO DIGITAL CONVERTER DATA (USED IN SINGLE SHOT ACQUISITION)
308		D_1	
309		D_2	
310		D_3	
311		D_4	
312		D_5	
313		D_6	
314		D_7	
315	40	D_0	WORD ACQUISITION DATA
316		D_1	
317		D_2	
318		D_3	
319		D_4	
320		D_5	
321		D_6	
322		D_7	

MASTER INDEX (CONT)

LINE No.	PORT No.	DATA	FUNCTION
323		D_0	
324		D_1	
325		D_2	
326	41	D_3	
327		D_4	PLOT MARKER OUTPUT
328		D_5	1 FOR FIRQ ENABLE (GENERATED ON PROG. CLK)
329		D_6	1 FOR TRANSFER CLK ENABLE } TO PLOTTER
330		D_7	1 FOR PROG. CLK ENABLE } TO PLOTTER
331		D_0	HARDWARE POWER-UP /RESTART DATA = 0
332		D_1	BINARY ADDRESS OF PAGE SELECTOR
333		D_2	BINARY ADDRESS OF PAGE SELECTOR
334		D_3	ENABLE "PAGED" RAM AND ROM
335	42	D_4	
336		D_5	
337		D_6	
338		D_7	
		D_0	
		D_1	
		D_2	
		D_3	
		D_4	
		D_5	
		D_6	
		D_7	
		D_0	
		D_1	
		D_2	
		D_3	
		D_4	
		D_5	
		D_6	
		D_7	

ABBREVIATIONS USED FOR COMPONENT DESCRIPTIONS

RESISTORS

CC	Carbon Composition	½W	10%	unless otherwise stated
CF	Carbon Film	¼W	5%	unless otherwise stated
MO	Metal Oxide	½W	2%	unless otherwise stated
MF	Metal Film	¼W	1%	unless otherwise stated
WW	Wire Wound	6W	5%	unless otherwise stated
CP	Control Potentiometer		20%	unless otherwise stated
PCP	Preset Potenitometer Type MPD, PC		20%	unless otherwise stated

CAPACITORS

CE(1)	Ceramic		+80% -25%	
CE(2)	Ceramic	500V	±10%	unless otherwise stated
CE(3)	Ceramic	50V		
SM	Silver Mica			
PF	Plastic Film		±10%	unless otherwise stated
PS	Polystyrene			
PE	Polyester		±10%	unless otherwise stated
PC	Polycarbonate			
E	Electrolytic (Aluminium)		+50% -10%	
T	Tantalum		+50% -10%	

5110 'Y' PRE-AMP

Ref	Value	Description	Tol %±	Rating	Part No.	Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS											
R101	1M	MF			451606	R157	30k	MF	2		38629
R102	56	CF			28715	R158	1k5	MF	2		38598
R103	1M	MF			450981	R159	10k	CF			21809
R104	22	CF		1/8W	43142	R160	12k	MF	2		38620
R105	22	CF		1/8W	43142	R161	3k	MF	2		38605
R106	82	CF		1/8W	43149						
R107	330k	CF			32357	R163	1k	PCP			39233
R108	10k	CF			21809	R164	330	CF			28721
R109	3k3	CF			21803	R165	330	CF			28721
R110	6k8	CF			21807	R166	100	MF	2		38570
R111	47	CF			28714	R167	100	MF	2		38570
R112	10	CF			21793	R168	510	MF	2		38587
R113	1k5	CF			21801	R169	1k	CF			21799
R114	47	CF			28714	R170	27	CF			28711
R115	22M	CC			451727	R171	470	CF			21797
R116	680	MF	2		38590	R172	330	CF			28721
R117	10	CF			21793	R173	100	CF		1/8W	43150
R118	100	CF		1/8W	43150	R174	100	CF		1/8W	43150
R119	150	MF	2		38574	R175	1k	CF			21799
R120	1k6	MF	2		38599	R176	33	CF		1/8W	43144
R121	1k6	MF	2		38599	R177	33	CF		1/8W	43144
R122	10	CF			21793	R178	5k	CP			39234
						R179	20k	PCP			39235
R124	820	MF	2		38592	R180	50k	PCP			39268
R125	820	MF	2		38592	R181	200	PCP			39231
R126	1k8	MF	5		28725	R182	50	PCP			39267
R127	100	CF			21794	R183	100	PCP			39230
R128	100	CF			21794	R184	1k	PCP			39233
R129	470	CF			21797	R185	270	CF		1/8W	43716
R130	100	CF		1/8W	43150	R186	330	CF			28721
R131	100	CF		1/8W	43150	R187	330	CF			28721
R132	100	CF			21794	R188	1k1	MF	2		38595
R133	390	CF			28722						
R134	22	CF			28710	R193	10k	MF	2		38618
R135	10	CF			21793	R194	3k6	MF	2		38607
R136	1k2	MF	2		38596	R195	3k6	MF	2		38607
R137	1k2	MF	2		38596	R196	47k	CF			21815
R138	47	CF		1/8W	43146	R197	10k	PCP			39265
R139	47	CF		1/8W	43146	R198	33k	CF			21814
R140	10	CF			21793	R199	1M5	MF	0.5		451801
R142	47	CF		1/8W	43146	R201	470	CF			21797
R143	47	CF			28714	R202	100	CF			21794
R144	47	CF			28714	R203	470	CF			21797
R145	100	CF		1/8W	43150	R204	100	CF			21794
R146	100	CF		1/8W	43150	R205	100	CF			21794
R147	22	CF			28710	R206	100	CF			21794
R148	270	MF	2		38580	R207	100	CF			21794
R149	270	MF	2		38580	R208	100	CF			21794
R150	470	MF	2		38586						
R151	3k9	MF	2		38608	R251	470	CF			21797
R152	47	CF		1/8W	43146	R252	100	CF			21794
R153	47	CF		1/8W	43146	R253	470	CF			21797
R154	10k	MF	2		38618	R254	100	CF			21794
R155	13k	MF	2		38621						
R156	750	MF	2		38591	R301	1M	MF			451606

5110 'Y' PRE-AMP (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
R302	56	CF			28715
R303	1M	MF			450981
R304	22	CF		1/8W	43142
R305	22	CF		1/8W	43142
R306	82	CF		1/8W	43149
R307	330k	CF			32357
R308	10k	CF			21809
R309	3k3	CF			21803
R310	6k8	CF			21807
R311	47	CF			28714
R312	10	CF			21793
R313	1k5	CF			21801
R314	47	CF			28714
R315	22M	CC			451727
R316	680	MF	2		38590
R317	10	CF			21793
R318	100	CF			43150
R319	150	MF			38574
R320	1k6	MF	2		38599
R321	1k6	MF	2		38599
R322	10	CF			21793
R324	820	MF	2		38592
R325	820	MF	2		38592
R326	1k8	CF			28725
R327	100	CF			21794
R328	100	CF			21794
R329	470	CF			21797
R330	100	CF		1/8W	43150
R331	100	CF		1/8W	43150
R332	100	CF			21794
R333	390	CF			28722
R334	22	CF			28710
R335	10	CF			21793
R336	1k2	MF	2		38596
R337	1k2	MF	2		38596
R338	47	CF		1/8W	43146
R339	47	CF		1/8W	43146
R340	10	CF			21793
R342	47	CF			28714
R343	47	CF			28714
R344	47	CF			28714
R345	100	CF		1/8W	43150
R346	100	CF		1/8W	43150
R347	22	CF			28710
R348	270	MF	2		38580
R349	270	MF	2		38580
R350	470	MF	2		38586
R351	3k9	MF	2		38608
R352	47	CF		1/8W	43146
R353	47	CF		1/8W	43146
R354	10k	MF	2		38618
R355	13k	MF	2		38621
R356	750	MF	2		38591
R357	30k	MF	2		38629
R358	1k5	MF	2		38598
R359	10k	CF			21809
R360	12k	MF	2		38620
R361	3k	MF	2		38605
R363	1k	PCP			39233
R364	330	CF			28721
R365	330	CF			28721
R366	100	MF	2		38570
R367	100	MF	2		38570
R368	510	MF	2		38587
R369	1k	CF			21799
R370	27	CF			28711
R371	470	CF			21797
R372	330	CF			28721
R373	100	CF		1/8W	43150
R374	100	CF		1/8W	43150
R375	1k	CF			21799
R376	33	CF		1/8W	43144
R377	33	CF		1/8W	43144
R378	5k	CP			39234
R379	20k	PCP			39235
R380	50k	PCP			39268
R381	200	PCP			39231
R382	50	PCP			39267
R383	100	PCP			39230
R384	1k	PCP			39233
R385	270	CF		1/8W	43716
R386	330	CF			28721
R387	330	CF			28721
R388	1k1	MF	2		38595
R393	10k	MF	2		38618
R394	3k6	MF	2		38607
R395	3k6	MF	2		38607
R396	47k	CF			21815
R397	10k	PCP			39265
R398	33k	CF			21814
R399	1M5	MF	0.5		451801
R409	150	CF			28719
R410	10	CF			21793
R411	10	CF			21793
R412	680	CF			28723
R413	680	CF			28723
R414	10	CF			21793
R415	270	CF			28720
R416	270	CF			28720
R420	2k2	CP			A4/42993
R421	10	CF			21793
R422	680	CF			28723
R423	3k	MF	2		38605
R424	3k	MF	2		38605
R425	560	MF	2		38588
R426	560	MF	2		38588

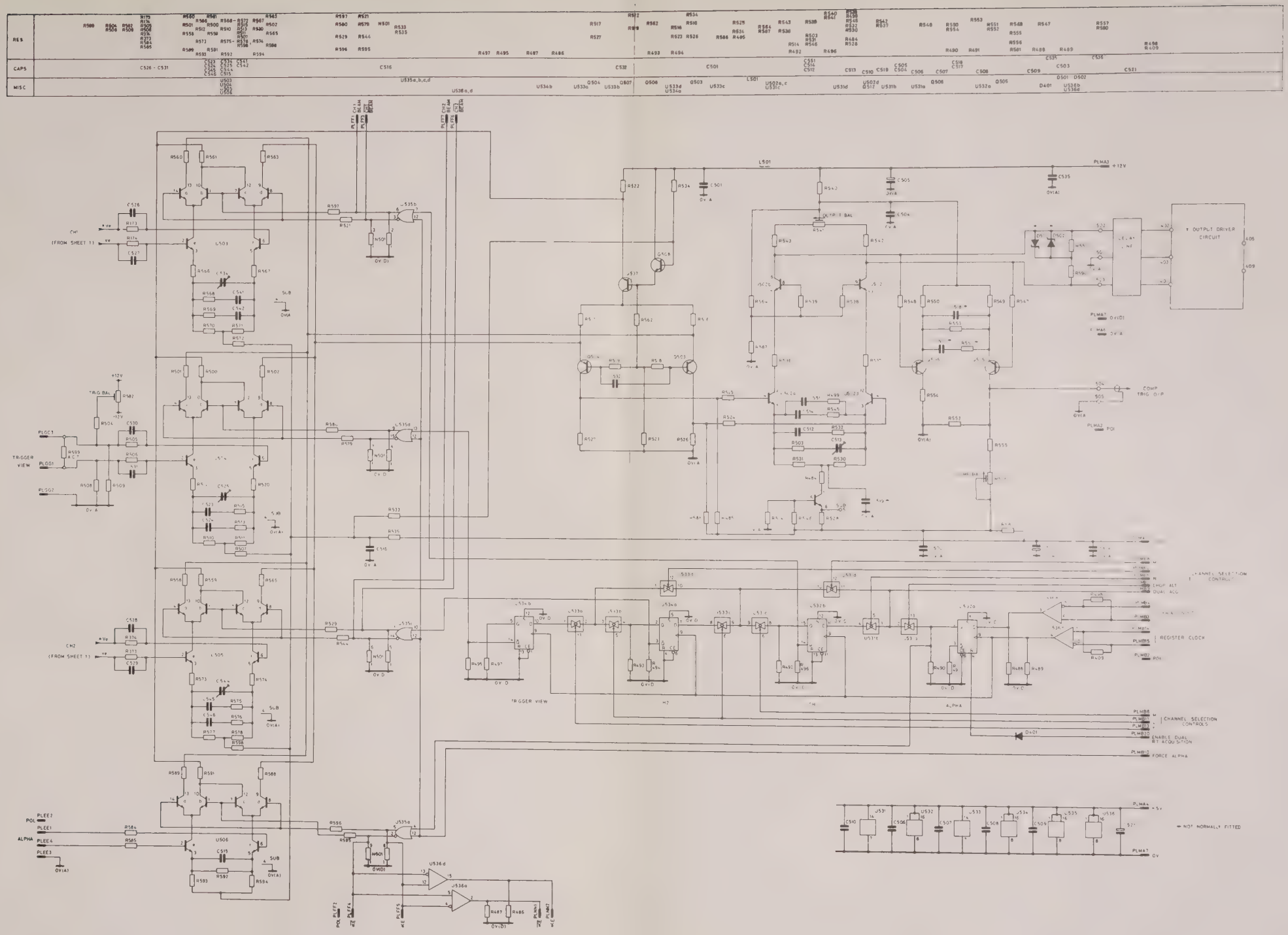


Fig. 6.1(a) Pre-amplifier Circuit Diagram

5110 'Y' PRE-AMP (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
R555	1k5	CF			21801
R556	1k	PCP			39233
R557	150	MF	2		38574
R558	47	CF			28714
R559	68	CF			28716
R560	47	CF			28714
R561	68	CF			28716
R562	820	MF	5		38592
R563	47	CF			28714
R564	2k2	CF			21802
R565	47	CF			28714
R566	22	CF		1/8W	43142
R567	22	CF		1/8W	43142
R568	6k8	CF		1/8W	43245
R569	2k2	CF		1/8W	43357
R570	47	CF			28714
R571	47	CF			28714
R572	1k2	MF	2		38596
R573	22	CF		1/8W	43142
R574	22	CF		1/8W	43142
R575	2k2	CF		1/8W	43357
R576	6k8	CF		1/8W	43245
R577	47	CF			28714
R578	47	CF			28714
R579	100	MF	5		21794
R580	100	MF	5		21794
R581	10	MF	5		21793
R582	10k	PCP			39268
R583	3k9	CF		1/8W	44231
R584	100	CF			21794
R585	100	CF			21794
R586	1k2	MF	2		38596
R587	1k2	CF			21800
R588	47	CF			28714
R589	47	CF			28714
R590	75	MF	2		38567
R591	68	CF			28716
R592	470	MF	2		38586
R593	2k2	MF	2		38602
R594	2k2	MF	2		38602
R595	100	CF			21794
R596	100	CF			21794
R597	100	CF		1/8W	43150
R598	1k2	MF	2		38596
R599	390	CF A.O.T.			28722
N501	560 x 8	Resistor Network			39258
N502	22k	Resistor Network			451373
CAPACITORS					
C101	10nF	CE(3)		25V	450548
C102	3.3pF	CE(3)			42402
C103	120pF	CE(3)			42421
C104	10pF	CE(3)			36606
C105	1nF	CE(3)			42432
C106	470pF	CE(3)			42428
C107	8.2pF	CE(3)			36605
C108	10nF	CE(3)		25V	450548
C109	10nF	CE(3)		25V	450548
C110	10nF	CE(2)		250V	22395
C112	10nF	CE(3)		25V	450548
C114	10nF	CE(3)		25V	450548
C115	1nF	CE(3)			42432
C116	10nF	CE(3)		25V	450548
C117	10nF	CE(3)		25V	450548
C118	1nF	CE(3)			42432
C119	100nF	CE(3)			43498
C120	1.5pF	CE(2)			40356
C121	10nF	CE(3)		25V	450548
C122	10nF	CE(3)		25V	450548
C123	3.3pF	CE(3)			36600
C129	10nF	CE(3)		25V	450548
C130	2.2pF	CE(3)			42400
C131	39pF	CE(3)			42415
C133	10nF	CE(3)		25V	450548
C134	10nF	CE(3)		25V	450548
C136	10nF	CE(3)		25V	450548
C137	220pF	CE(3)			42424
C139	5.6pF	CE(3)			42405
C140	220pF	CE(2)			451625
C141	10nF	CE(3)		25V	450548
C142	2.2pF	CE(3)			36598
C143	2.2pF	CE(2)			44361
C144	22µF	T		35V	35932
C145	5.6nF	CE(2)			22394
C201	2n2	CE(3)			42436
C202	2n2	CE(3)			42436
C203	2n2	CE(3)			42436
C204	2n2	CE(3)			42436
C206	2n2	CE(3)			42436
C207	2n2	CE(3)			42436
C208	2n2	CE(3)			42436
C209	2n2	CE(3)			42436
C210	2n2	CE(3)			42436
C251	2n2	CE(3)			42436
C252	2n2	CE(3)			42436
C253	2n2	CE(3)			42436
C254	2n2	CE(3)			42436
C255	2n2	CE(3)			42436
C256	2n2	CE(3)			42436
C257	2n2	CE(3)			42436

5110 'Y' PRE-AMP (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS (Cont.)					
C258	2n2	CE(3)			42436
C259	2n2	CE(3)			42436
C260	2n2	CE(3)			42436
C261	2n2	CE(3)			42436
C301	10nF	CE(3)		25V	450548
C302	3.3pF	CE(3)			42402
C303	120pF	CE(3)			42421
C304	10pF	CE(3)			36606
C305	1nF	CE(3)			42432
C306	470pF	CE(3)			42428
C307	8.2pF	CE(3)			36605
C308	10nF	CE(3)		25V	450548
C309	10nF	CE(3)		25V	450548
C310	10nF	CE(2)		250V	22395
C312	10nF	CE(3)		25V	450548
C314	10nF	CE(3)		25V	450548
C315	1nF	CE(3)			42432
C316	10nF	CE(3)		25V	450548
C317	10nF	CE(3)		25V	450548
C318	1nF	CE(3)			42432
C319	100nF	CE(3)			43498
C320	1.5pF	CE(2)			40356
C321	10nF	CE(3)		25V	450548
C322	10nF	CE(3)		25V	450548
C323	3.3pF	CE(3)			36600
C329	10nF	CE(3)		25V	450548
C330	2.2pF	CE(3)			42400
C331	39pF	CE(3)			42415
C333	10nF	CE(3)		25V	450548
C334	10nF	CE(3)		25V	450548
C336	10nF	CE(3)		25V	450548
C337	220pF	CE(3)			42424
C339	5.6pF	CE(3)			42405
C340	220pF	CE(2)			451625
C341	10nF	CE(3)		25V	450548
C342	2.2pF	CE(3)			36598
C343	1pF	CE(3)		500V	40357
C344	22µF	CE(3)		35V	35932
C345	5.6nF	CE(3)		500V	22394
C400	10nF	CE(2)		250V	22395
C420	10nF	CE(2)			42569
C421	1pF	CE(3)			36594
C422	1pF	CE(3)			36594
C423	10nF	CE(2)			42569
C450	10nF	CE(2)			42569
C451	1pF	CE(3)			36594
C452	1pF	CE(3)			36594
C453	10nF	CE(2)			42569
C471	10nF	CE(2)		250V	22395
C472	10nF	CE(2)		250V	22395
C473	100nF	CE(2)		25V	36709
C501	10nF	CE(3)		25V	450548
C502	10nF	CE(3)		25V	450548
C503	22µF	E		25V	32181
C504	10nF	CE(3)		25V	450548
C505	22µF	E		25V	32181
C506	10nF	CE(3)		25V	450548
C507	10nF	CE(3)		25V	450548
C508	10nF	CE(3)		25V	450548
C509	10nF	CE(3)		25V	450548
C510	10nF	CE(3)		25V	450548
C511	1500pF	CE(2)			22388
C512	39pF	CE(2)			22371
C513	2/28pF	Trimmer			43501
C514	10pF	CE(2)			22364
C515	5.6pF	CE(3)			42405
C516	10nF	CE(3)		25V	450548
C517	1500pF	CE(2)			22388
C518		Not Fitted			
C519	8.2pF	CE(3)			42407
C521	22µF	E		25V	32181
C523	330pF	CE(3)			43438
C524	12pF	CE(3)			36607
C525	4/27pF	Trimmer			36273
C526	2.2pF	CE(3)			36598
C527	2.2pF	CE(3)			36598
C528	2.2pF	CE(3)			36598
C529	2.2pF	CE(3)			36598
C530	2.2pF	CE(3)			36598
C531	2.2pF	CE(3)			36598
C532	5.6pF	CE(3)			42405
C534	4/27pF	Trimmer			36273
C535	10nF	CE(3)		25V	450548
C536	10nF	CE(3)		25V	450548
C541	150pF	CE(3)			451799
C542	12pF	CE(3)			36607
C544	4/27pF	Trimmer			36273
C545	12pF	CE(3)			36607
C546	150pF	CE(3)			451799
Q101		AE37			40414
Q102		BF371			36275
Q103		MPSH10			40315

5110 'Y' PRE-AMP (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS (Cont.)					
Q104		BF479			39270
Q105		BF479			39270
Q301		AE37			40414
Q302		BF371			36275
Q303		MPSH10			40315
Q304		BF479			39270
Q305		BF479			39270
Q420		MPSH10			40315
Q421		MPSH10			40315
Q450		MPSH10			40315
Q451		MPSH10			40315
Q503		BF479			39270
Q504		BF479			39270
Q505		BF479			39270
Q506		BF479			39270
Q507		2N3906			21533
Q508		2N3904			24146
DIODES					
D100		IN4149			1949
D101		2811			452034
D102		2811			452034
D104		IN3595			29330
D105	8V2	ZENER			33933
D107		IN4149			1949
D110		IN4148			23802
D112	10V	ZENER			33935
D201		IN4148			23802
D202		IN4148			23802
D203		IN4148			23802
D251		IN4148			23802
D252		IN4148			23802
D253		IN4148			23802
D300		IN4149			1949
D301		2811			452034
D302		2811			452034
D304		IN3595			29330
D305	8V2	ZENER			33933
D307		IN4149			1949
D310		IN4148			23802
D312	10V	ZENER			33935
D401		IN4148			23802
U101		LF355BN			42050
U102		SL360C			42126
U103		SL2364 (Selected)			451912
U104		SL3145			43980
U105		741			36736
U107		MC3386			450978
U301		LF355BN			42050
U302		SL360C			42126
U303		SL2364 (Selected)			451912
U304		SL3145			43980
U305		741			36736
U307		MC3386			450978
U420		SL3145CDP			43980
U450		SL3145CDP			43980
U501		LM3302			450917
U502		CA3145			451910
U503		SL2364			451913
U504		SL2364			451913
U505		SL2364			451913
U506		SL2364			451913
U531		4066			40044
U532		10131			39246
U533		4066			40044
U534		10131			39246
U535		10101			41062
U536		10115			450928
MISCELLANEOUS					
S201					450846
S251					450846
L101					26986
L102					26986
L301					26986
L302					26986
L501					26986
T101					A4/43216
T301					A4/43216
PLAY					41391
PLAZ					41391

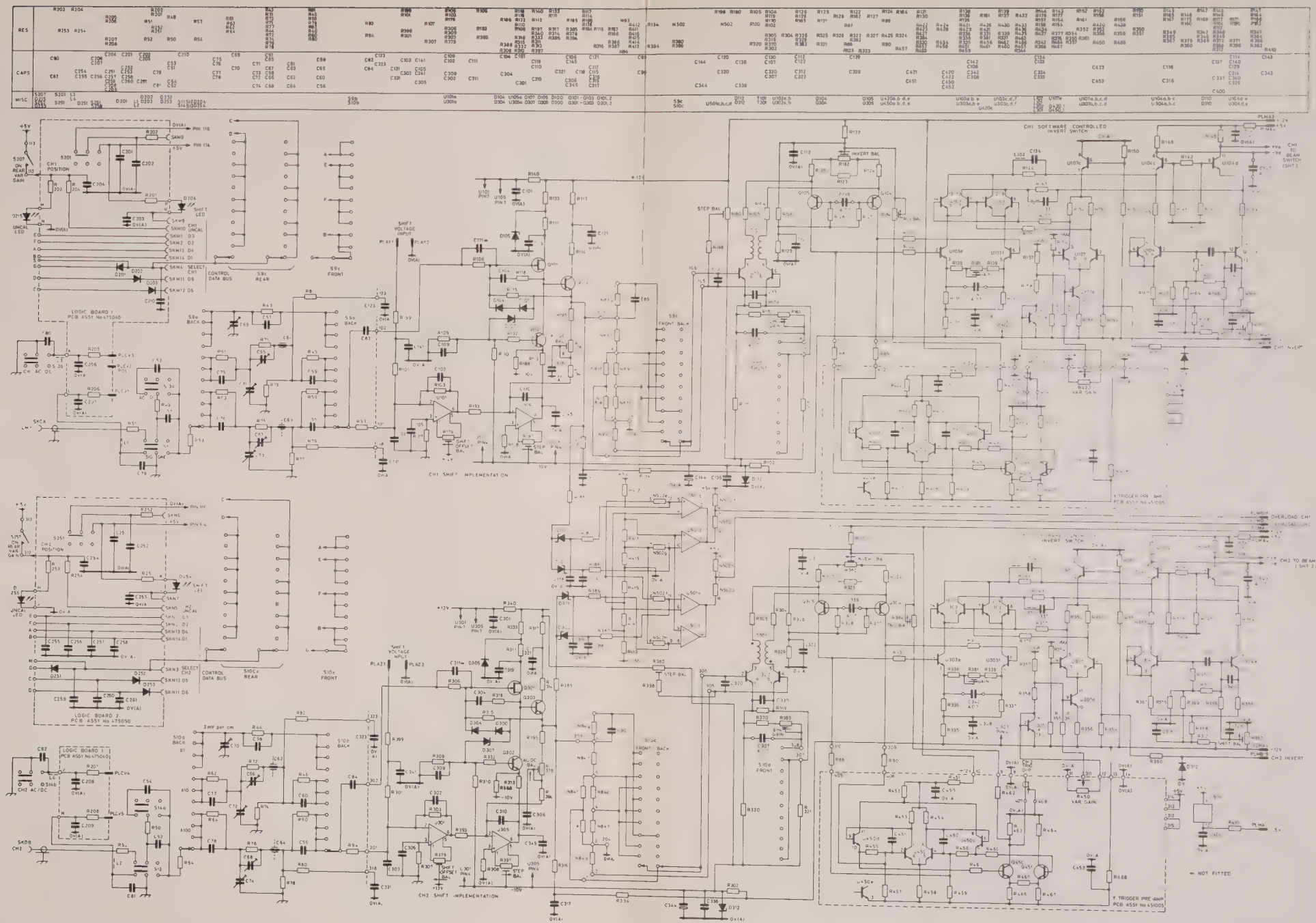


Fig. 6.1(b) Pre-amplifier Circuit Diagram

5110 Y OUTPUT & SAMPLING

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R3001	91	MF	2		38569
R3003	91	MF	2		38569
R3005	100	CF			21794
R3006	100	CF			21794
R3007	470	CF			21797
R3008	820	CF			28724
R3009	820	CF			28724
R3010	820	CF			28724
R3011	330	CF			28721
R3012	270	CF			28720
R3013	270	CF			28720
R3014	220	CF			21796
R3015	91	MF	2		38569
R3016	91	MF	2		38569
R3017	390	CF			28722
R3018	390	CF			28722
R3020	12k	CF			21810
R3021	4k7	CF			21805
R3022	470	CF			21797
R3023	180	CF			21795
R3024	470	CF			21797
R3025	150	CF		A.O.T.	28719
R3026	150	MF	2		38574
R3027	150	MF	2		38574
R3028	100	CF			21794
R3029	10	CF			21793
R3030	47	CF			28714
R3031	47	CF			28714
R3032	47	CF			28714
R3033	47	CF			28714
R3034	22	CF			28710
R3035	22	CF			28710
R3036	100	CF			21794
R3037	100	CF			21794
R3038	10	CF			21793
R3039	1k5	CF			21801
R3040	10	CF			21793
R3041	47	CF			28714
R3042	33	CF		A.O.T.	28712
R3043	100	CF			21794
R3044	2k7	CF			28726
R3045	2k7	CF			28726
R3046	10	CF			21793
R3047	22	CF			43142
R3048	22	CF			43142
R3049	10	CF			21793
R3051	10k+10k	CP	With S3002		A4/451168
R3052	10k+10k	CP	With S3002		A4/451168
R3053	470	CF			21797
R3054	680	CF			28723
R3055	6M2	CF			42132
R3056	1M	CP			450835

Ref	Value	Description	Tol %±	Rating	Part No
R3057	470	CF			21797
R3058	2k2	CP			450838
R3059	39	WW		2½W	451168
R3060	1k	CP			450920
R3061	680	CF			28723
R3062	470	CF			21797
R3063	4k7	CF			21805
R3064	4k7	CF			21805
R3065	6k8	CF			21807
R3066	6k8	CF			21807
R3067	47	CF			28714
R3068	470	CF			21797
R3069	470	CF			21797
R3101	560	CF			44223
R3102	560	CF			44223
R3103	120	CF			43713
R3104	1k	CF			44226
R3105	120	CF			43713
R3108	100	CF			43150
R3109	100	CF			43150
R3110	47	CF			28714
R3113	560	CF			44223
R3114	560	CF			44223
R3117	560	CF			44223
R3118	560	CF			44223
R3119	120	CF			43713
R3120	82	CF			28717
R3121	120	CF			28718
R3122	82	CF			28717
R3123	120	CF			28718
R3124	4R7	CF			29433
R3125	820	CF			28724
R3126	82	CF			28717
R3127	120	CF			28718
R3128	82	CF			28717
R3129	120	CF			28718
R3131	1k	MF	2		38594
R3132	330	CF			28721
R3135	47	MF	2		38562
R3136	47	CF			28714
R3137	330	CF			28721
R3140	3k	CF			41186
R3141	24k	MF			38855
R3142	36k	MF			450934
R3143	12k	MF			450506
R3144	3k	CF			41186
R3145	30	MF			450932
R3146	4R7	CF			29433
R3147	4R7	CF			29435

5110 Y OUTPUT & SAMPLING (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
R3148	30	MF			450932
R3149	12k	MF			450506
R3150	10k	CF			21809
R3151	39k	MF			38632
R3152	10	CF			21793
R3153	270	CF			18543
R3154	68	MF			450933
R3155	330	MF	2		38582
R3156	330	CF			28721
R3157	330	CF			28721
R3158	180	CF			21795
R3159	10	CF			43138
R3160	22	CF			43142
R3161	200	CP			39231
R3162	10	CF			43138
R3163	22	CF			43142
R3164	68	MF			450933
R3165	330	MF	2		38582
R3166	820	CF			28724
R3167	820	CF			28724
R3168	180	CF			21795
R3169	1k	CF			21799
R3170	10k	MF	2		38618
R3171	10k	MF	2		38618
R3172	10k	MF	2		38618
R3173	10k	MF	2		38618
R3174	10k	CP			39265
R3175	39k	MF	2		38632
R3176	10k	MF	2		38618
R3177	150	MF	½		40526
R3178	150	MF	½		40526
R3179	2k2	CF			21802
R3180	150	MF	½		40526
R3181	2k2	CF			21802
R3182	150	MF	½		40526
R3183	27	CF			43143
R3184	100k	CP			39269
R3185	1M	CF			31840
R3186	10M	CF			32661
R3187	1k	CF			21799
R3188	1k8	CF		A.O.T.	28725
R3189	330	CF			28721
R3190	2k7	CF			38604
R3191	1k2	CF			38596
R3192	27	CF		1/8W	43143
R3198	1k8	CF		A.O.T.	28725
R3199	36k	MF			450934
R3200	2k2	CF			43357
R3201	2k2	CF			43357
R3202	2k2	CF			43357
R3203	2k2	CF			43357
R3204	100	CF			43150
R3205	100	CF		1/8W	43150
R3207	100	CP			39230
R3208	560	CF		1/8W	44223
R3212	560	CF		1/8W	44223
R3213	560	CF		1/8W	44223
R3214	560	CF		1/8W	44223
R3215	47	CF		1/8W	43146
R3216	47	CF		1/8W	43146
CAPACITORS					
C3001	8.2pF	CE(3)			42407
C3002	100nF	CE(3)			43498
C3003	8.2pF	CE(3)			42407
C3004	1nF	CE(2)			22387
C3007	47µF	T		35V	35933
C3008	10nF	CE(3)			42444
C3009	560pF	CE(3)			42429
C3010	560pF	CE(3)			42429
C3011	10nF	CE(3)			42444
C3013	10nF	CE(3)			42444
C3015	10nF	CE(3)			42444
C3016	10nF	CE(3)			42444
C3017	10pF	CE(3)			42408
C3018	10pF	CE(3)			42408
C3020	18pF	CE(2)			22367
C3021	5.6pF	CE(2)			22361
C3022	1.5/9pF	Trimmer			36272
C3023	4/27pF	Trimmer			36273
C3036	5.6pF	CE(3)			42405
C3037	5.6pF	CE(3)			42405
C3101	100nF	CE(3)			43498
C3102	10nF	CE(3)			42444
C3103	10nF	CE(3)			42444
C3104	1nF	CE(3)			42432
C3105	1nF	CE(3)			42432
C3106	10pF	CE(3)			42408
C3107	10pF	CE(3)			42408
C3108	3.3nF	CE(3)			42438
C3109	10nF	CE(3)			42444
C3110	56pF	CE(3)			42417
C3111	56pF	CE(3)			42417
C3113	100nF	CE(3)			43498
C3114	100nF	CE(3)			43498
C3115	1nF	CE(2)			22387
C3116	1nF	CE(2)			22387
C3117	10nF	CE(3)			42444
C3118	10pF	CE(2)			22364
C3120	10µF	E		25V	32180
C3121	10µF	E		25V	32180

5110 Y OUTPUT & SAMPLING (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS (Cont.)					
C3122	10µF	E		25V	32180
C3123	10µF	E		25V	32180
C3124	10µF	E		25V	32180
C3125	10µF	E		25V	32180
C3130	4.7µF	T		35V	53249
C3131	4.7µF	T		35V	53249
C3133	100µF	T		10V	53571
C3138	100µF	T		10V	53571
C3144	4.7µF	T		35V	53249
C3145	10µF	E		25V	32180
C3148	10µF	E		25V	32180
C3150	5.6pF	CE(3)			36603
C3151	100nF	CE(3)			43498
C3152	1nF	CE(3)			42432
C3153	10nF	CE(3)			42444
C3154	10pF	CE(3)			42408
C3155	1.2/10pF	Trimmer			451127
C3156	100nF	CE(3)			43498
C3157	10µF	E		25V	32180
C3158	10µF	E		25V	32180
C3159	100nF	CE(3)			43498
C3160	22µF	CE(3)			36610
C3161	5/45pF	Trimmer			36274
C3162	47pF	CE(3)			36614
C3163	33µF	CE(3)			36612
C3164	10pF	CE(3)			42408
C3165	10nF	CE(3)		250V	22395
C3166	10nF	CE(2)		250V	22395
C3170	15pF	CE(3)			42410
C3177	10nF	CE(3)			42444
C3178	5.6pF	CE(3)			42405
C3179	22pF	CE(3)			42412
C3180	5.6pF	CE(3)			42405
C3181	22pF	CE(3)			42412
C3183	27pF	CE(2)		400V	451937
C3184	27pF	PS			450516
C3186	10nF	CE(3)			42444
C3187	100nF	CE(3)			43498
C3188	100nF	CE(3)			43498
C3189	10nF	CE(3)			42444
C3192	5.6pF	CE(2)			22361
C3198	22pF	CE(2)		A.O.T.	22368
C3199	22pF	CE(2)		A.O.T.	22368

Ref	Value	Description	Tol %±	Rating	Part No
DIODES					
D3001		IN4148			23802
D3050		IN4148			23802
D3051		IN4148			23802
D3052	9V1	ZENER			33934
D3115		2811			452034
D3116		2811			452034
D3120		MBD101			452032
D3121		MBD101			452032
D3122		MBD101			452032
D3123		MBD101			452032
D3124		2811			452034
Q3001		BF479			39270
Q3002		BF479			39270
Q3003		ZTX326A			41753
Q3004		ZTX326A			41753
Q3005		2N5771			38089
Q3006		2N5771			38089
Q3007		BF479			39270
Q3008		BF479			39270
Q3050		BFX88			23337
Q3051		BFY51			29329
Q3110		BF480			450674
Q3111		BF480			450674
Q3112		BF479			39270
Q3113		BF479			39270
Q3115		BFT96 or BFQ23			450675
Q3116		BFR96			39019
Q3120		2N3906			21533
Q3121		BC192B			33205
Q3122		BC212			29327
Q3123		2N3904			24146
Q3150		BFR96			39019
Q3151		BFQ51			451882
Q3152		BFQ51			451882
Q3153		BF480			450674
Q3154		BF480			450674
Q3190		NPD5565			450919
Q3191		NPD5565			450919
Q3193		BC547B			450546
Q3194		BC547B			450546
MISCELLANEOUS					
L3001		FX1242			26986

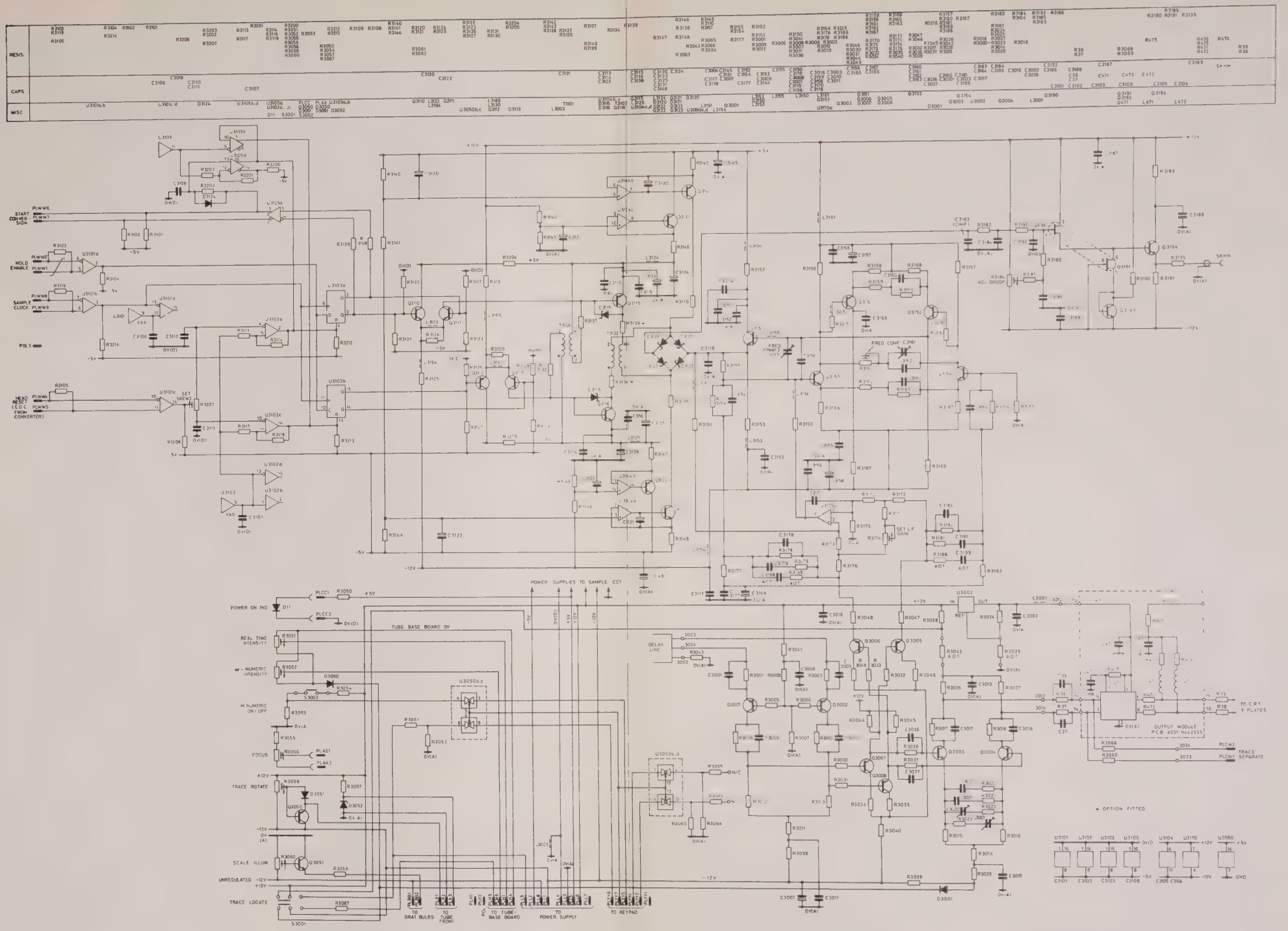


Fig. 6.2 Y Output and Sampling Circuit Diagram

5110 TIMEBASE

Ref	Value	Description	Tol %±	Rating	Part No	Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS											
R1201	4k7	CF			21805	R1257	22k	CF			21812
R1202	180	CF			21795	R1258	15	CF			28708
R1203	2k2	CF			21802	R1259	3k3	CF			21803
R1204	2k2	CF			21802	R1260	47	CF			28714
R1205	3k3	CF			21803	R1261	910	CF	2		38593
R1206	4k7	CF			21805	R1262	27	CF		1/8W	43143
R1207	6k8	CF			21807	R1263	470Ω	CF			21797
R1208	560	CF			21798	R1264	10	CF		1/8W	43138
R1209	1k5	CF			21801	R1265	10	CF		1/8W	43138
R1210	270	CF			28720	R1266	10	CF		1/8W	43138
R1211	3k3	MF	2		38606	R1267	10	CF		1/8W	43138
R1212	470	MF	2		38586	R1268	10	CF		1/8W	43138
R1213	220	MF	2		38578	R1269	36	MF	2		38559
R1214	390	CF			28722	R1270	56	CF			28715
R1215	3k3	CF			21803	R1271	68k	CF			21816
R1216	330	CF			44220	R1272	15k	MF	2		38622
R1217	5k6	CF		1/8W	44233	R1273	39k	CF			28728
R1218	3k3	CF			21803	R1274	13k	MF	2		38621
R1219	3k3	CF		1/8W	43358	R1275	50k	CP			42157
R1220	10	CF			21793	R1276	39k	CF			28728
R1221	820	MF	2		38592	R1277	5k6	CF			21806
R1222	1k2	CF			21800	R1278	6k8	CF			21807
R1223	10k	CF			21809	R1279	6k8	CF			21807
R1224	360	MF	2		38583	R1280	27k	CF		1/8W	44239
R1225	6k8	CF			21807	R1281	2k7	CF		1/8W	44230
R1226	1k5	CF			21801						
R1227	470	CF			21797	R1289	1k	MF	2		38594
R1228	10	CF			21793	R1290	1k5	MF	2		38598
R1229	270k	CF			32330						
R1230	150k	MF	2		38640	R1292	2k2	MF	2		38602
R1231	15k	CF			28727						
R1232	3k3	CF			21803	N1201	560x8	Resistor Network			39258
R1233	8k2	CF			21808						
R1234	47	CF			28714	R1308	560	CF			21798
R1235	10k	CF			21809						
R1236	1k5	CF			21801	R1311	1k8	MF	2		28725
R1237	510	MF	2		38587	R1312	470	MF	2		21797
R1238	220k	MF	2		38650	R1313	220	MF	2		21796
R1239	10k	CF			21809						
R1240	8k2	CF			21808	R1316	330	CF		1/8W	44220
R1241	15k	CF			28727	R1317	5k6	CF		1/8W	44233
R1242	560	CF			21798						
R1243	1k5	CF			21801	R1319	3k3	CF		1/8W	43358
R1244	220	CF			21796	R1320	10	CF			21793
R1245	1k5	CF			21801	R1321	820	MF	2		38592
R1246	2k2	MF	2		38602	R1322	1k2	CF			21800
R1247	47	CF			28714						
R1248	12k	CF			21810	R1324	360	MF	2		38583
R1249	33k	CF			21814	R1325	6k8	CF			21807
R1250	470k	CF			32330	R1326	1k5	CF			21801
R1251	470k	CF			32330	R1327	470	MF	2		21797
R1252	470	CF			21797	R1328	10	CF			21793
R1253	2k7	CF			28726						
R1254	10k	CF			21809	R1331	15k	CF			28727
R1255	5k	CP			42156						
R1256	12k	CF			21810	R1333	8k2	CF			21808

5110 TIMEBASE (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
R1336	1k5	CF			21801
R1337	510	MF	2		38587
R1340	8k2	CF			21808
R1341	15k	CF			28727
R1342	560	CF			21798
R1343	1k5	CF			21801
R1344	220	MF	2		21796
R1345	1k5	CF			21801
R1347	47	MF	2		28714
R1348	12k	CF			21810
R1349	33k	CF			21814
R1350	470k	CF			32330
R1351	470k	CF			32330
R1354	10k	CF			21809
R1355	5k	CP			42156
R1357	22k	CF			21812
R1358	15	CF			28708
R1360	47	MF	2		28714
R1361	910	MF	2		38593
R1362	2k7	CF			28726
R1366	27	MF	2		38556
R1367	2k2	MF	2		38602
R1368	3k3	MF	2		28606
R1370	56	MF	2		28715
R1371	68k	CF			21816
R1372	15k	MF	2		38622
R1373	39k	MF	2		28728
R1374	13k	MF	2		38621
R1375	50k	CP			42157
R1376	39k	CF			28728
R1377	5k6	CF			21806
R1380	470	MF	2		21797
R1381	6k8	MF	2		36814
R1382	8k2	MF	2		21808
R1385	470	MF	2		21797
R1386	680	CF			28723
R1387	3k9	CF			21804
R1389	36	MF	2		38559
R1391	2k	PCP			40178
N1301	560x8	Resistor Network			39258
R1401	4k7	MF	2		38610
R1402	1k5	MF	2		38598
R1403	1k5	MF	2		38598
R1404	2k2	CF			21802
R1405	2k2	CF			21802
R1406	2k2	CF			21802
R1407	1k8	CF			38600
R1408	3k6	MF	2		38607
R1409	10k	CF			21809
R1410	180	MF	2		21795
R1411	2k2	CF			21802
R1412	2k2	CF			21802
R1413	2k2	CF			21802
R1414	180	MF	2		21795
R1418	180	CF		1/8W	43715
R1420	9k1	MF	2		38617
R1421	1k5	MF	2		38598
R1422	1k5	MF	2		38598
R1424	470	MF	2		21797
R1425	560	MF	2		38588
R1426	56	MF	2		38564
R1427	56	MF	2		38564
R1430	220	MF	2		21796
R1431	1k5	MF	2		38598
R1432	1k	MF	2		38594
R1433	1k5	MF	2		38598
CAPACITORS					
C1202	10nF	CE(3)			42444
C1206	560pF	CE(3)			42429
C1207	680pF	CE(3)			42430
C1209	33pF	CE(3)			42414
C1210	27pF	CE(3)			42413
C1212	68pF	CE(3)			42418
C1214	10nF	CE(3)			42444
C1216	10pF	CE(2)			22364
C1220	10nF	CE(3)			42444
C1222	56pF	CE(2)			22373
C1223	10nF	CE(3)			42444
C1225	47pF	CE(3)			42416
C1226	0.1µF	CE(2)		63V	451072
C1227	10nF	CE(2)		100V	39190
C1230	10nF	CE(3)			42444
C1231	10nF	CE(3)			42444
C1232	10nF	CE(3)			42444
C1233	10nF	CE(3)			42444

5110 TIMEBASE (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS (Cont.)					
C1236	10nF	CE(3)			42444
C1240	100nF	CE(3)			43498
C1244	220pF	CE(2)			22379
C1245	2.2µF	CE(4)		63V	451071
C1246	22nF	CE(2)		100V	450118
C1247	10µF	E		10V	40353
C1249	56pF	CE(2)			22373
C1250	150pF	CE(2)		100V	43587
C1251	3/45pF	Trimmer			43504
C1270	100nF	CE(2)		100V	37018
C1271	10µF	E		25V	32180
C1304	10nF	CE(2)		50V	42444
C1312	68pF	CE(2)		50V	42418
C1316	10pF	CE(2)			22364
C1320	10nF	CE(2)		250V	22395
C1322	56pF	CE(2)			22373
C1323	50V	CE(3)			42444
C1324	10µF	E		25V	32180
C1330	10nF	CE(3)			42444
C1331	10µF	E		25V	32180
C1332	10nF	CE(3)			42444
C1334	10µF	E		25V	32180
C1336	10nF	CE(2)			22395
C1344	220pF	CE(3)			42424
C1345	2.2µF	PC		63V	451071
C1346	22nF	CE(2)		100V	450118
C1347	10µF	E		10V	40353
C1349	56pF	CE(2)			42417
C1350	150pF	CE(2)		100V	43587
C1351	3/45pF	Trimmer			43504
C1370	100nF	CE(2)		100V	37018
C1372	22µF	T		35V	35932
C1380	10nF	CE(3)			42444
C1381	10nF	CE(3)			42444
C1401	10nF	CE(3)			42444
C1402	10nF	CE(3)			42444
C1403	10nF	CE(3)			42444
C1404	10nF	CE(3)			42444
C1405	10nF	CE(3)			42444
C1406	10nF	CE(3)			42444
C1408	47µF	T		35V	53249
C1409	10nF	CE(3)			42444
C1410	10nF	CE(3)			42444
C1411	10nF	CE(3)			42444
DIODES					
D1201		IN4148			23802
D1202		IN4148			23802
D1203		IN4148			23802
D1204		IN4148			23802
D1205		IN4148			23802
D1206		IN4148			23802
D1208		IN4148			23802
D1209		IN4148			23802
D1222		IN4148			23802
D1223		IN4148			23802
D1225		IN4148			23802
D1226		IN4148			23802
D1229	3V9	ZENER			33925
D1230		IN4148			23802
D1231		IN4148			23802
D1233		IN4148			23802
D1236		IN4148			23802
D1237		IN4148			23802
D1238	2V7	ZENER			33921
D1240		IN4148			23802
D1241		IN4148			23802
D1306		IN4148			23802
D1322		IN4148			23802
D1329	3V9	ZENER			33925
D1330		IN4148			23802
D1333		IN4148			23802
D1336		IN4148			23802
D1337		IN4148			23802
D1340		IN4148			23802
D1341		IN4148			23802
D1342		IN4148			23802
D1401		IN4148			23802
D1402		IN4148			23802
D1403	10V	ZENER			33935
D1404		IN4148			23802

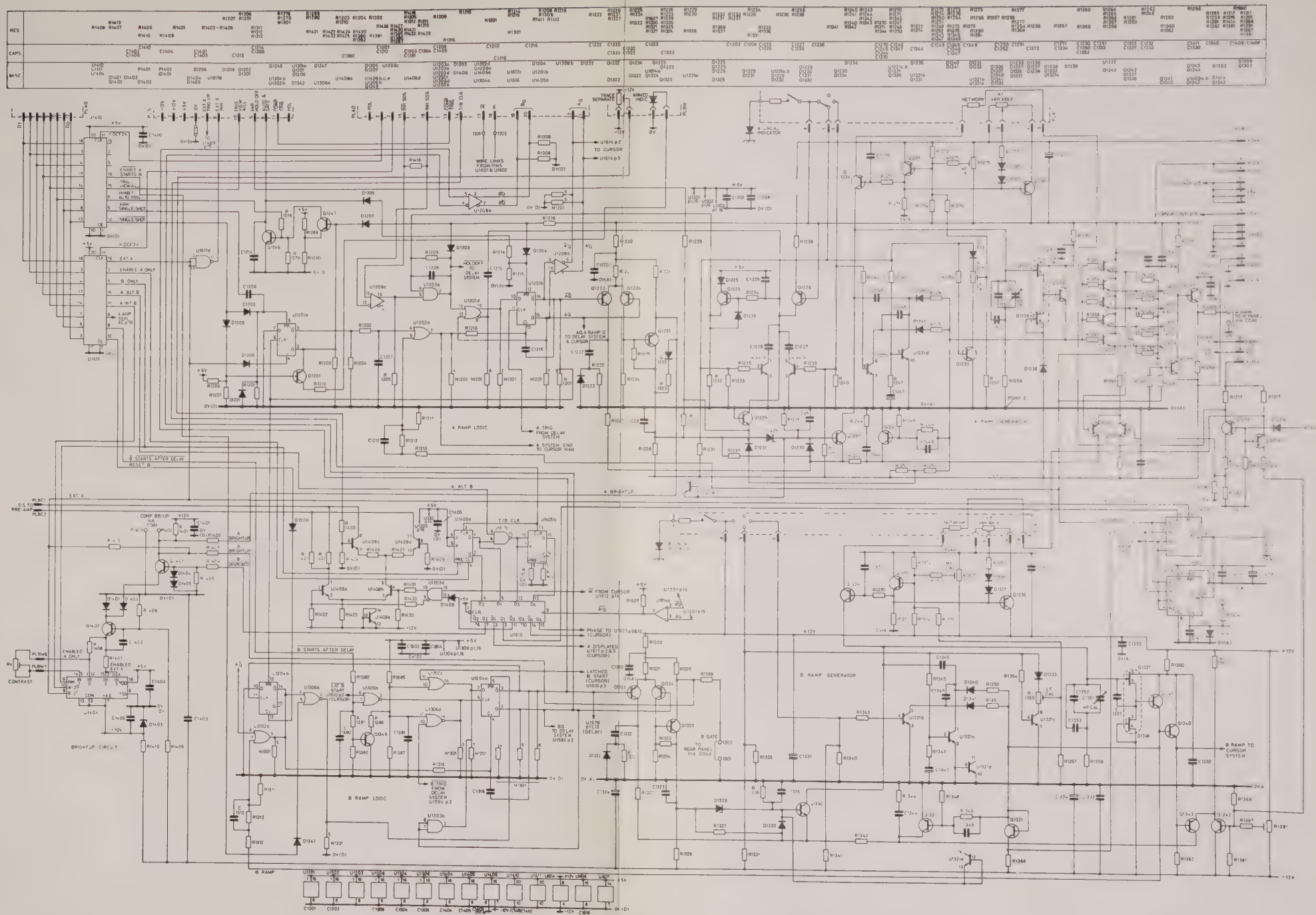


Fig. 6.3 Timebase Circuit Diagram

5110 'X' OUTPUT & DRIVER

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1901	3k3	CF			21803
R1902	220	CF			21796
R1903	680	CF			28723
R1904	9k1	MF	2		38617
R1905	9k1	MF	2		38617
R1906	1k3	MF	2		38597
R1907	220	CF			21796
R1908	270	MF	2		38580
R1909	270	MF	2		38580
R1910	22	CF			28710
R1911	22	CF			28710
R1012	430	MF	2		38585
R1913	47	CF			28714
R1914	2k2	PCP			36868
R1915	220	PCP			35881
R1916	47	CF			28714
R1917	2k2	PCP			36868
R1918	36k	MO			28811
R1919	68	CF			28716
R1920	680	CF			28723
R1921	10k	CF			21809
R1922	10k	CF			21809
R1923	22	CF			28710
R1924	100	CF			21794
R1925	36k	MO			28811
R1926	100	CF			21794
R1927	150k	MF	2		38646
R1928	100	CF			21794
R1929	22	CF			28710
R1930	150k	MF	2		38646
R1931	22	CF			28710
R1932	680	CF			28723
R1933	75	MO			28780
R1934	100	CF			21794
R1935	36k	MO			28811
R1936	68	CF			28716
R1937	680	CF			28710
R1938	100	CF			21794
R1939	10k	MF	2		38618
R1940	10k	MF	2		38618
R1941	6k8	CF			21807
R1942	6k8	CF			21807
R1943	51k	MF	2		38635
R1944	22	CF			28710
R1945	2k2	MF	2		38602
R1946	10k	PCP			39848
R1947	5k6	MF	2		38612
R1948	1k	PCP			35880
R1949	470	MF	2		38586
R1950	270	CF			28720
R1951	2k2	MF	2		38602
R1952	22	CF			28710
R1954	10	CF			21793
R1955	51k	MF	2		38635
R1956	10	CF			21793
R1957	22	CF			28710
R1958	22	CF			28710
R1959	4k7	MF	2		38610
R1960	470	MF	2		38586
R1961	470	PCP			37419
R1962	470	MF	2		38586
R1963	470	PCP			37419
R1964	4k3	MF	2		38609
R1965	24k	MF	2		38627
R1966	10k	CF			21809
R1967	2k2	CF			21802
R1968	220	CF			21796
R1969	10	CF			21793
R1970	22	CF			28710
R1971	220	CF			21796
R1972	220	CF			21796
R1973	680	MF	2		38590
R1974	22	CF			28710
R1975	47k	CF			21815
R1976	560	CF			21798
R1979	100k	CF			21819
R1980	33k	CF			21814
R1981	39k	CF			28728
R1982	100k	CP			42173
R1983	82k	CF			21818
R1984	1M	CP			42174
R1985	220k	CF			21823
R1987	820	MF	2		38592
R1988	820	MF	2		38592
R1989	470	CF			21797
R1990	470	CF			21797
R1991	120	CF			28718
R1992	47	CF			28714
N1901		Resistor Network			A3/450622
CAPACITORS					
C1901	10µF	E		25V	32180
C1902	150nF	PE		250V	35601
C1903	39pF	CE(3)			42415
C1904	1.5pF	CE(2)			40356
C1905	33µF	E		16V	32173
C1906	9pF	Trimmer			36272
C1907	150pF	CE(3)			42422
C1908	33µF	E		16V	32173
C1909	10nF	CE(3)		200V	450119
C1910	10nF	CE(3)		200V	450119
C1911	10nF	CE(3)		200V	450119
C1912	10nF	CE(3)		200V	450119
C1913	10nF	CE(3)			42444
C1914	10nF	CE(3)			42444
C1915	100nF	CE(3)			43498
C1916	10nF	CE(3)			42444
C1917	10nF	CE(3)		200V	450119

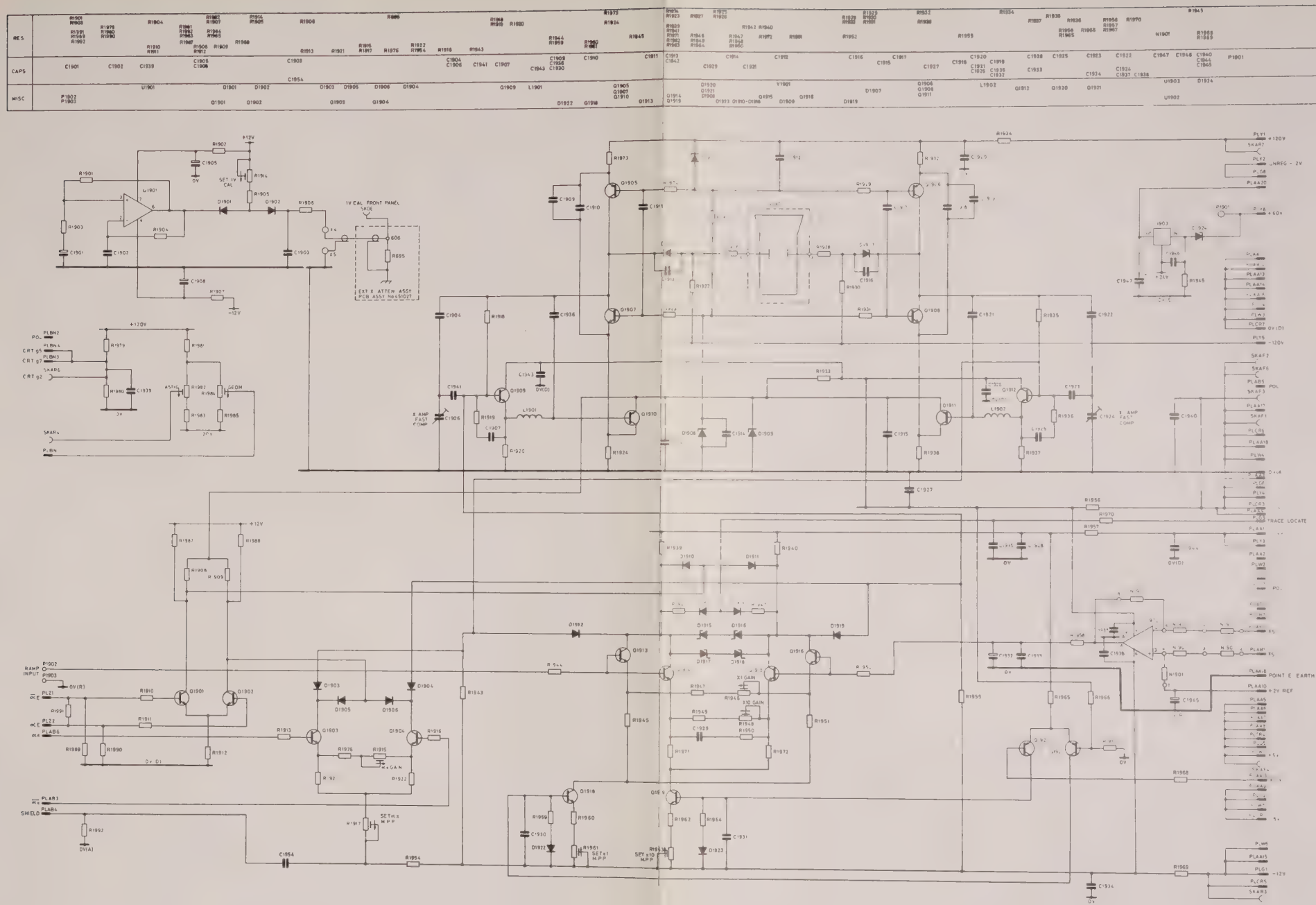


Fig. 6.4 X Output and Calibrator Circuit Diagram

5110 TRIGGER

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R601	300k	MF	2		38653
R602	300k	MF	2		38653
R604	68	CF			28716
R605	56	CF			28715
R606	33	CF			28712
R607	360	MF	2		38655
R608	43k	MF	2		38633
R609	10	CF			21793
R610	39	CF			28713
R611	3k3	CF			21803
R612	3k3	CF			21803
R613	51	MF	2		38563
R614	51	MF	2		38563
R620	47k	CP	WITH SWITCH		A4/450628
R621	10	CF			21793
R622	47	CF			28714
R623	390k	MF	2		38656
R624	220k	CF			21823
R625	22k	CP			A4/450627
R626	10	CF			21793
R651	300k	MF	2		38653
R652	300k	MF	2		38653
R654	33	CF			28712
R655	56	CF		1/8W	43147
R656	15	CF			28708
R657	360	MF	2		38655
R658	43k	MF	2		38633
R659	10	CF			21793
R660	39	CF			28713
R662	150	CF		1/8W	43714
R663	100	CF		1/8W	43150
R664	150	CF		1/8W	43714
R665	100	CF		1/8W	43150
R667	22	CF			28710
R669	22	CF			28710
R670	10	CF			21793
R671	10	CF			21793
R672	390	MF	2		38656
R674	47	CF			28714
R675	22k	CP			A4/450627
R691	470	CF			21797
R692	470	CF			21797
R693	1M	CF			31840
R694	47	CF			28714
R701	56	CF			28715
R702	560	CF			21798
R703	390	MF	2		38584
R704	560	CF			21798
R705	390	MF	2		38584
R706	820	CF			28724
R707	6k8	CF			21807
R708	10	CF			21793
R709	1k5	MF	2		38598
R710	120	CF			28718
R711	6k8	MF	2		38614
R712	10k	MF	2		38618
R713	1k5	MF	2		38598
R714	910	MF	2		38593
R715	1k	PCP			39261
R716	47	CF			28714
R717	82	CF			28717
R718	1k8	CF			28725
R719	3k3	CF			21803
R720	20k	PCP			39229
R721	5k6	CF			21806
R722	4k7	CF			21805
R723	100	CF			21794
R724	180	MF	2		38576
R725	3k3	CF			21803
R726	820	CF			28724
R727	33	CF			28712
R728	47	CF			28714
R729	150	CF			28719
R730	3k3	CF			21803
R731	47	CF			28714
R732	820	CF			28724
R733	150	CF			28719
R734	3k3	CF			21803
R735	62	MF	2		38565
R736	390	CF			28722
R737	33	CF			28712
R738	1k	MF	2		38594
R739	180	MF	2		38576
R740	560	CF			21798
R741	56	CF			28715
R742	56	CF			28715
R743	3k3	CF			21803
R744	680	CF			28723
R745	39	CF			28713
R746	270	CF			28720
R747	2k2	CF			21802
R748	10	CF			21793
R749	10	CF			21793
R750	39	CF			28713
R751	270	CF			28720
R752	10	CF			21793
R753	22	CF			28710
R754	22	CF			28710
R755	10	CF			21793
R756	270	CF			28720

5110 TRIGGER (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
R757	27	CF			28711
R759	270	CF			28720
R760	27	CF			28711
R761	1k	CF			21799
R762	240	MF	2		38579
R764	470	CF			21797
R765	2k2	CF			21802
R766	330	CF			28721
R767	330	CF			28721
R768	1k2	MF	2		38596
R769	390	MF	2		38584
R770	560	CF			21798
R771	300	MF	2		38581
R772	1k5	MF	2		38598
R773	47	CF			28714
R774	330	CF			28721
R775	22	CF			28710
R777	6k8	CF			21807
R778	6k8	CF			21807
R780	1k	CF			21799
R783	10	CF			21793
R784	3k9	CF			21804
R785	8k2	CF			21808
R786	270	CF			28720
R787	1k5	CF			21801
R788	56	CF			28715
R789	10k	CF			21809
R790	100k	CF			21819
R791	470	CF			21797
R792	560k	CF			32359
R793	270	CF			28720
R794	47k	CF			21815
R795	12k	CF			21810
R796	68k	CF			21816
R797	390	CF			28722
R798	300	MF	2		38581
R799	2k2	CF			21802
R801	56	CF			28715
R802	220	CF			21796
R803	390	MF	2		38584
R804	560	CF			21798
R805	390	MF	2		38584
R816	47	CF			28714
R820	20k	CP			39229
R821	5k6	CF			21806
R822	4k7	CF			21805
R823	100	CF			21794
R824	180	MF	2		38576
R825	3k3	CF			21803
R826	820	CF			28724
R831	47	CF			28714
R834	33	CF			28712
R835	62	MF	2		38565
R836	680	CF			28723
R838	1k	MF	2		38594
R839	180	MF	2		38576
R841	22	CF			28710
R842	22	CF			28710
R844	680	CF			28723
R845	39	CF			28713
R846	270	CF			28720
R849	10	CF			21793
R850	39	CF			28713
R851	270	CF			28720
R852	10	CF			21793
R853	22	CF			28710
R854	22	CF			28710
R855	10	CF			21793
R856	270	CF			28720
R857	27	CF			28711
R859	270	CF			28720
R860	27	CF			28711
R861	1k	CF			21799
R862	240	MF	2		38579
R864	470	CF			21797
R865	2k2	CF			21802
R866	330	CF			28721
R867	330	CF			28721
R868	1k2	MF	2		38596
R869	390	MF	2		38584
R870	560	CF			21798
R871	300	CF	2		38581
R872	1k5	MF	2		38598
R873	47	CF			28714
R874	330	CF			28721
R875	3k3	CF			21803
CAPACITORS					
C601	39pF	CE(2)			22371
C604	1.5/27pF	Trimmer			36273
C606	33pF	CE(2)			22370
C607	3/15pF	Trimmer			44053

5110 TRIGGER (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS (Cont.)					
C608	56pF	CE(2)			22373
C609	1.5/27pF	Trimmer			36273
C610	15pF	CE(3)			42410
C612	10nF	CE(2)		250V	22395
C620	10nF	CE(2)		250V	22395
C621	10nF	CE(2)		250V	22395
C622	100pF	CE(2)			22376
C623	100nF	CE(2)		250V	39199
C624	82pF	CE(2)			22375
C651	33pF	CE(2)			22370
C654	1.5/27pF	Trimmer			36273
C656	56pF	CE(2)			22373
C657	3/15pF	Trimmer			44053
C658	56pF	CE(2)			22373
C659	1.5/27pF	Trimmer			36273
C660	15pF	CE(3)			42410
C670	10nF	CE(2)		250V	22395
C671	10nF	CE(2)		250V	22395
C672	100nF	CE(2)		250V	39199
C673	100pF	CE(2)			22376
C690	4μF	T		35V	53249
C691	10nF	CE(3)			42444
C692	4μF	T		35V	53249
C701	10nF	CE(3)			42444
C702	10nF	CE(3)			42444
C703	10nF	CE(3)			42444
C704	10nF	CE(3)			42444
C705	10nF	CE(3)			42444
C706	10nF	CE(3)			42444
C707	10nF	CE(3)			42444
C708	10nF	CE(3)			42444
C709	120pF	CE(3)	A.O.T.		42444
C710	22μF	E		16V	450580
C711	10nF	CE(2)		250V	22395
C712	10nF	CE(3)			42444
C713	10nF	CE(2)		250V	22395
C714	22μF	E		16V	450580
C715	10nF	CE(2)			42444
C716	10nF	CE(2)			42444
C725	220pF	CE(3)		50V	42424
C728	5.6nF	CE(3)			42441
C732	5.6nF	CE(3)			42441
C735	10pF	CE(3)			42408
C736	22pF	CE(3)			42412
C738	10nF	CE(3)			42444
C739	10nF	CE(3)			42444
C740	10nF	CE(2)		250V	22395
C743	10nF	CE(3)			42444
C745	39pF	CE(3)			42415
C758	33pF	CE(3)			42414
C762	15pF	CE(3)			42410
C765	10nF	CE(2)		250V	22395
C768	10nF	CE(3)			42444
C769	10nF	CE(3)			42444
C772	10nF	CE(2)		250V	22395
C780	10nF	CE(3)			42444
C781	120pF	CE(3)			42421
C782	10nF	CE(3)			42444
C783	100nF	CE(2)		100V	37018
C784	100nF	CE(2)		100V	37018
C785	10nF	CE(3)			42444
C788	270pF	CE(3)			42425
C801	10nF	CE(3)			42444
C803	10nF	CE(3)			42444
C804	10nF	CE(3)			42444
C807	10nF	CE(3)			42444
C808	10nF	CE(3)			42444
C811	10nF	CE(3)			42444
C813	10nF	CE(3)		250V	22395
C815	47μF	E		10V	32167
C816	10nF	CE(3)			42444
C825	220pF	CE(3)			42424
C835	18pF	CE(3)			42411
C836	33pF	CE(3)			42414
C845	39pF	CE(3)			42415
C858	33pF	CE(3)			42414
C862	15pF	CE(2)			22366
C865	10nF	CE(2)		250V	22395
C868	10nF	CE(3)			42444

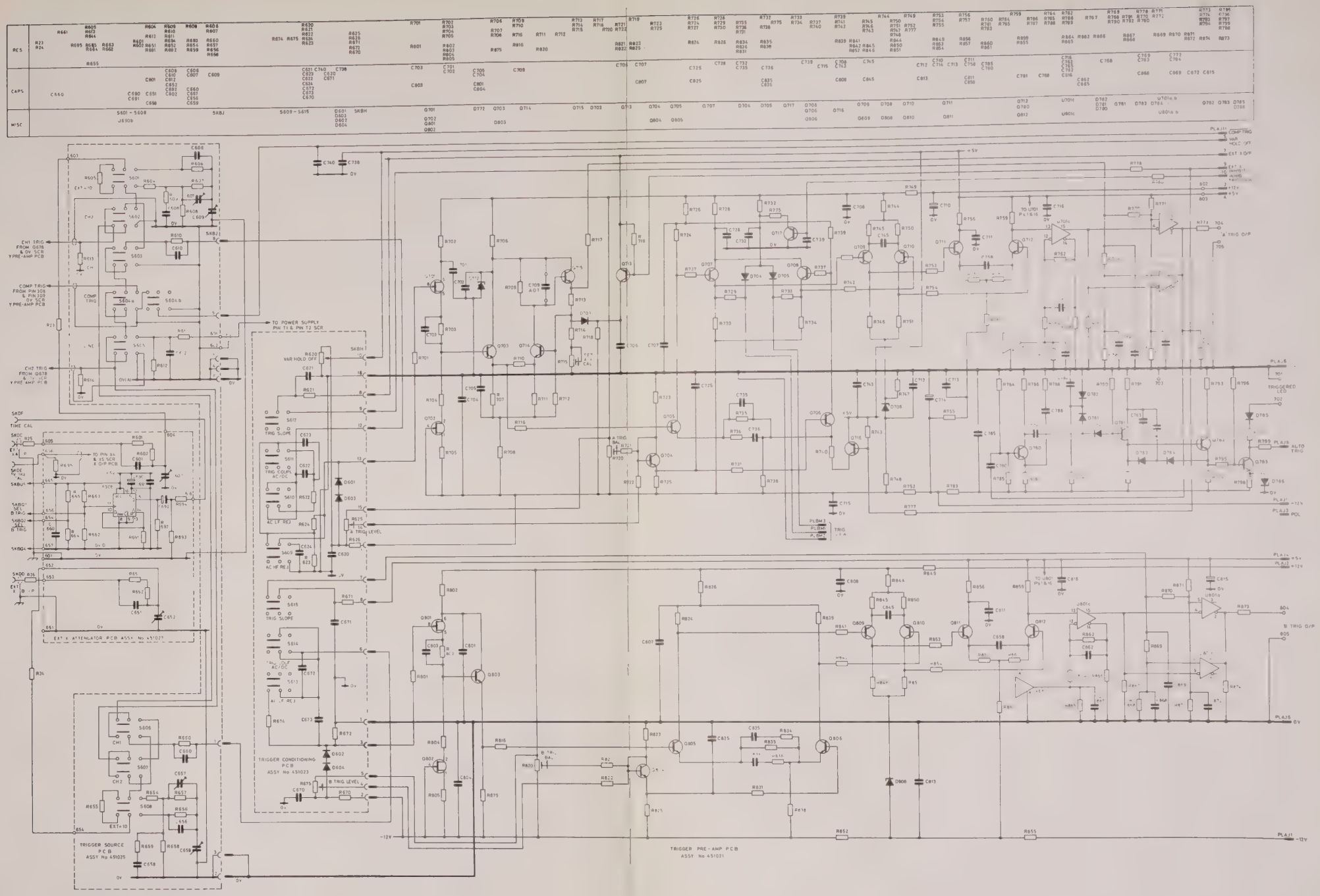


Fig. 6.5 Trigger Pre-amplifier Circuit Diagram

5110 DISPLAY MANAGEMENT

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1401	47k	CF			21815
R2402	1k5	CF			21801
R2403	47k	CF			21815
R2404	47k	CF			21815
R2405	3k3	CF			21803
R2406	2k2	CF			21802
R2407	47k	CF			21815
R2408	3k3	CF			21803
R2409	1k	CF			21799
R2410	2k2	CF			21802
R2411	10k	CF			21809
R2412	10k	CF			21809
R2413	2k2	CF			21802
R2414	680	CF			28723
R2415	1k8	CF			28725
R2416	4k7	CF			21805
R1417	2k2	CF			21802
R2418	2k2	CF			21802
R1419	2k2	CF			21802
R2420	4k7	CF			21805
R2421	2k2	CF			21802
R2422	47k	CF			21815
R2423	2k2	CF			21802
R2424	8k2	CF			21808
R2425	1k	CF			21799
R2426	1k2	CF			21800
R2427	120	CF			28718
R2428	10k	CF			21809
R2429	10k	CF			21809
R2430	1k2	CF			21800
R2431	2k2	CF			21802
R2432	8k2	CF			21808
R2433	330	CF			28721
R2434	330	CF			28721
R2435	2k2	CF			21802
R2436	2k2	CF			21802
R2437	2k2	CF			21802
R2438	2k2	CF			21802
R2439	2k2	CF			21802
R2440	560	CF			21798
R2441	330	CF			28721
R2442	2k2	CF			21802
R2443	2k2	CF			21802
R2444	560	CF			21798
R2445	330	CF			28721
R2446	2k2	CF			21802
R2447	2k2	CF			21802
R2448	2k2	CF			21802
R2449	8k2	CF			21808
R2450	330	CF			28721
R2451	1k2	CF			21800
R2452	220k	CF			21823
R2453	220k	CF			21823
R2454	330	CF			28721
R2455	330	CF			28721
R2456	4k7	CF			21805
R2457	4k7	CF			21805
R2458	4k7	CF			21805
R2459	4k7	CF			21805
R2460	47k	CF			21815
R2461	47k	CF			21815
R2462	2k2	CF			21802
R2463	10k	CF			21809
R2464	8k2	CF			21808
R2465	8k2	CF			21808
R2466	1k	CF			21799
R2467	1k	CF			21799
R2468	1k	CF			21799
R2569	47k	CF			21815
R2470	330	CF			28721
R2471	330	CF			28721
R2472	10k	CF			21809
R2473	390	CF			28722
R2474	1k	CF			21799
R2475	4k7	CF			21805
R2476	390	CF			28722
R2477	390	CF			28722
R2478	2k2	CF			21802
R2479	10k	CF			21809
R2480	330	CF			28721
R2481	10k	CF			21809
R2482	4k7	CF			21805
R2483	120	CF			28718
R2484	470	CF		1/8W	44222
R2485	470	CF		1/8W	44222
R2486	470	CF		1/8W	44222
R2487	470	CF		1/8W	44222
R2488	470	CF		1/8W	44222
R2489	470	CF		1/8W	44222
R2490	470	CF		1/8W	44222
R2491	470	CF		1/8W	44222
R2492	1k	CF		1/8W	44226
N2401	47kx8	Resistor Network			450602
N2402	4k7x8	Resistor Network			39225
CAPACITORS					
C2401	22µF	E		25V	32181
C2402	39pF	CE(3)			42415
C2403	5.6pF	CE(3)			42405
C2404	120pF	CE(3)			42421
C2405	3/45pF	Trimmer			36274
C2406	100nF	CE(3)			43498
C2407	270pF	CE(3)			42425
C2408	10nF	CE(3)		25V	450548
C2410	47µF	E		10V	32167
C2411	10nF	CE(3)		25V	450548
C2412	10nF	CE(3)		25V	450548
C2413	10nF	CE(3)		25V	450548
C2414	10nF	CE(3)		25V	450548
C2415	10nF	CE(3)		25V	450548

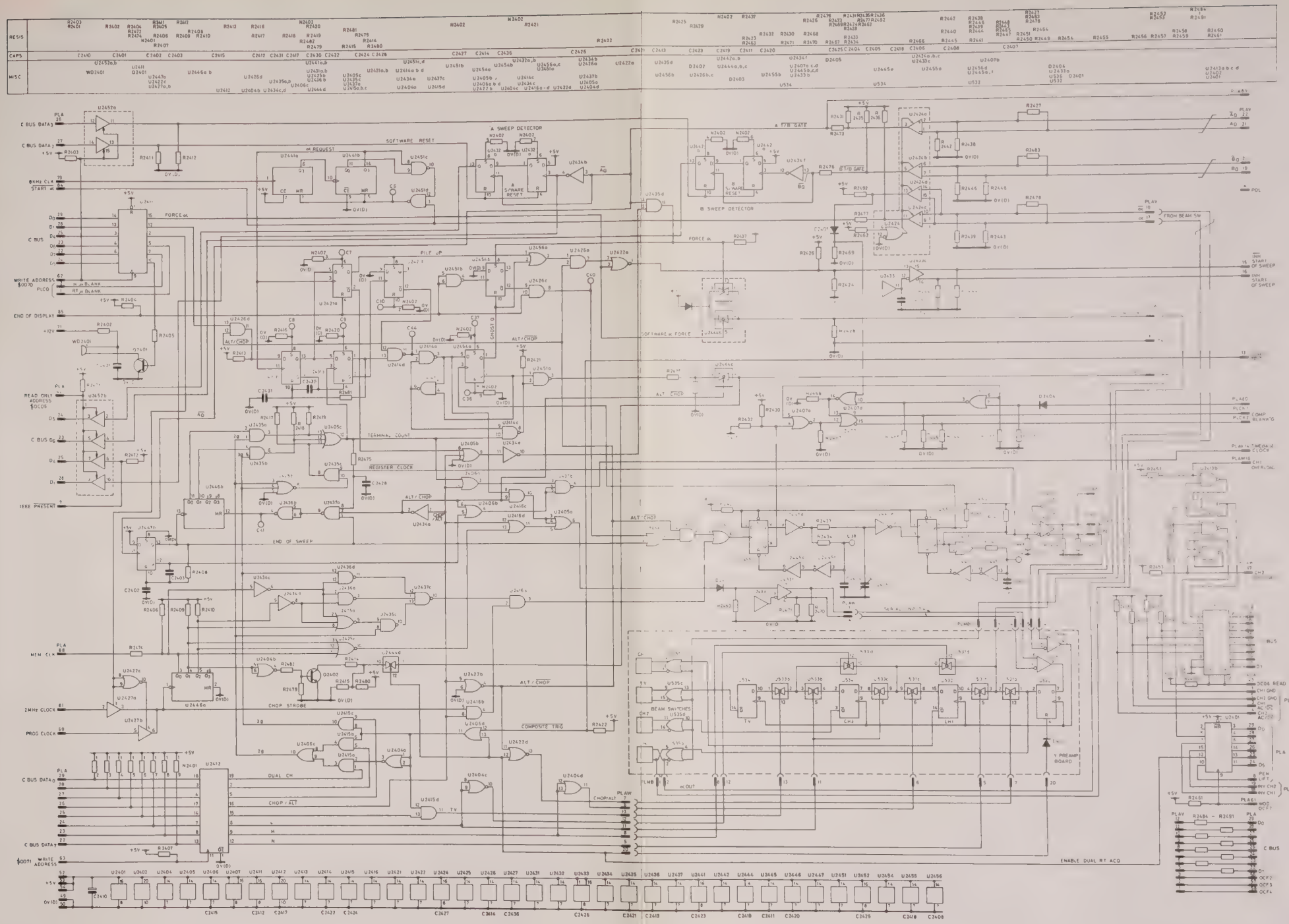


Fig. 6.6 Display Management Circuit Diagram

5110 VOLTAGE GENERATOR

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R2501	1k	MF	2		38594
R2502	33k	MF			451581
R2503	20k	PCP			39229
R2504	20k	PCP			39229
R2505	200k	CP			450907
R2506	20k	PCP			39229
R2507	20k	PCP			39229
R2508	47	CF			28714
R2509	47	CF			28714
R2510	3k48	MF			451580
R2511	3k3	MF	2		38606
R2512	3k3	MF	2		38606
R2513	3k3	MF	2		38606
R2514	82k	MF			450321
R2515	1k8	MF			450437
R2516	10k	MF	0.25		450905
R2517	10k	MF	0.25		450905
R2518	20k	PCP			39229
R2519	1k3	MF	0.5		450904
R2520	91k	MF	2		38641
R2521	91k	MF	2		38641
R2522	91k	MF	2		38641
R2523	91k	MF	2		38641
R2524	91k	MF	2		38641
R2525	91k	MF	2		38641
R2526	91k	MF	2		38641
R2527	91k	MF	2		38641
R2528	1k	CF			21799
R2530	47	CF			28714
R2531	47	CF			28714
R2532	47	CF			28714
R2533	47	CF			28714
R2534	47	CF			28714
R2535	47	CF			28714
R2536	47	CF			28714
R2537	47	CF			28714
R2540	10	CF			21793
R2541	10	CF			21793
R2542	10	CF			21793
R2543	10	CF			21793
R2544	10	CF			21793
R2545	10	CF			21793
R2546	10	CF			21793
R2547	10	CF			21793
R2551	1k	MF	2		38594
R2552	10k	MF	2		38618
R2553	10k	MF	2		38618
R2554	10k	MF	2		38618
R2555	10k	MF	2		38618
R2556	10k	MF	2		38618
R2557	10k	MF	2		38618
R2558	1k	MF	2		38594
R2559	100k	MF	2		38642

Ref	Value	Description	Tol %±	Rating	Part No
R2560	100k	MF	2		38642
R2561	10k	MF	2		38618
R2562	10k	MF	2		38618
R2563	100k	MF	2		38642
R2564	200k	MF	2		38649
R2565	1k	MF	2		38594
R2566	30k	MF	2		38629
R2567	1k2	CF			21800
R2568	200k	MF	2		38649
R2569	10k	CF			21809
R2570	1k	CF			21799
R2571	470k	CF			32330
R2572	47k	CF			21815
R2573	1k	CF			21799
R2574		Fitted with option only			
R2576	10k	MF	2		38618
R2577	10k	MF	2		38618
R2578	100	CF			21794
R2579	10k	CF			21809
R2581	100	CP			39263
R2582	100	CP			39263
R2583	100k	CP			42158
R2584	100k	CP			42158
R2585	12k	MF	0.5		451609
R2586	18k	MF	0.5		451610
R2587	12k	MF	0.5		451609
R2588	18k	MF	0.5		451610
R2589	4k7	CF			21805
R2590	4k7	CF			21805
N2501	8k2x8	Resistor Network			450705
N2502		Resistor Network			A3/450621
N2503		Resistor Network			A3/450621
CAPACITORS					
C2502	100nF	CE(3)			43498
C2503	10nF	CE(3)		25V	450548
C2504	10nF	CE(3)		25V	450548
C2505	10nF	CE(3)		25V	450548
C2506	10nF	CE(3)		25V	450548
C2507	100nF	CE(3)			43498
C2508	10nF	CE(3)		25V	450548
C2509	10nF	CE(3)		25V	450548
C2510	10nF	CE(3)		25V	450548
C2511	10nF	CE(3)		25V	450548
C2512	10nF	CE(3)		25V	450548
C2513	10nF	CE(3)		25V	450548
C2514	10nF	CE(3)		25V	450548
C2515	10nF	CE(3)		25V	450548
C2516	10nF	CE(3)		25V	450548
C2517	10μF	E		25V	32180
C2518	10nF	CE(3)		25V	450548
C2519	22μF	E		25V	32181

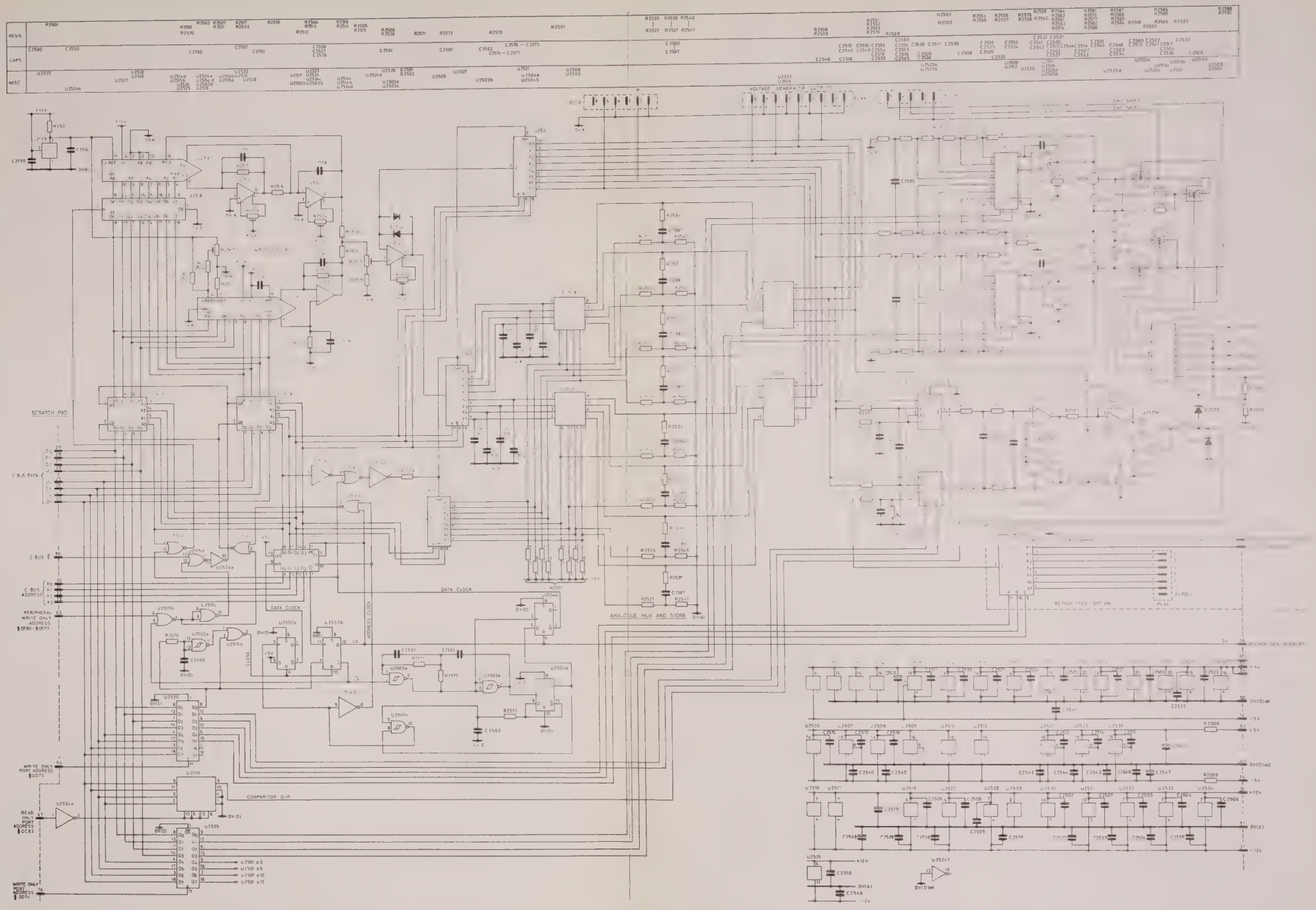


Fig. 6.7 Voltage Generator Circuit Diagram

5110 CURSOR (TIMEBASE)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1601	1k6	MF	2		38599
R1602	620	MF	2		38589
R1603	470	MF	2		38586
R1604	2k7	MF	2		38604
R1605	2k4	MF	2		38603
R1606	560	CF		1/8W	44223
R1607	1k	CF		1/8W	44226
R1608	560	CF		1/8W	44223
R1609	1k2	CF		1/8W	44227
R1610	2k2	CF		1/8W	43357
R1611	150	MF	2		28719
R1612	150	MF	2		28719
R1613	50	CP			42155
R1614	120	CF		1/8W	43713
R1615	180	CF		1/8W	43715
R1616	150	MF	2		28719
R1617	150	MF	2		28719
R1618	560	CF		1/8W	44223
R1619	2k2	CF		1/8W	43357
R1620	1k2	CF		1/8W	44227
R1621	2k2	CF		1/8W	43357
R1622	120	CF		1/8W	43713
R1623	180	CF		1/8W	43715
R1624	120	CF		1/8W	43713
R1625	180	CF		1/8W	43715
R1626	120	CF		1/8W	43713
R1627	270	CF		1/8W	43716
R1629	180	CF		1/8W	43715
R1631	10	CF			21793
R1632	10	CF			21793
R1633	10	CF			21793
R1634	10k	CF			21809
R1635	10k	CF			21809
R1636	3k3	CF			21803
R1637	100	MF	2		21794
R1639	270	CF		1/8W	43716
R1641	10	CF			21793
R1642	10	CF			21793
R1643	10	CF			21793
R1644	10k	CF			21809
R1645	10k	CF			21809
R1646	3k3	CF			21803
R1647	100	MF	2		21794
R1651	10	CF			21793
R1652	10	CF			21793
R1653	10	CF			21793
R1654	10k	CF			21809
R1655	10k	CF			21809
R1657	100	MF	2		21794
R1658	330	CF		1/8W	44220
R1661	10	CF			21793
R1662	10	CF			21793
R1663	10	CF			21793
R1664	10k	CF			21809
R1665	10k	CF			21809
R1667	100	MF	2		21794
R1668	100	CF		1/8W	43150
R1669	100	CF		1/8W	43150
R1671	470	MF	2		21797
R1672	120	CF		1/8W	43713
R1673	330	CF		1/8W	44220
R1681	10	CF		1/8W	43138
R1682	10	CF		1/8W	43138
R1683	10	CF		1/8W	43138
R1684	10	CF		1/8W	43138
N1301	2k2x8	Resistor Network			43185
N1601	560x8	Resistor Network			451135
N1602	560x8	Resistor Network			451135
N1603	2k2x8	Resistor Network			43185
N1604	1k	Resistor Network			451207
N1605	120	Resistor Network			450884
N1606	180	Resistor Network			450885
N1608	560x8	Resistor Network			39258
N1615		Resistor Network			A3/450622
N1616		Resistor Network			A3/450622
N1617		Resistor Network			A3/450622
N1618		Resistor Network			A3/450622
N1630		Resistor Network			A3/450622
N1631		Resistor Network			A3/450622
CAPACITORS					
C1601	10nF	CE(3)			42444
C1602	10nF	CE(3)			42444
C1603	10nF	CE(3)			42444
C1604	10nF	CE(3)			42444
C1605	10nF	CE(3)			42444
C1606	10nF	CE(3)			42444
C1607	10nF	CE(3)			42444
C1608	10nF	CE(3)			42444
C1609	10nF	CE(3)			42444
C1610	10nF	CE(3)			42444
C1611	100pF	CE(2)			22376
C1612	10nF	CE(3)			42444
C1613	100pF	CE(2)			22376
C1614	33pF	CE(2)			22370
C1615	10nF	CE(3)			42444
C1616	10nF	CE(3)			42444
C1617	10nF	CE(2)			22395

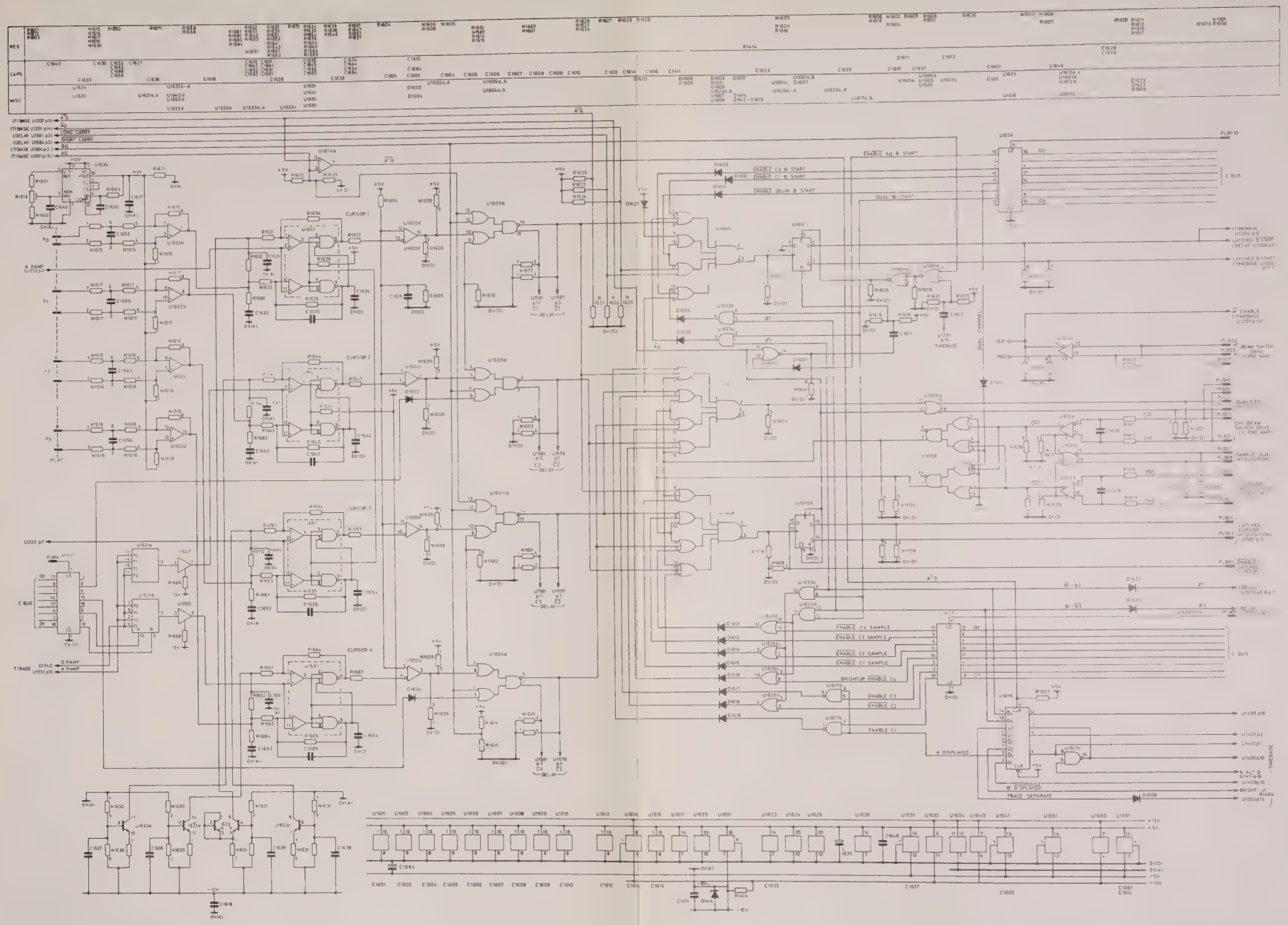


Fig. 6.8 Timebase (cursor management), Circuit Diagram

5110 TIMEBASE (DELAY)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1514	180	CF			43715
R1515	120	CF		1/8W	43713
R1516	330	CF			28721
R1519	560	CF			44223
R1522	330	CF			44220
R1523	330	CF			44220
R1528	180	CF			43715
R1529	1k	CF			21799
R1530	180	CF			43715
R1531	4k7	CF			21805
R1532	10	CF			21793
R1534	560	CF			44223
R1535	560	CF			44223
R1536	560	CF			44223
R1537	180	CF		1/8W	43715
R1538	120	CF		1/8W	43713
R1539	560	CF			21798
R1540	10k	CF			21809
R1541	2k2	CF			21802
R1542	100	CF			21794
R1543	1k	CF			21799
R1544	8k2	CF			21808
R1545	8k2	CF			21808
R1546	2k2	CF			21802
R1547	56	CF		1/8W	43147
R1548	68	CF		1/8W	28716
R1549	68	CF		1/8W	43148
R1550	560	CF			21798
R1551	560	CF			21798
R1552	2k2	CF			21802
R1571	4k7	CF			21805
R1572	1k	CF			21799
R1573	2k2	CF			21802
R1580	220	CF			21796
R1581	330	CF			28721
R1582	330	CF			28721
R1583	1k1	CF			38595
R1584	330	CF			28721
R1585	270	CF			28720
R1586	100	CF			21794
R1587	100	CF		1/8W	43150
R1588	1k	CF			21799
R1590	10k	CF			21809
R1591	10	CF			21793
R1593	560	CF			21798
R1594	560	CF			21798
N1570	560x8	Resistor Network			39258
N1571	560x8	Resistor Network			39258
N1572	2k2x8	Resistor Network			43185
N1573	560x8	Resistor Network			39258
N1581	560x8	Resistor Network			39258
N1582	2k2x8	Resistor Network			43185
N1584	2k2x8	Resistor Network			43185
N1585	2k2x8	Resistor Network			43185
N1586	560x4	Resistor Network			451135
N1587	560x4	Resistor Network			451135
CAPACITORS					
C1537	1nF	CE(3)		50V	42432
C1540	1n5	CE(3)			42434
C1541	2p2	CE(3)			42400
C1542	18pF	CE(3)			42411
C1543	2p2	CE(3)			42405
C1544	1n5	CE(3)			42434
C1546	1nF	CE(3)			42432
C1566	10nF	CE(3)			42444
C1567	10nF	CE(3)			42444
C1568	10nF	CE(3)			42444
C1569	10nF	CE(3)			42444
C1570	180pF	CE(3)			42423
C1571	56pF	CE(3)			42417
C1572	33pF	CE(3)			42414
C1573	22pF	CE(3)			41412
C1574	68pF	CE(3)			41418
C1577	100pF	CE(3)			42420
C1580	10nF	CE(3)			42444
C1581	10nF	CE(3)			42444
C1582	10nF	CE(3)			42444
C1583	10nF	CE(3)			42444
C1584	10nF	CE(3)			42444
C1585	10nF	CE(3)			42444
C1586	10nF	CE(3)			42444
C1587	10nF	CE(3)			42444
C1588	10nF	CE(3)			42444
C1589	10nF	CE(3)			42444
C1590	10nF	CE(3)			42444
C1591	10nF	CE(3)			42444
C1592	10nF	CE(3)			42444
C1593	10nF	CE(3)			42444
C1594	10nF	CE(3)			42444
C1595	10nF	CE(3)			42444
C1596	10nF	CE(3)			42444
C1598	10nF	CE(3)			42444
C1599	10nF	CE(3)			42444

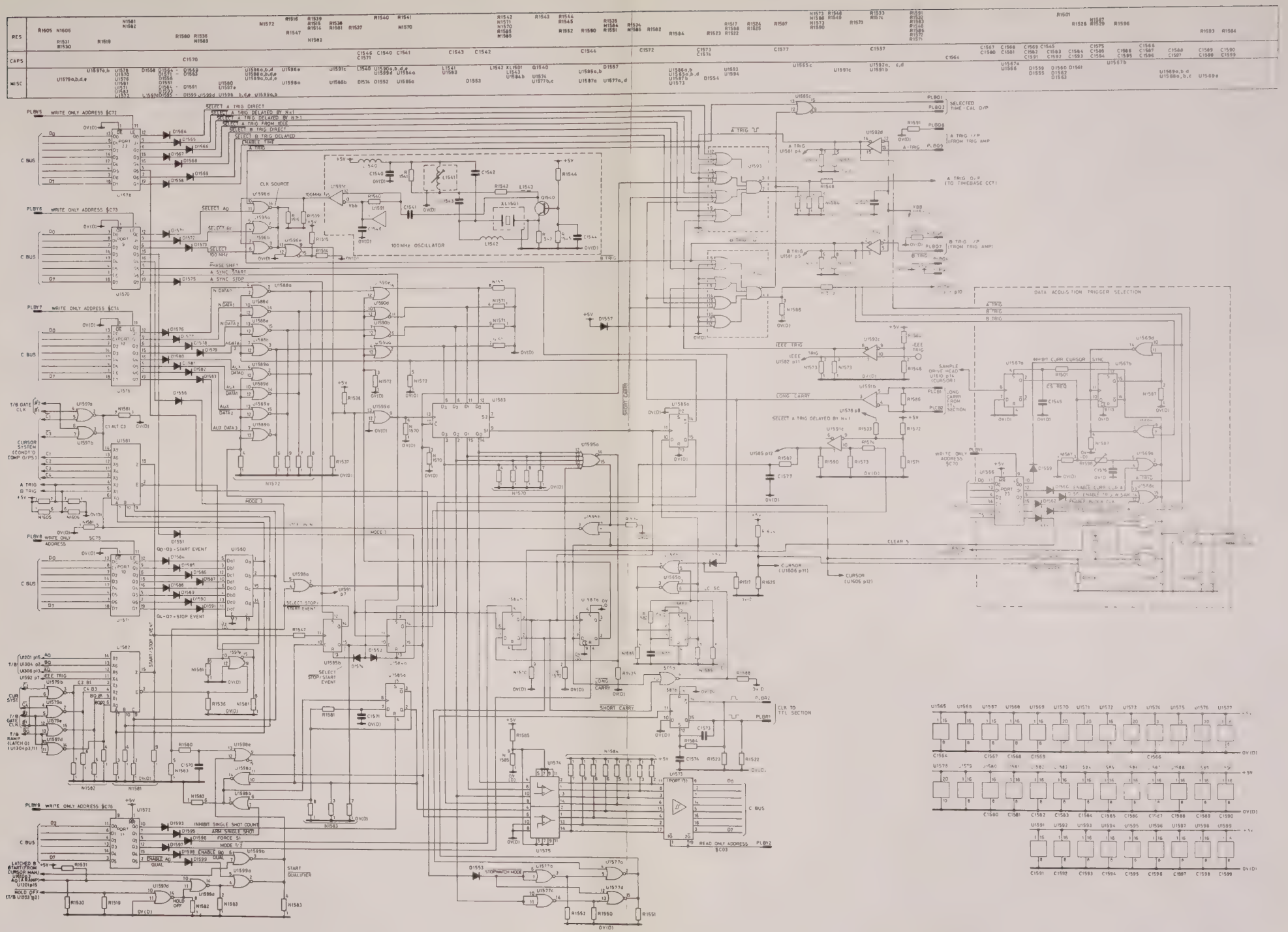


Fig. 6.9 Delay System Circuit Diagram

5110 ACQUISITION & STORE

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R2601	56	MF	2		38564
R2604	10k	CF			21809
R2605	150	CF			28719
R2606	62	MF	2		38565
R2607	62	MF	2		38565
R2608	390	CF			28722
R2609	56	CF			28715
R2610	560	CF			21798
R2611	560	CF			21798
R2612	2k2	CF			21802
R2613	2k2	CF			21802
R2614	2k2	CF			21802
R2615	120	CF			28718
R2616	2k2	CF			21802
R2617	2k2	CF			21802
R2618	10k	CF			21809
R2619	10k	CF			21809
R2620	10k	CF			21809
R2621	10k	CF			21809
R2622	10k	CF			21809
R2623	10	CF			21793
R2624	2k2	CF			21802
R2625	2k2	CF			21802
R2626	1M	CF			21840
R2627	2k2	CF			21802
R2628	330	CF			28721
R2629	330	CF			28721
R2630	330	CF			28721
R2631	330	CF			28721
R2632	270	CF			28720
R2633	470	CF			21797
R2634	150	CF			28719
R2635	1k	PCP			39261
R2636	2k2	CF			21802
R2637	2k2	CF			21802
R2638	680	MF	2		38590
R2639	10	CF		1/8W	43138
R2640	10k	CF			21809
R2641	1M	CF			21840
R2642	120	CF			28718
R2643	120	CF			28718
R2644	120	CF			28718
R2645	120	CF			28718
R2646	120	CF			28718
R2647	10k	CF			21809
R2648	12k	CF			21810
R2649	2k2	CF			21802
R2650	820	MF	2		38592
R2651	820	MF	2		38592
R2652	10	CF			21793
R2653	10	CF			21793
R2654	10	CF			21793
R2655	22k	CF			21812
R2656	22k	CF			21812
R2657	1k	CF			21799
R2658	2k2	CF			21802
R2659	200	MF	2		38577
R2660	100	PCP			39263
R2661	2k2	MF	2		38602
R2662	10	CF			21793
R2663	620	MF	2		38589
R2664	1k	CF			21799
R2665	820	MF	2		38592
R2666	10	CF			21793
R2669	500	PCP			39262
R2670	2k2	CF			21802
R2671	2k2	CF			21802
R2672	2k2	CF			21802
R2674	330	CF			28721
R2675	220	CF			21796
R2676	5k6	MF	2		38612
R2677	5k1	MF	2		38611
R2678	220	CF			21796
R2679	10	CF			21793
R2685	470	CF			21797
R2686	470	CF			21797
R2687	2k2	CF			21802
R2689	10	CF			21793
R2690	10k	CF			21809
R2691	10k	CF			21809
R2692	10k	CF			21809
R2693	2k2	CF			21802
R2694	2k2	CF			21802
R2695	2k2	CF			21802
R2696	2k2	CF			21802
R2697	10k	CF			21809
R2698	3k3	CF			21803
R2699	2k2	CF			21802
N2601	4k7x8	Resistor Network			39225
N2602	1Mx8	Resistor Network			450727
N2603	1Mx10	Resistor Network			450930
N2604	220x4 330x4	Resistor Network			451059
N2605	220x4 330x4	Resistor Network			451059
CAPACITORS					
C2601	47µF	E		10V	32167
C2602	100pF	CE(3)			42420
C2603	10nF	CE(3)		25V	450548
C2604	10nF	CE(3)		25V	450548
C2605	2.2µF	T		35V	35930
C2606	10nF	CE(3)		25V	450548
C2607	10nF	CE(3)		25V	450548
C2608	10nF	CE(3)		25V	450548
C2609	10nF	CE(3)		25V	450548
C2610	10nF	CE(3)		25V	450548

5110 ACQUISITION & STORE (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS (Cont.)					
C2611	2.2μF	T		35V	35930
C2612	10nF	CE(3)		25V	450548
C2613	10pF	CE(2)		50V	36606
C2614	10pF	CE(2)		50V	36606
C2615	10pF	CE(2)		50V	36606
C2616	10nF	CE(3)		25V	450548
C2617	10nF	CE(3)		25V	450548
C2618	10nF	CE(3)		25V	450548
C2619	10pF	CE(2)		50V	36606
C2620	10nF	CE(3)		25V	450548
C2621	10nF	CE(3)		25V	450548
C2622	10nF	CE(3)		25V	450548
C2623	10nF	CE(3)		25V	450548
C2624	10nF	CE(3)		25V	450548
C2625	10nF	CE(3)		25V	450548
C2626	10nF	CE(3)		25V	450548
C2627	10nF	CE(3)		25V	450548
C2628	10pF	CE(2)		50V	36606
C2629	10pF	CE(2)		50V	36606
C2630	10nF	CE(3)		25V	450548
C2631	10nF	CE(3)		25V	450548
C2632	10nF	CE(3)		25V	450548
C2633	10pF	CE(2)		50V	36606
C2634	10pF	CE(2)		50V	36606
C2635	120pF	CE(3)			42421
C2636	10nF	CE(3)		25V	450548
C2637	10nF	CE(3)		25V	450548
C2638	10nF	CE(3)		25V	450548
C2639	10nF	CE(3)		25V	450548
C2640	10nF	CE(3)		25V	450548
C2641	10nF	CE(3)		25V	450548
C2642	10nF	CE(3)		25V	450548
C2642	10pF	CE(3)			42408
C2643	100pF	CE(3)			42420
C2644	100pF	CE(3)			42420
C2645	2.2μF	T		35V	35930
C2647	10nF	CE(3)		25V	450548
C2648	10nF	CE(3)		25V	450548
C2649	10nF	CE(3)		25V	450548
C2650	10nF	CE(3)		25V	450548
C2651	120pF	CE(3)			42421
C2660	100nF	CE(3)			43498
C2661	10nF	CE(3)		25V	450548
C2662	10nF	CE(3)		25V	450548
C2663	10nF	CE(3)		25V	450548
C2664	10nF	CE(3)		25V	450548
C2665	10nF	CE(3)		25V	450548
C2666	10nF	CE(3)		25V	450548
C2667	10nF	CE(3)		25V	450548
C2668	10nF	CE(3)		25V	450548
C2669	10nF	CE(3)		25V	450548
C2670	10nF	CE(3)		25V	450548
C2671	10nF	CE(3)		25V	450548
C2672	10nF	CE(3)		25V	450548

Ref	Value	Description	Tol %±	Rating	Part No
C2675	22pF	CE(3)			42412
C2676	22pF	CE(3)			42412
C2678	1.5nF	CE(3)			42434
C2680	47μF	E		10V	32167
C2681	56pF	CE(3)			42417
C2685	8.2pF	CE(3)			42407
C2686	83pF	CE(3)			42419
C2690	10nF	CE(3)		100V	451378
C2691	10nF	CE(3)		100V	451378
C2692	10nF	CE(3)		100V	451378
C2693	2.2μF	T		35V	35930
Q2606		MPS3640			24128
Q2607		MPS3640			24128
Q2608		2N3906			21533
Q2610		MPS2369			36625
DIODES					
D2601		IN4148			23802
D2602		IN4148			23802
D2603		IN4148			23802
D2604		IN4148			23802
D2605		IN4148			23802
D2606		IN4148			23802
U2601		74LS11			41076
U2602		4075			36204
U2603		74C244			450913
U2604		74C244			450913
U2605		74C244			450913
U2606		74C374			451266
U2607		74C374			451266
U2608		74C374			451266
U2609		4013			34954
U2612		74LS126			44391
U2616		74LS374			43386
U2617		26LS32			450915
U2618		26LS32			450915
U2620		2114–1			450459
U2621		2114–1			450459
U2622		2114–1			450459
U2623		2114–1			450459
U2624		2114–1			450459
U2625		4516			37058
U2626		4516			37058
U2627		4516			37058
U2628		4023			37812
U2629		4011			34593

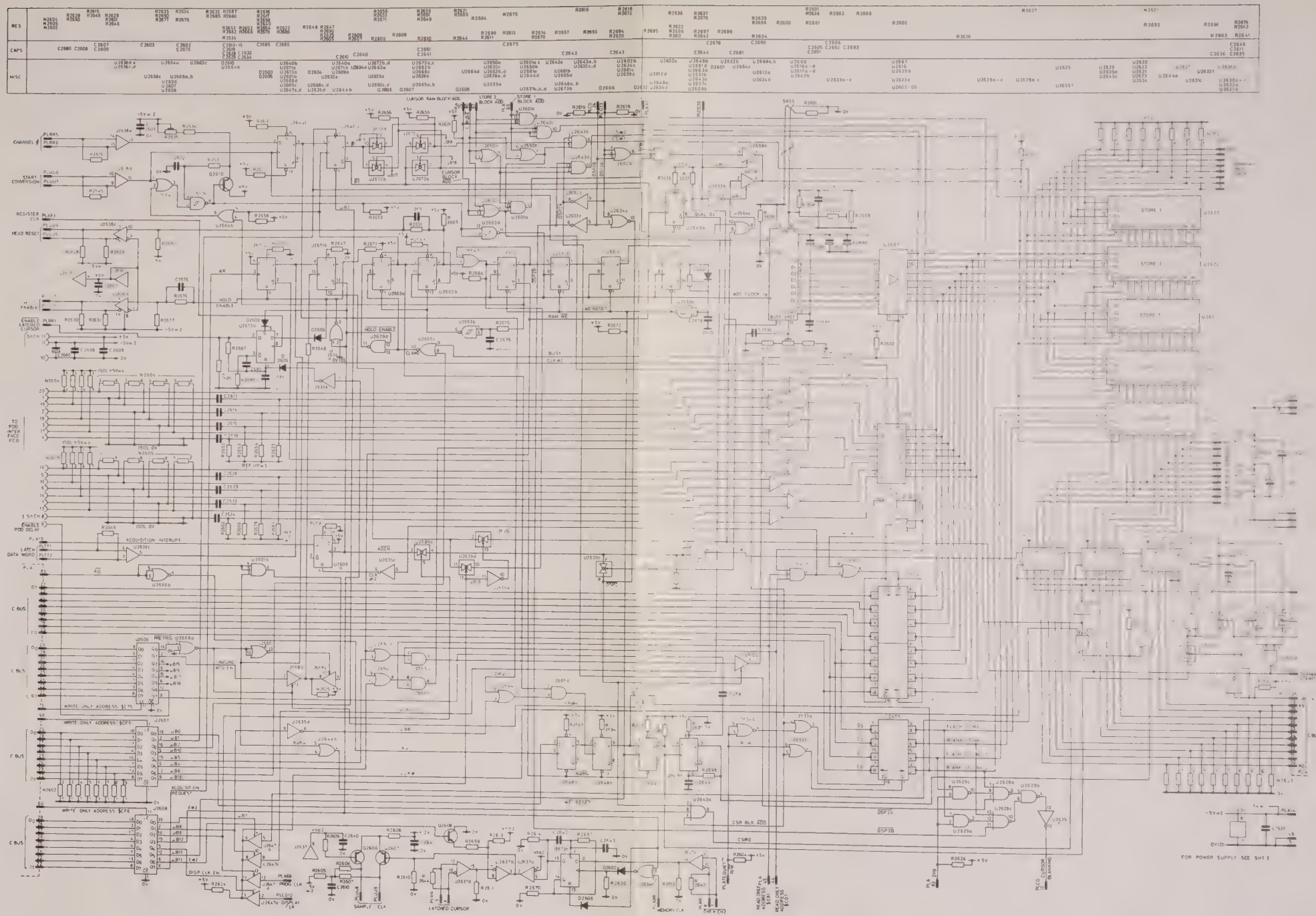


Fig. 6.10 Data Acquisition and Store Circuit Diagram

5110 DATA DISPLAY

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R2701	820	CF			28724
R2702	1M	CF			31840
R2703	4k7	CF			21805
R2704	4k7	CF			21805
R2705	4k7	CF			21805
R2706	4k7	CF			21805
R2707	10k	CF			21809
R2708	2k2	CF			21802
R2709	27k	CF			21813
R2710	18k	CF		A.O.T.	21811
R2712	1M	CF			31840
R2713				A.O.T.	451132
R2714	1M	CF			31840
R2715	1M	CF			31840
R2716	6k8	MF	2		38614
R2717	6k8	MF	2		38614
R2718	36	MF			450924
R2719	36	MF			450924
R2720	20k	PCP			39229
R2721	3k9	MF	2		38608
R2722	18k	MF	2		38624
R2723	3k3	MF	2		38606
R2724	1M	CF			31840
R2725	100	PCP			39263
R2726	200	MF	2		38577
R2727	200	MF	2		38577
R2728	3k6	MF	2		38607
R2729	3k6	MF	2		38607
R2730	1M	CF			31840
R2731	1M	CF			31840
R2732	2k4	MF	2		38603
R2733	6k8	MF	2		38614
R2734	470	MF	2		38586
R2735	1k	PCP			39261
R2736	6k8	MF	2		38614
R2737	6k8	MF	2		38614
R2738	36	MF			450924
R2739	36	MF			450924
R3740	560	CF			21798
R2741	10k	CF			21809
R2742	1M	CF			31840
R2743	10	CF			21793
R2744	10k	CF	was R7106		21809
R2745	470	MF	2		38586
R2746	1M	CF			31840
R2747	5k6	CF			21806
R2748	470	CF			21797
R2754	470	CF			21797
R2755	1M	CF			31840
R2756	470	CF			21797
R2757	470	CF			21797
R2759	1M	CF			31840
R2760	820	MF	2		38592

Ref	Value	Description	Tol %±	Rating	Part No
R2761	68k	MF	2		38638
R2762	10k	PCP			39228
R2763	5k	CP			42156
R2764	10k	PCP			39228
R2765	36k	MF	2		38631
R2766	2k4	MF	2		38603
R2767	68k	MF	2		38638
R2768	4k7	CF			21805
R2769	12k	MF	2		38620
R2770	1k5	MF	2		38698
R2771	2k2	PCP			36030
R2772	4k7	CF			21805
R2773	2k4	MF	2		38603
R2778	1k8	CF		A.O.T.	28725
R2780	1M	CF			31840
R2781	1M	CF			31840
R2782	1M	CF			31840
R2783	1M	CF			31840
R2784	1M	CF			31840
R2785	1M	CF			31840
R2786	100	CF			21794
R2787	100	CF			21794
R2788	1M	CF			31840
R2789	3k9	MF	2		38608
R2792	6k8	MF	2		38614
N2701	4k7x8	Resistor Network			39225
N2702	1Mx8	Resistor Network			450727
N2703	1Mx8	Resistor Network			450727
N2704	1Mx8	Resistor Network			450727
N2705	1Mx8	Resistor Network			450727
CAPACITORS					
C2701	22µF	E		25V	32181
C2702	10nF	CE(3)		25V	450548
C2706	10nF	CE(3)		25V	450548
C2707	10pF	CE(3)			42408
C2708	47pF	CE(3)			42416
C2709	10nF	CE(3)		25V	450548
C2710	15pF	CE(3)			42410
C2711	3.9nF	CE(3)			42439
C2712	100nF	CE(3)			43498
C2713	100nF	CE(3)			43498
C2714	100nF	CE(3)			43498
C2715	47pF	CE(3)			42416
C2716	470nF	CE(3)			43500
C2717	1nF	CE(3)			42432
C2718	10nF	CE(3)		25V	450548
C2719	10nF	CE(3)		25V	450548
C2720	10nF	CE(3)		25V	450548
C2721	10nF	CE(3)		25V	450548
C2722	10nF	CE(3)		25V	450548

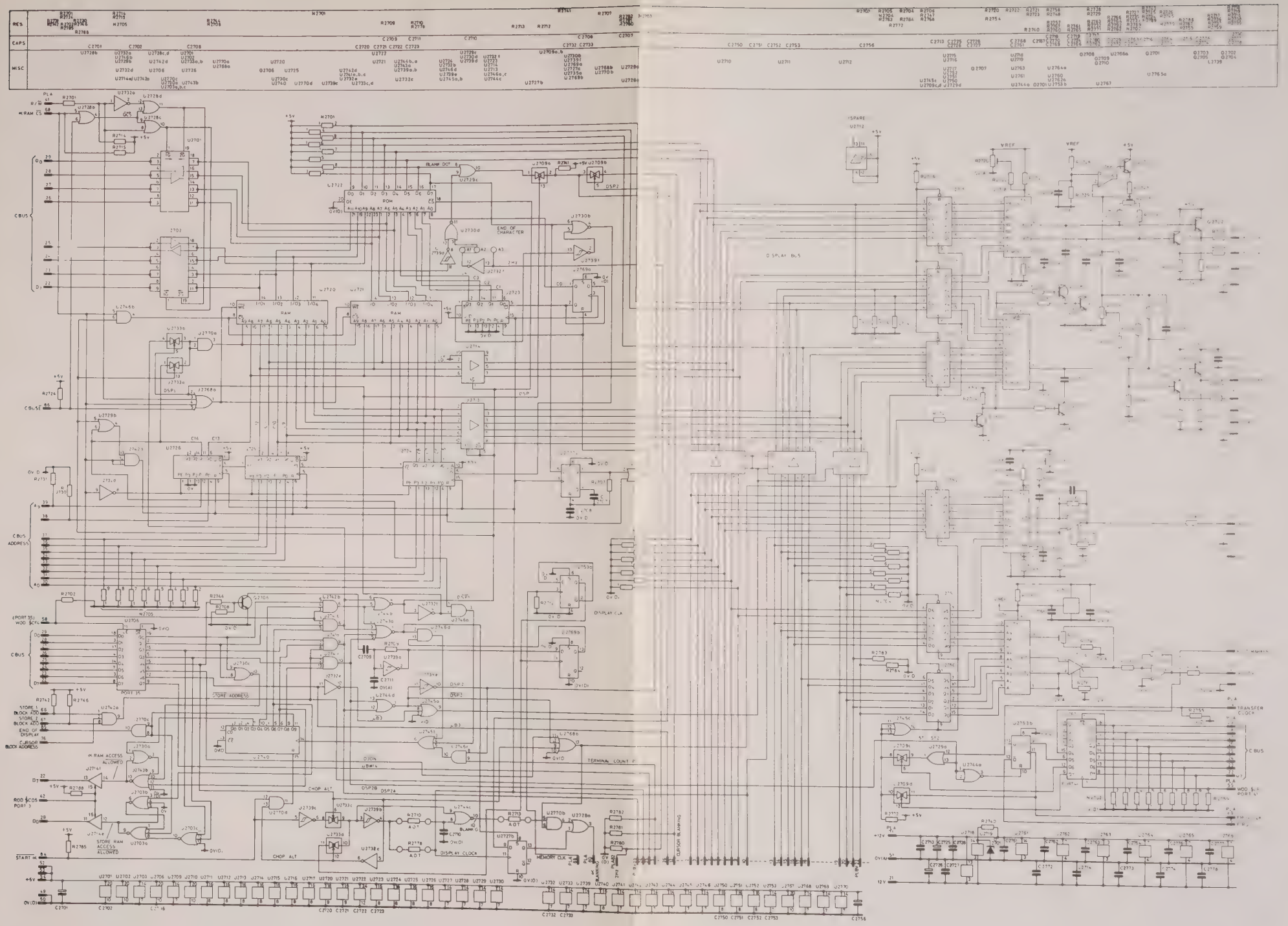


Fig. 6.11 Data Display Circuit Diagram

5110 C.P.U. P.C.B.

Ref	Value	Description	Tol %±	Rating	Part No	Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS											
R2001	1k	CF			21799	R2058	1k8	CF			28725
R2002	1k	CF			21799	R2059	1k	CF			21799
R2003	1k	CF			21799	R2060	180	CF			21795
R2004	1k	CF			21799	R2061	56	CF			28715
R2005	1k	CF			21799	R2062	2k2	CF			21802
R2006	1k	CF			21799	R2063	220	CF			21796
R2007	1k	CF			21799	R2064	2k2	MF	2		38602
R2008	1k	CF			21799	R2065	1k	MF	2		38598
R2009	1k	CF			21799	R2066	3k9	MF	2		38608
R2010	1k	CF			21799	R2067	3k3	CF			21803
R2011	1k	CF			21799	R2068	330	CF			28721
R2012	1k	CF			21799	R2069	560	CF			21798
R2013	1k	CF			21799	R2070	1M	CF			31840
R2014	1k	CF			21799	R2071	22k	CF			21812
R2015	1k	CF			21799	R2072	82k	CF			21818
R2016	1k	CF			21799	R2073	820	CF			28724
R2017	1k	CF			21799	R2074	10k	CF			21809
R2018	1k	CF			21799	R2075	820	CF			28724
R2019	1k	CF			21799	R2076	82k	CF			21818
R2020	1k	CF			21799	R2077	390k	CF			32358
R2021	1k	CF			21799	R2078	4k7	CF			21805
R2022	1k	CF			21799	R2079	4k7	MF	2		38610
R2023	27k	MF	2		38628	R2080	500	PCP			39232
R2024	18k	MF	2		38624	R2081	470	MF	2		38586
R2025	1k	CF			21799	R2082	620	MF	2		38589
R2026	1k	CF			21799	R2083	10k	CF			21809
						R2084	1k	CF			21799
R2028	1k	CF			21799	R2085	82k	CF			21818
R2029	1k	CF			21799	R2086	820	CF			28724
R2030	1k	CF			21799	R2087	4k7	CF			21805
R2031	1k	CF			21799	R2088	2k2	CF			21802
R2032	1k	CF			21799	R2089	47k	CF			21815
R2033	1k	CF			21799	R2090	1k	CF			21799
R2034	1k	CF			21799	R2091	2k2	CF			21802
R2035	1k	CF			21799	R2092	2k2	CF			21802
R2036	2k2	CF			21802	R2093	1k	CF			21799
R2037	1k	CF			21799	R2094	2k2	CF			21802
R2038	4k7	CF			21805	R2095	1k	CF			21799
R2039	1k	CF			21799	R2096	330	CF			28721
R2040	1k	CF			21799	R2097	10k	CF			21809
R2041	1k	CF			21799	R2098	2k2	CF			21802
R2042	1k	CF			21799						
R2043	1k	CF			21799	R2100	10k	CF			21809
R2044	1k	CF			21799	R2101	2k2	CF			21802
R2045	1k	CF			21799	R2102	1k	CF			21799
R2046	1k	CF			21799	R2103	2k2	CF			21802
R2050	1k	CF			21799	N2001	2k2x4	Resistor Network			43185
R2051	1k	CF			21799	N2002	2k2x4	Resistor Network			43185
R2052	1k	CF			21799	N2003	2k2x4	Resistor Network			43185
R2053	1k	CF			21799	N2004	2k2x4	Resistor Network			43185
R2054	1k	CF			21799	N2005	2k2x4	Resistor Network			43185
R2055	1k	CF			21799	N2006	2k2x4	Resistor Network			43185
R2057	2k2	CF			21802	N2020	1kx8	Resistor Network			44892

5110 C.P.U. P.C.B. (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
N2037	3k3x8	Resistor Network			41625
N2038	2k2x4	Resistor Network			43185
N2088	3k3x8	Resistor Network			41625
CAPACITORS					
C2001	10nF	CE(3)			42444
C2002	2.2µF	T		35V	35930
C2003	10nF	CE(3)			42444
C2006	10nF	CE(3)			42444
C2010	10nF	CE(3)			42444
C2012	100nF	CE(3)			43498
C2013	5.6nF	CE(3)			42441
C2015	10nF	CE(3)			42444
C2016	10nF	CE(3)			42444
C2017	10nF	CE(3)			42444
C2018	10nF	CE(3)			42444
C2020	100nF	CE(3)			43498
C2021	10nF	CE(3)			42444
C2022	47nF	CE(3)			43497
C2023	10nF	CE(3)			42444
C2024	10nF	CE(3)			42444
C2027	10nF	CE(3)			42444
C2029	5.6nF	CE(3)			42441
C2030	5.6nF	CE(3)			42441
C2031	5.6nF	CE(3)			42441
C2032	10nF	CE(3)			42444
C2034	10nF	CE(3)			42444
C2035	10nF	CE(3)			42444
C2036	5.6nF	CE(3)			42441
C2040	10nF	CE(3)			42444
C2042	10nF	CE(3)			42444
C2043		Not Fitted			
C2044	22pF	CE(3)			42412
C2045	10pF	CE(3)			42408
C2050	10nF	CE(3)			42444
C2052	10nF	CE(3)			42444
C2053	47nF	CE(3)			43497
C2054	10nF	CE(3)			42444
C2055	47µF	E			32167
C2057	470pF	CE(3)			42428
C2058	10nF	CE(3)			42444
C2059	10nF	CE(3)			42444
C2061	10nF	CE(3)			42444
C2062	10nF	CE(3)			42444
C2063	10nF	CE(3)			42444
C2064	10nF	CE(3)			42444
C2066	10nF	CE(3)			42444
C2068	47nF	CE(3)			43497
C2069	10nF	CE(3)			42444
C2070	220nF	CE(3)			43499
C2071	100pF	CE(3)			42420
C2080	47nF	CE(3)			43497
C2082	10nF	CE(3)			42444
C2085	10nF	CE(3)			42444
C2086	10nF	CE(3)			42408
C2087	100pF	CE(3)			42420
Q2020		2N2369			36625
Q2060		2N3906			21533
DIODES					
D2058		IN4148			23802
D2072		IN4148			23802
D2085		IN4148			23802
D2090		IN4148			23802
U2001		Eprom Programmed			451637
U2002		Eprom Programmed			451638
U2003		Eprom Programmed			451639
U2004		Eprom Programmed			451640
U2005		Eprom Programmed			451641
U2006		Eprom Programmed			451642
U2010		74LS138			40233
U2011		4013			34954
U2012		LM3302N			450917
U2015		74LS00			36730
U2016		74LS00			36730
U2017		74LS10			36857
U2018		74LS14			43379
U2019		10116			39244
U2020		MC6809P			451081
U2021		74LS245			44397
U2022		74LS368			41093
U2023		74LS244			43384

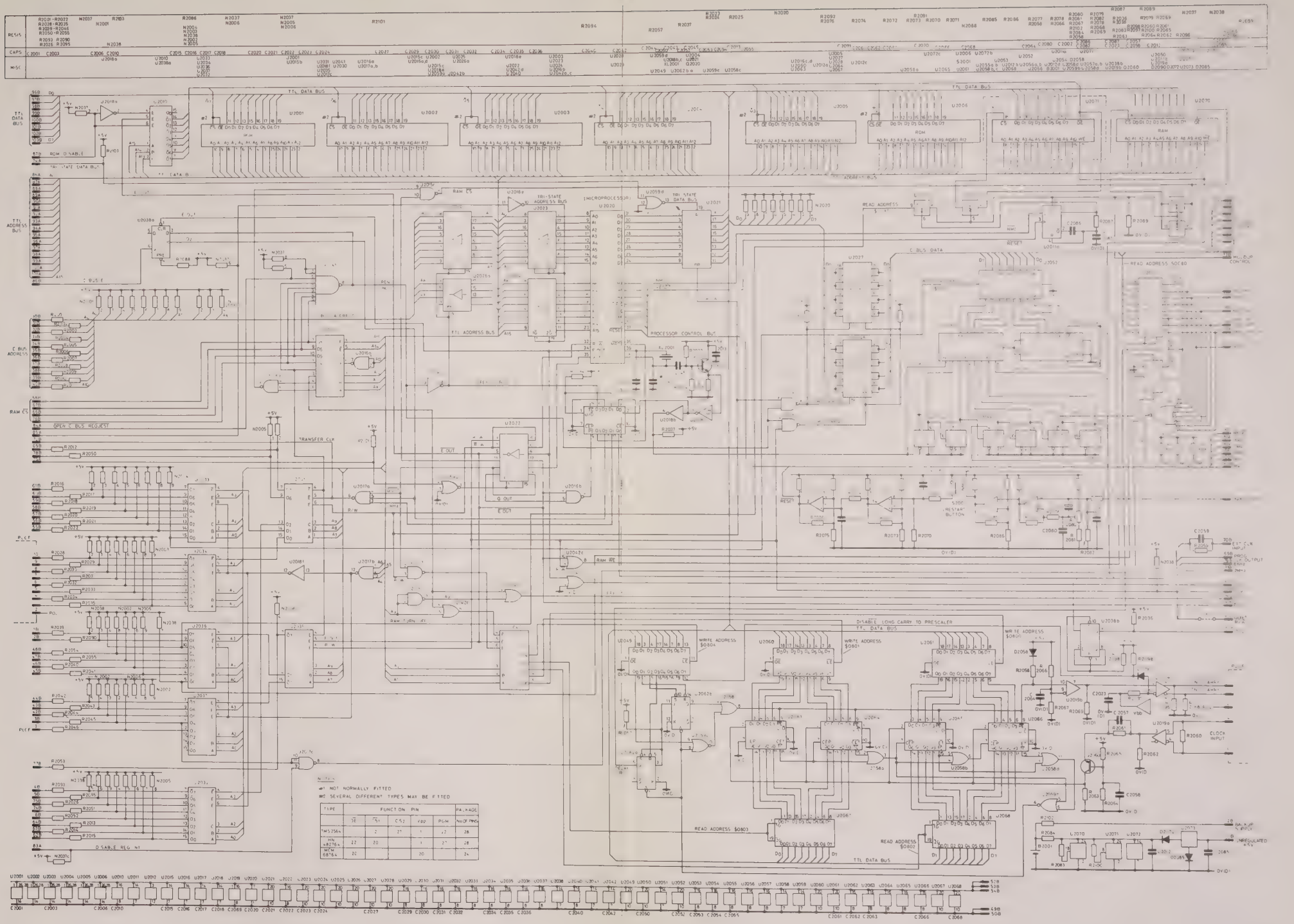


Fig. 6.12 C.P.U. Circuit Diagram

5110 KEYPAD & ENCODER ASSY.

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1841	120	CF			28718
R1842	22k	CF			21812
R1843	22k	CF			21812
R1851	1k	CF			21799
R1852	1k	CF			21799
R1853	100k	CF			21819
R1854	100k	CF			21819
R1855	10k	CF			21809
N1801	180x4	Resistor Network			450937
N1802	180x8	Resistor Network			450938
N1851	4k7x8	Resistor Network			39225
N1852	4k7x8	Resistor Network			39225
N1853	22kx8	Resistor Network			36459
N1854	1Mx8	Resistor Network			450727
N1855	1Mx6	Resistor Network			451571
CAPACITORS					
C1801	100nF	CE(3)			43498
C1802	100nF	CE(3)			43498
C1803	10nF	CE(3)			42444
C1804	10nF	CE(3)			42444
C1841	100nF	CE(3)			43498
C1851	1nF	CE(3)			42432
C1852	1nF	CE(3)			42432
C1853	120pF	CE(3)			42421
C1854	120pF	CE(3)			42421
C1855	100pF	CE(3)			42420
C1856	4700pF	CE(3)			42440
C1857	2200pF	CE(E)		50V	42436
C2858	2200pF	CE(3)			42436
C1861	10nF	CE(3)		25V	450548
C1862	10nF	CE(3)		25V	450548
C1863	10nF	CE(3)		25V	450548
C1864	10nF	CE(3)		25V	450548
C1865	47µF	T		35V	35933
Q1841		OPTOENCODER			450963
Q1842		OPTOENCODER			450963
U1801		74C374			451266
U1802		74C374			451266
U1851		74C244			450913
U1852		74C244			450913
U1853		4075			36204
U1854		74C244			450913
U1855		40174			37057
U1856		4013			34954
U1857		4013			34954
U1858		4093			41299

Ref	Value	Description	Tol %±	Rating	Part No
U1859		4001			36195
U1860		4070			41902
U1861		4013			34954
U1862		4066			40044
DIODES					
D1801		LED YELLOW			450921
D1802		LED YELLOW			450921
D1803		LED YELLOW			450921
D1804		LED YELLOW			450921
D1805		LED GREEN			450922
D1806		LED GREEN			450922
D1807		LED GREEN			450922
D1808		LED GREEN			450922
D1809		IN4148			23802
D1810		IN4148			23802
D1811		IN4148			23802
D1812		IN4148			23802
D1813		IN4148			23802
D1814		IN4148			23802
D1815		IN4148			23802
D1816		IN4148			23802
D1817		IN4148			23802
D1818		IN4148			23802
D1819		IN4148			23802
D1820		IN4148			23802
D1821		IN4148			23802
D1822		IN4148			23802
D1823		IN4148			23802
D1824		IN4148			23802
D1825		IN4148			23802
D1826		IN4148			23802
D1827		IN4148			23802
D1828		IN4148			23802
D1829		IN4148			23802
D1830		IN4148			23802
D1831		IN4148			23802
D1832		IN4148			23802
D1833		IN4148			23802
D1834		IN4148			23802
D1835		IN4148			23802
D1836		IN4148			23802
D1837		IN4148			23802
D1838		IN4148			23802
D1839		IN4148			23802
D1840		IN4148			23802
D1841		IN4148			23802
D1842		IN4148			23802
D1843		IN4148			23802
D1844		IN4148			23802
D1845		IN4148			23802
D1846		IN4148			23802
D1847		IN4148			23802
D1848		IN4148			23802
D1849		IN4148			23802
D1850		IN4148			23802

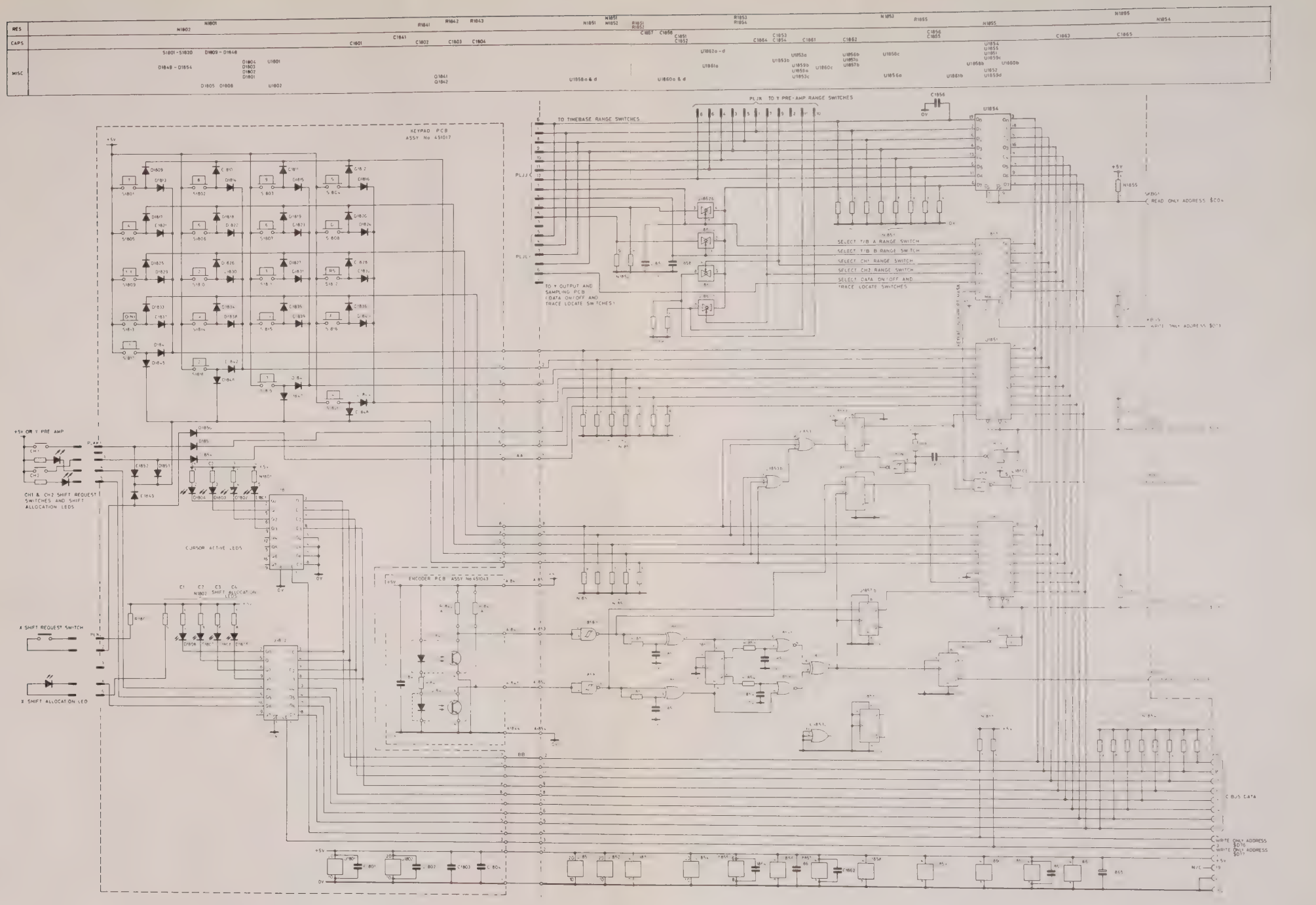

KEYPAD PCB
ASSY No 451017
TO TIMEBASE RANGE SWITCHES
PL1K TO Y PRE-AMP RANGE SWITCHES
TO Y OUTPUT AND SAMPLING PCB (DATA ON/OFF AND TRACE LOCATE SWITCHES)
SELECT T/B A RANGE SWITCH
SELECT T/B B RANGE SWITCH
SELECT CH1 RANGE SWITCH
SELECT CH2 RANGE SWITCH
SELECT DATA ON/OFF AND TRACE LOCATE SWITCHES
+5V OR Y PRE AMP
CH1 & CH2 SHIFT REQUEST SWITCHES AND SHIFT ALLOCATION LEDS
CURSOR ACTIVE LEDS
A SHIFT REQUEST SWITCH
B SHIFT ALLOCATION LED
ENCODER PCB ASSY No 451043
C BUS DATA

Fig. 6.13 Keypad and Encoder Circuit Diagram

5110 IEEE OPTION 5104

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R2901	3k3	CF			21803
R2911	3k3	CF			21803
R2912	1k0	CF			21799
R2915	330	CF			28721
R2917	2k2	CF			21802
R2940	330	CF			28721
R2941	2k2	CF			21802
R2942	2k2	CF			21802
R2943	2k2	CF			21802
R2944	330k	CF			32357
R2945	330k	CF			32357
R2946	2k2	CF			21802
R2952	3k3	CF			21803
R2953	4k7	CF			21805
R2954	4k7	CF			21805
R2955	4k7	CF			21805
R2956	4k7	CF			21805
R2957	4k7	CF			21805
R2958	680	CF			28723
R2959	2k2	CF			21802
N2913	2k2x8	Resistor Network			43185
N2914	2k2x8	Resistor Network			43185
N2921	330x8	Resistor Network			44880
N2922	330x8	Resistor Network			44880
N2931	330x8	Resistor Network			44880
N2935	330x8	Resistor Network			44880
N2941	2k2x8	Resistor Network			43185
N2944	2k2x8	Resistor Network			43185
N2969	2k2x8	Resistor Network			43185
CAPACITORS					
C2901	10nF	CE(3)			42444
C2902	10nF	CE(3)			42444
C2903	10nF	CE(3)			42444
C2904	10nF	CE(3)			42444
C2905	47µF	E		10V	32167
C2906	10nF	CE(3)			42444
C2907	1000µF			16V	32178
C2908	1000µF	E		16V	32178
C2909	47µF	E		10V	32167
C2911	10nF	CE(3)			42444
C2912	10nF	CE(3)			42444
C2913	10nF	CE(3)			42444
C2914	10nF	CE(3)			42444
C2915	220nF	CE(3)			43499
C2916	10nF	CE(3)			42444
C2917	10nF	CE(3)			42444
C2918	270pF	CE(3)			42425
C2932	100pF	CE(3)			42420
C2933	10pF	CE(3)			42408
C2934	100pF	CE(3)			42420
C2935	10pF	CE(3)			42408
C2941	100nF	CE(3)			43498
C2942	10nF	CE(3)			42444
C2943	10nF	CE(3)			42444
C2945	10nF	CE(3)			42444
C2946	10nF	CE(3)			42444
C2948	10nF	CE(3)			42444
C2952	100nF	CE(3)			43498
C2953	10nF	CE(3)			42444
C2955	10nF	CE(3)			42444
C2956	10nF	CE(3)			42444
C2960	10nF	CE(3)			42444
C2961	10nF	CE(3)			42444
C2962	10nF	CE(3)			42444
C2963	10nF	CE(3)			42444
C2964	10nF	CE(3)			42444
C2965	10nF	CE(3)			42444
C2966	10nF	CE(3)			42444
C2967	100nF	CE(3)			43498
C2968	100nF	CE(3)			43498
Q2901		MPS2369			36625
DIODES					
D2901		IN4003			23462
D2902		IN4003			23462
D2903		IN4003			23462
D2904		IN4003			23462
D2951		IN4148			23802
D2952		IN4148			23802
D2953		IN4148			23802
U2901		MC3446			42679
U2902		MC3446			42679
U2903		MC3446			42679
U2904		MC3446			42679
U2905		LM309K			53629
U2911		74LS74			36732
U2912		74LS86			34821
U2913		74C240			451326
U2914		74C244			450913

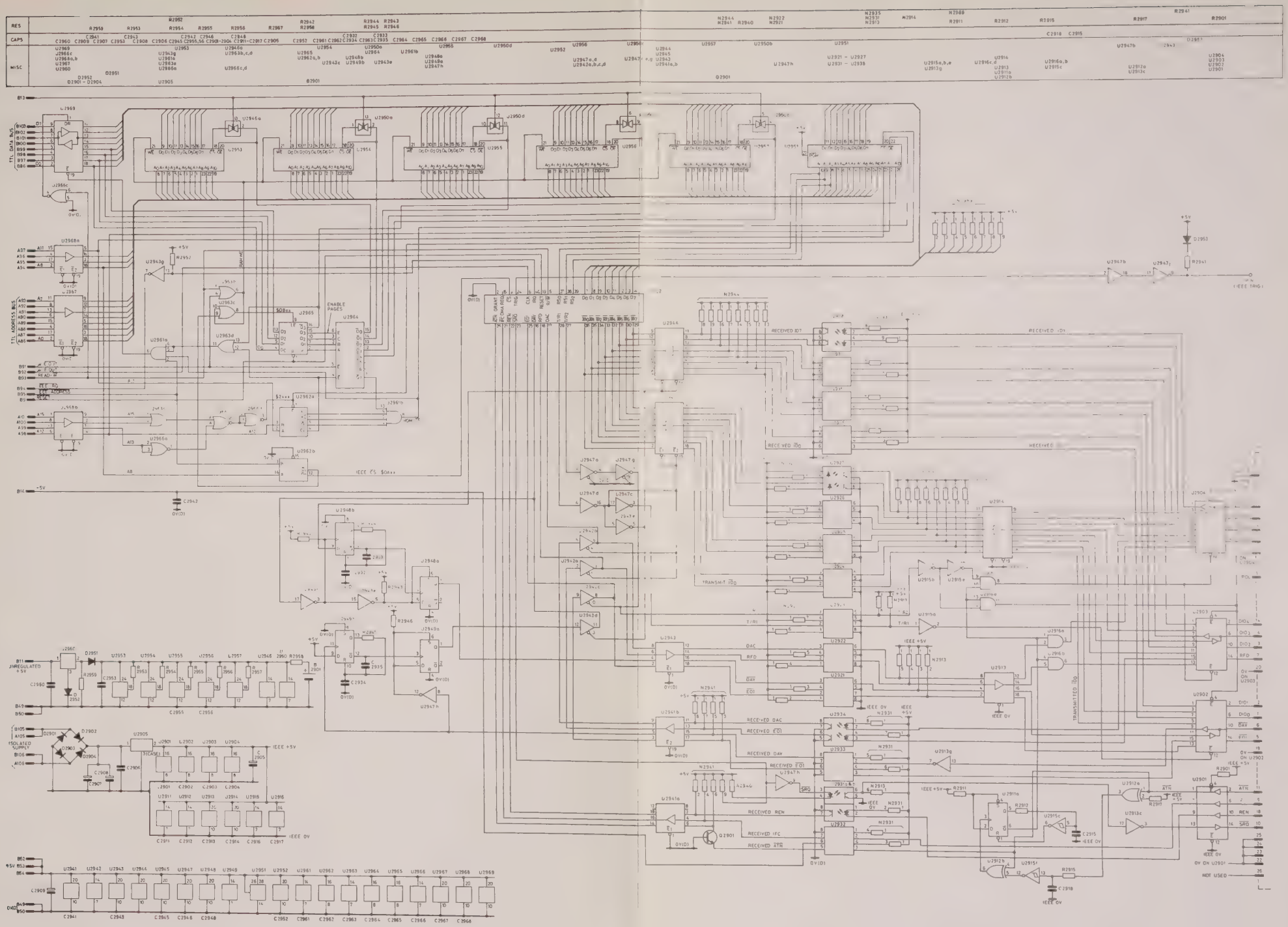


Fig. 6.14 I.E.E.E. Circuit Diagram

5110 POWER SUPPLY

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1001	6k8	CF			21807
R1002	10k	CF			21809
R1003	1k	CF			21799
R1004	470	CF			21797
R1005	500	PCP			39232
R1006	1k1	MF	2		38595
R1007	470	CF			21797
R1009	10	CF			21793
R1010	1k5	MF	2		38598
R1011	200	PCP			39231
R1012	3k	MF	2		38605
R1013	470	MF	2		38586
R1014	3k6	MF	2		38607
R1015	2k7	MF	2		38604
R1016	10	CF			21793
R1017	10	CF			21793
R1018	10	CF			21793
R1020	200	MF	2		38577
R1021	100	PCP			39230
R1022	2k	MF	2		38601
R1030	2k	MF	2		38601
R1031	100	PCP			39230
R1032	200	MF	2		38577
R1041	1k8	WW	5	2½W	17823
R1042	6k8	MF	2		38614
R1043	4k7	MF	2		38610
R1044	3k3	CF			21803
R1060	15	CF		1W	19026
R1061	2k7	MF	2	½W	26728
R1062	18k	MF	2		38624
R1063	3k6	MF	2		38607
R1080	3k3	CF			21803
R1081	15k	CF			28727
CAPACITORS					
C1002	100nF	CE(3)			43498
C1003	10nF	CE(3)			42444
C1004	1µF	T		35V	34895
C1005	10µF	E		25V	32180
C1006	100nF	CE(3)			43498
C1011	22µF	E		25V	32181
C1012	10µF	E		25V	32180
C1013	22µF	E		25V	21181
C1014	100nF	CE(3)			43498
C1021	22µF	E		25V	32181
C1022	10µF	E		25V	32180
C1023	22µF	E		25V	32181
C1024	22µF	E		25V	32181

Ref	Value	Description	Tol %±	Rating	Part No
C1025	22µF	E		25V	32181
C1026	100nF	CE(3)			43498
C1027	100nF	CE(3)			43498
C1031	22µF	E		25V	32181
C1032	10µF	E		25V	32180
C1033	22µF	E		25V	32181
C1034	100nF	CE(3)			43498
C1040	22µF	E		25V	32181
C1041	100nF	CE(3)			43498
C1042	22µF	E		25V	32181
C1050	220µF	E		100V	450848
C1051	220µF	E		100V	450848
C1060	470µF	E		63V	451540
C1061	100µF	E		10V	32168
C1062	100µF	E		10V	32168
C1070	10µF	E		250V	450847
C1071	10µF	E		250V	450847
Q1002		2N6504			44845
Q1060		TIP30A			38415
Q1061		BC182B			33205
Q1080		2N2369			36625
DIODES					
D1003	6V8	ZENER			33931
D1012		IN4003			32771
D1020		IN4003			32771
D1021		IN4003			32771
D1022		IN4003			32771
D1023		IN4003			32771
D1026		IN4001			4103
D1027		IN4001			4103
D1030		IN4003			32771
D1040	33V	ZENER			450673
D1041		IN4003			32771
D1050		IN4003			32771
D1051		IN4003			32771
D1052		IN4003			32771
D1055		IN4003			32771
D1056		IN4003			32771
D1057		IN4003			32771
D1058		IN4003			32771

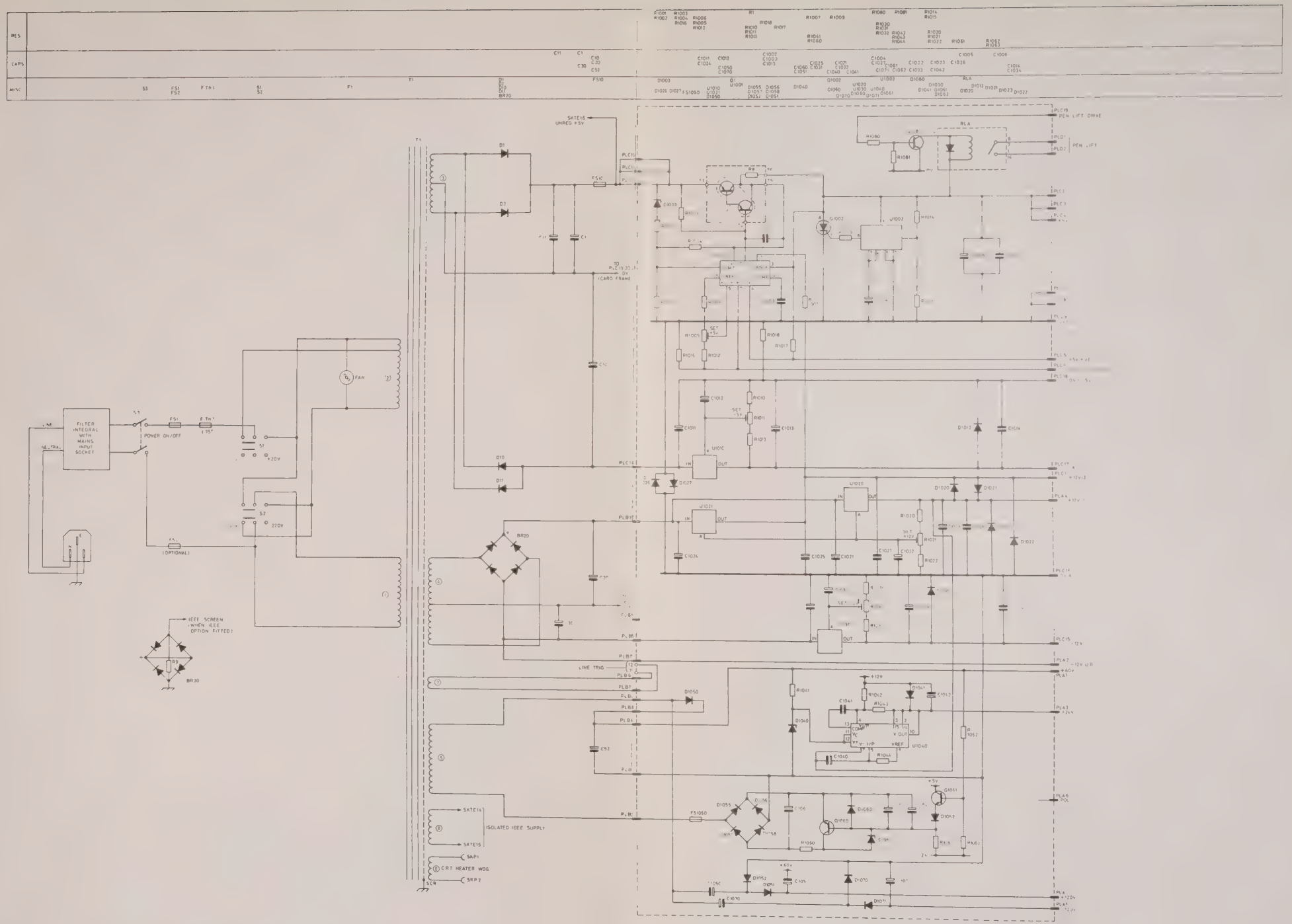


Fig. 6.15 Power Supply Circuit Diagram

RESIS	R1101 R1102 R1105 R1106 R1103 R1109 R1114 R1111 R1112 R1113	R1117 R1118 R1119 R1121 R1126 R1123 R1120 R1125 R1124
CAPS	C1101 C1102 C1104 C1105 C1106	C1109 C1114 C1112 C1111 C1117 C1115 C1113 C1116
MISC	L1101 D1104 D1101 D1102 Q1101 D1103 Q1102 D1105 Q1103	T1101 Q1104 D1107 D1108 D1109 D1116 Q1105 D1115 D1111 D1112 D1114

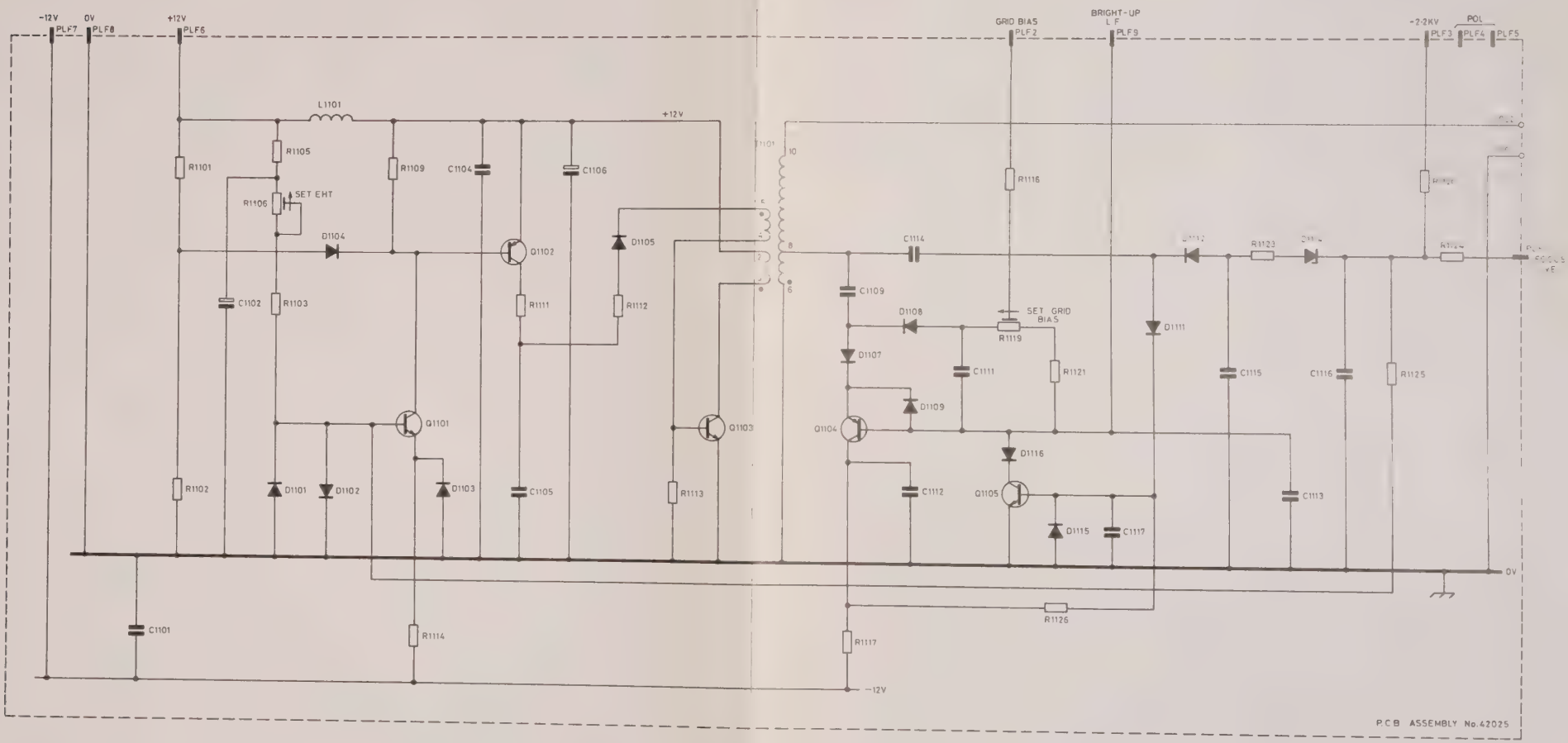


Fig. 6.16 E.H.T. Oscillator Circuit Diagram

5110 TUBEBASE P.C.B.

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R901	2k2	CF			21802
R902	22	CF			28710
R903	5k6	CF			21806
R904	3k3	CF			21803
R905	47	CF			28714
R906	47	CF			28714
R907	2k2	CF			21802
R908	2k2	CF			21902
R909	3k3	CF			21803
R910	47	CF			28714
R911	47	CF			28714
R912	2k2	CF			21802
R913	47	CF		1/8W	43146
R914	47	CF		1/8W	43146
R915	47	CF		1/8W	43146
R916	47	CF		1/8W	43146
R917	560	CF		1/8W	44223
R920	1k	CF			21799
R921	82	CF			28717
R922	120	CF			28718
R923	390	CF			28722
R924	82	CF			28717
R925	120	CF			28718
R926	330	CF			28721
R927	330	CF			28721
R928	220	CF			21796
R929	220	CF			21796
R930	2k2	CF			21802
R932	4k7	CF	2		38610
R933	1k2	CF	2		38596
R934	10	CF			21793
R935	2k2	CF	2		38602
R937	5k6	MF	2		38612
R938	18k	CF			21811
R939	22k	CF			21812
R940	100	CF			21794
R941	36k	MF	2		38631
R942	680	CF			28723
R943	1k5	CF			21801
R944	47k	CF			21815
R945	390	CF			28722
R946	1M	CF			31840
R947	6k8	MF	2		38614
R948	47	CF			28714
R949	33k	CF			21814
R950	5k6	CF			38612
R951	68k	CF			21816
R962	100	CF			21794
R953	10	CF			21793
R954	5k6	CF			21806
R955	22k	CF			21812
R956	10	CF			21793
R960	100k	CF			21819
R961	10k	CF			21809
R962	100k	CF			21819
R964	1k8	CF			28725
R965	1k8	CF			28725
R966	39	CF			28713
R970	22k	CF			21812
R992	120	CF			28718
CAPACITORS					
C902	10nF	CE(3)			42444
C919	10nF	CE(3)			42444
C920	4.7nF	CE(3)			42440
C921	10nF	CE(3)			42444
C922	10nF	CE(3)			42444
C930	10nF	CE(3)			42444
C931	10nF	CE(3)			42444
C932	68pF	CE(3)			42418
C933	100nF	CE(3)		100V	43610
C934	10nF	CE(3)		100V	43609
C935	10nF	CE(3)		200V	450119
C936	10nF	CE(3)		100V	43609
C937	10nF	CE(3)			42444
C945	10nF	PE.		5kV	37854
C960	220pF	CE(2)		3kV	402006
C961	4.7nF	CE(2)		3kV	1514
C962	4.7nF	CE(2)		3kV	1514
C963	4.7nF	CE(2)		3kV	1514
C964	10nF	CE(3)		200V	450119
C965	4.7nF	CE(2)		3kV	1514
C966	4.7nF	CE(2)		3kV	1514
C967	4.7nF	CE(2)		3kV	1514
C980	180pF	CE(3)			42423
Q901		2N3906			21533
Q902		2N3906			21533
Q903		2N3906			21533
Q904		2N3906			21533
Q920		BF479			39270
Q921		BF479			39270
Q922		BF480			450674
Q923		BF480			450674
Q924		BFT96			450675
Q925		BFR96			39019
Q930		2N5771			38089

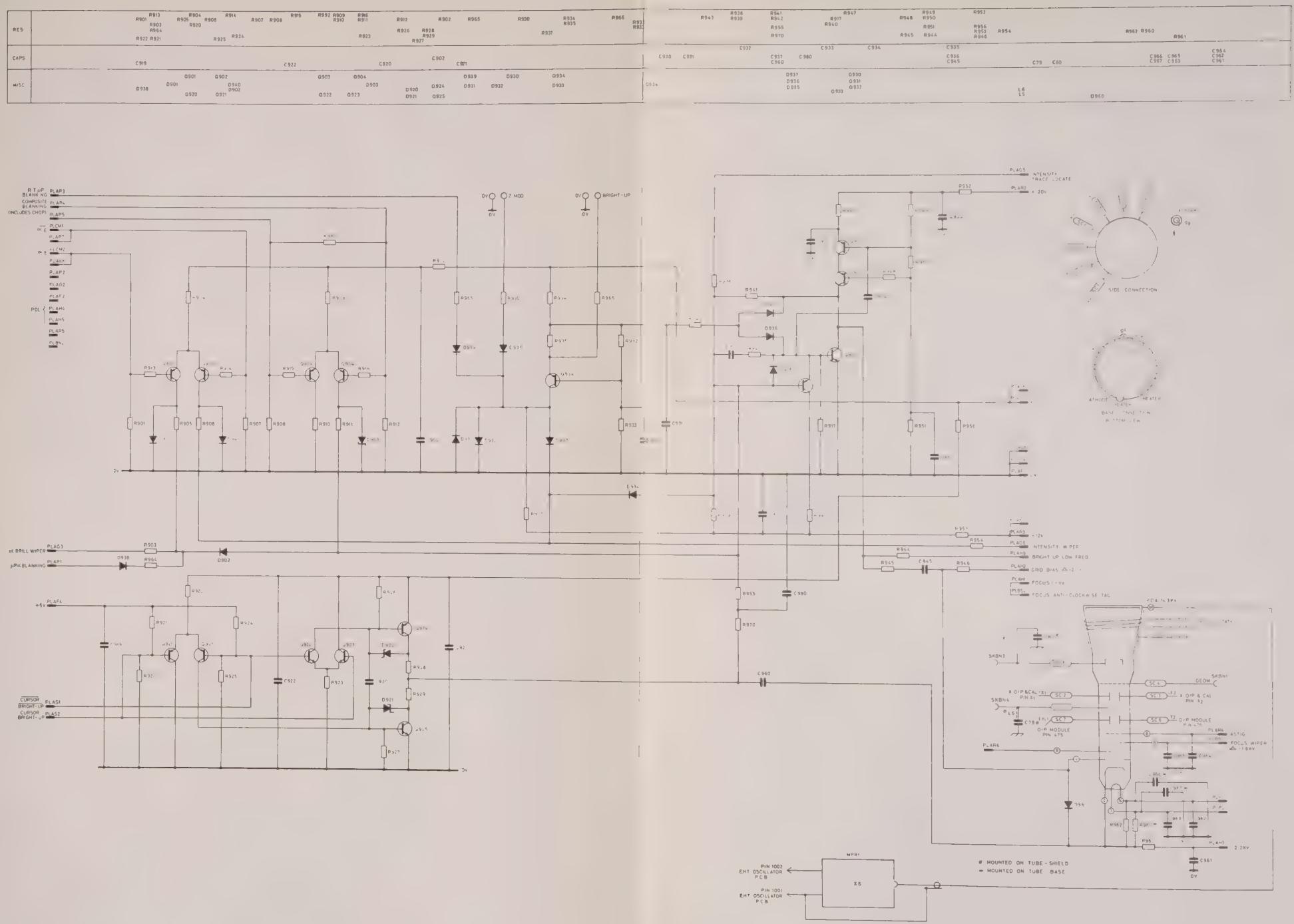


Fig. 6.17 Tubebase Circuit Diagram

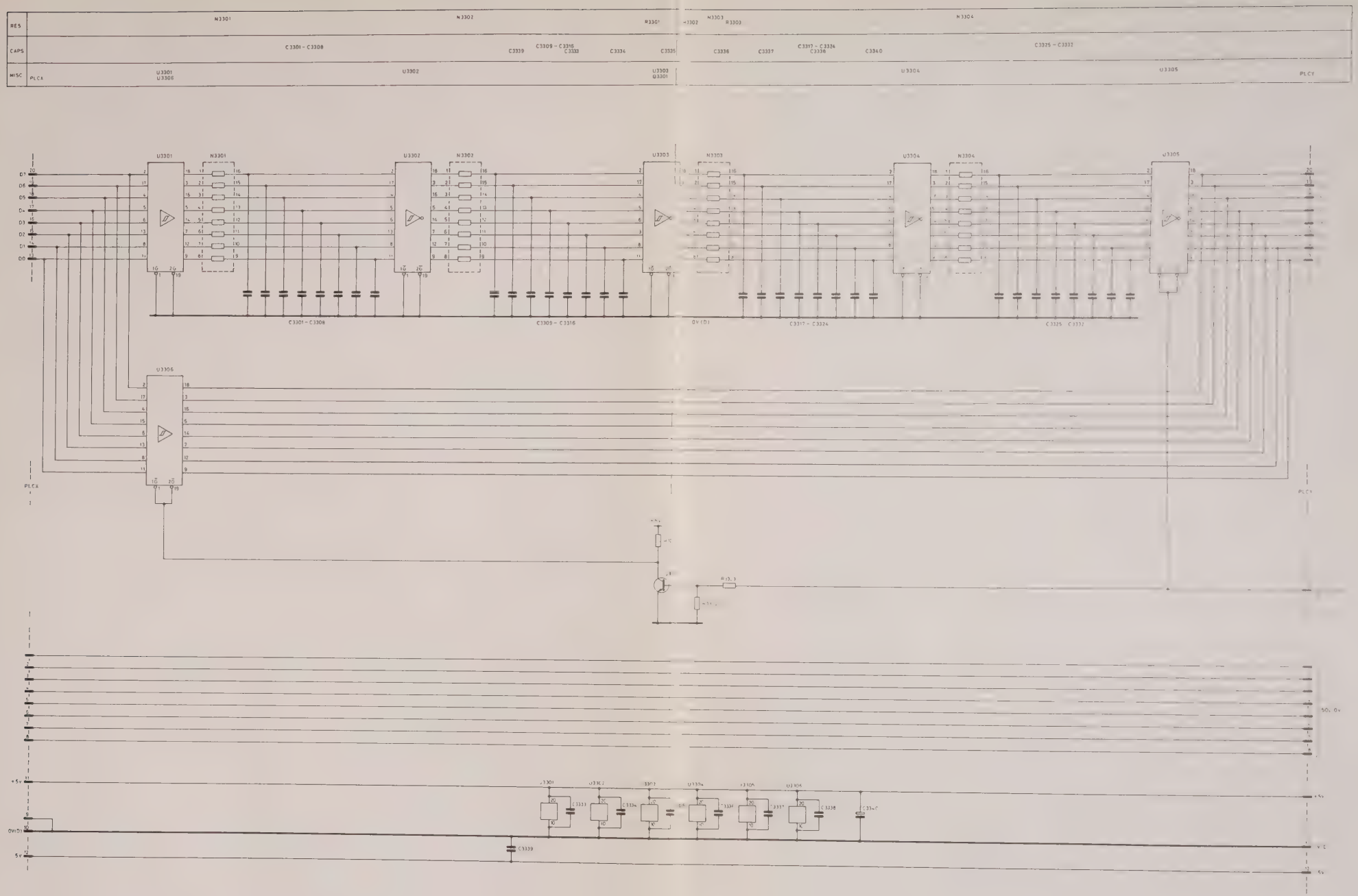


Fig. 6.18 Pod Interface Circuit Diagram

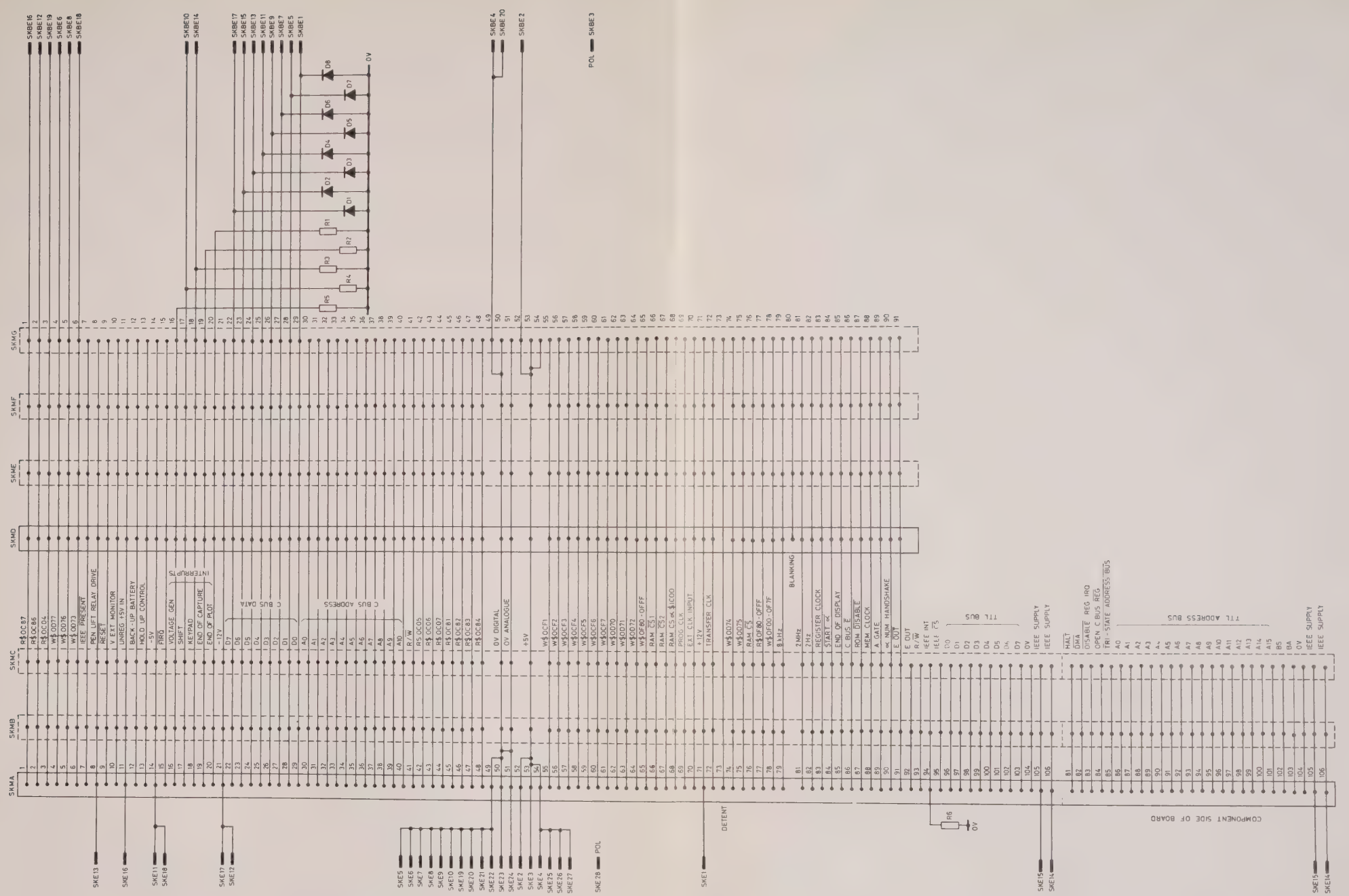


Fig. 6.19 Motherboard Circuit Diagram

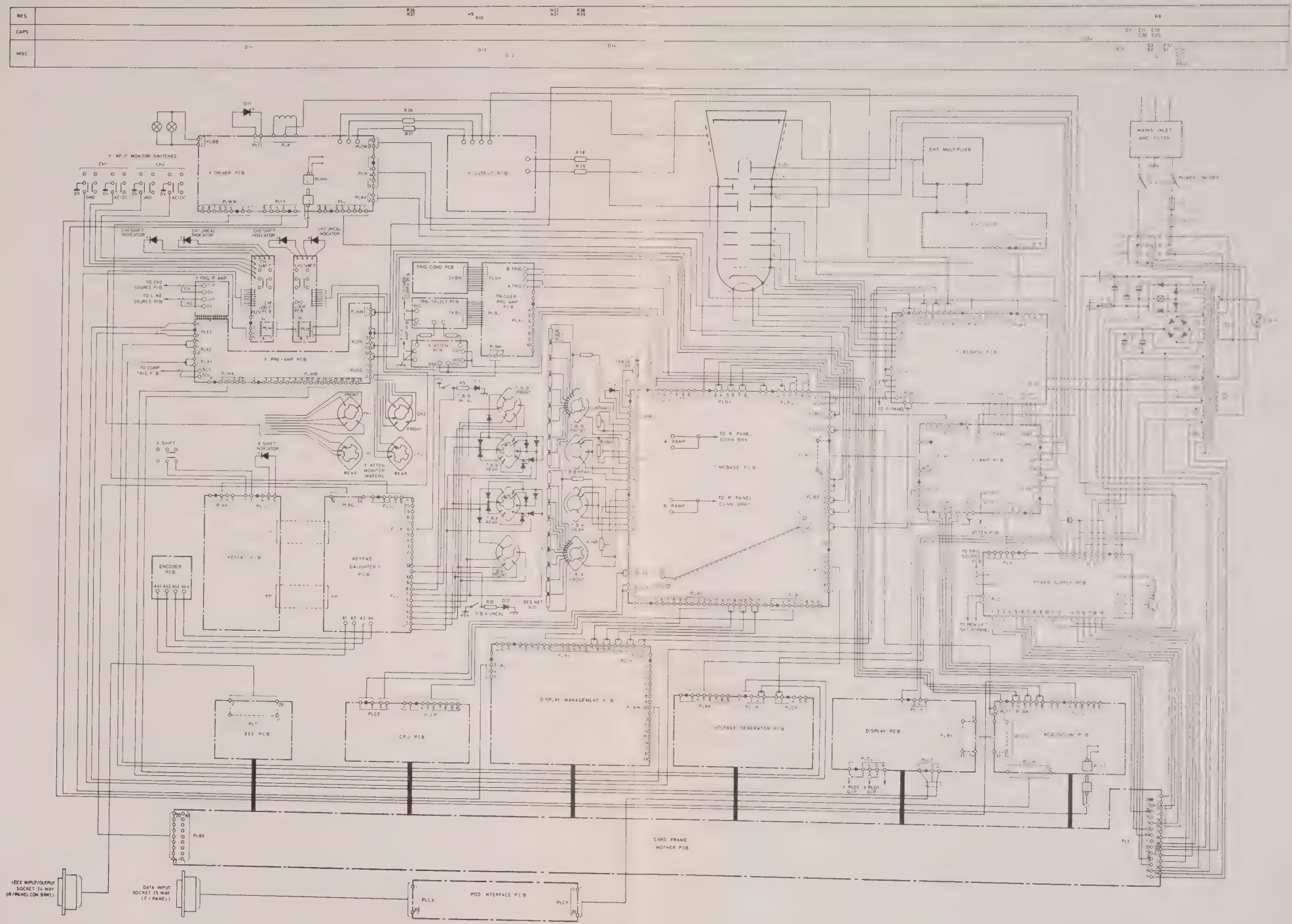
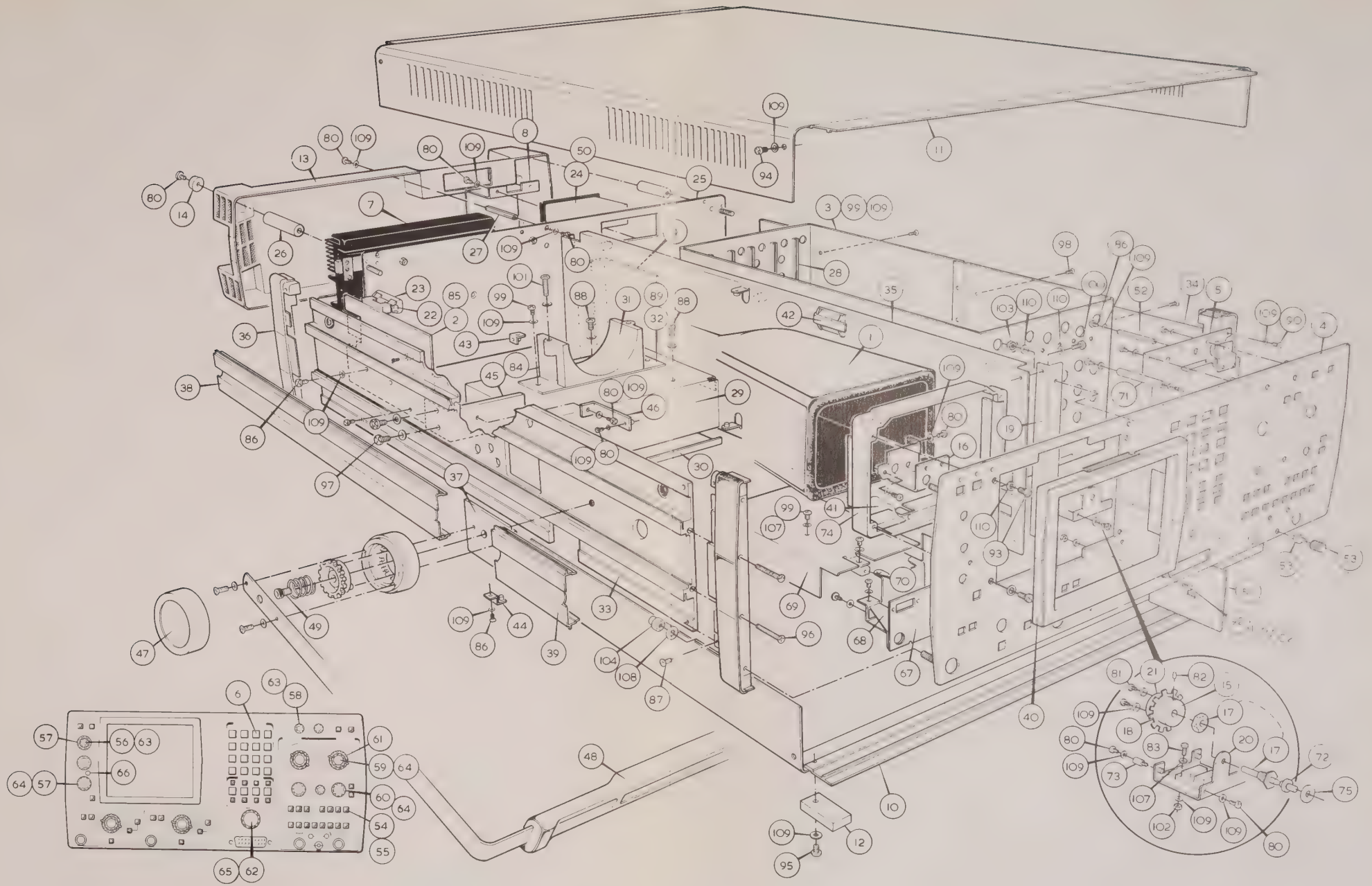


Fig. 6.20 Interconnection Circuit Diagram



Mechanical View Circuit Diagram

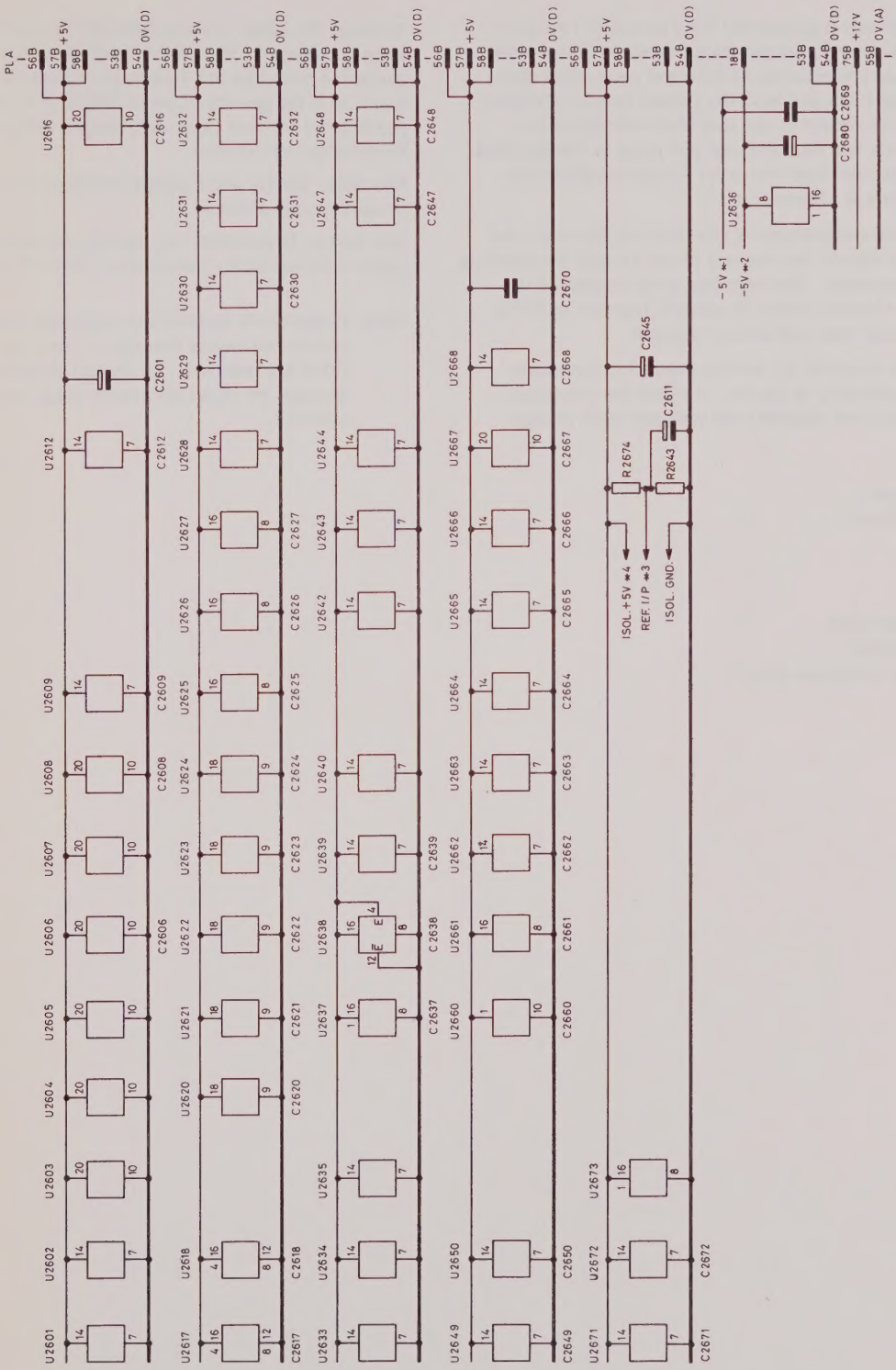


Fig. 6.21 Low Voltage Power Supply Distribution

Guarantee and Service Facilities

Section 7

This instrument is guaranteed for a period of two years from its delivery to the purchaser, covering faulty workmanship and replacement of defective parts other than cathode ray tubes and batteries (where fitted). Cathode ray tubes are subject to the manufacturers guarantee. This assumes fair wear and tear and usage in the specified environment and does not cover routine recalibrations and mechanical adjustments.

We maintain comprehensive after sales facilities and the instrument should be returned to our factory for servicing if this is necessary. The type and serial number of the instrument should always be quoted, together with full details of any fault and service required.

Equipment returned for servicing must be adequately packed, preferably in the box in which the instrument was supplied and shipped with transportation charges prepaid. We accept no responsibility for instruments arriving damaged. Should the cause of failure during the guarantee period be due to misuse or abuse of the instrument, or if the guarantee has expired the repair will be put in hand without delay and charged unless other instructions are received.

Our Sales, Service and Engineering Departments are ready to assist you at all times.

The Service Department can provide maintenance and repair information by telephone or letter, if required.

Note: Please check fuses before returning instruments for service and ensure that any 13 Amp mains plugs fitted are removed. To prevent possible transit damage, we regret that mains plugs cannot be returned.

Service Dept.,
Roebuck Road,
Hainault,
Essex,
IG6 3UE

Tel: 01-500 1000
Telex: 263785
Telegrams: Attenuate Ilford

WL 100 11 83 Issue 1.

45 2896

Manual Part Number ~~470401~~